What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

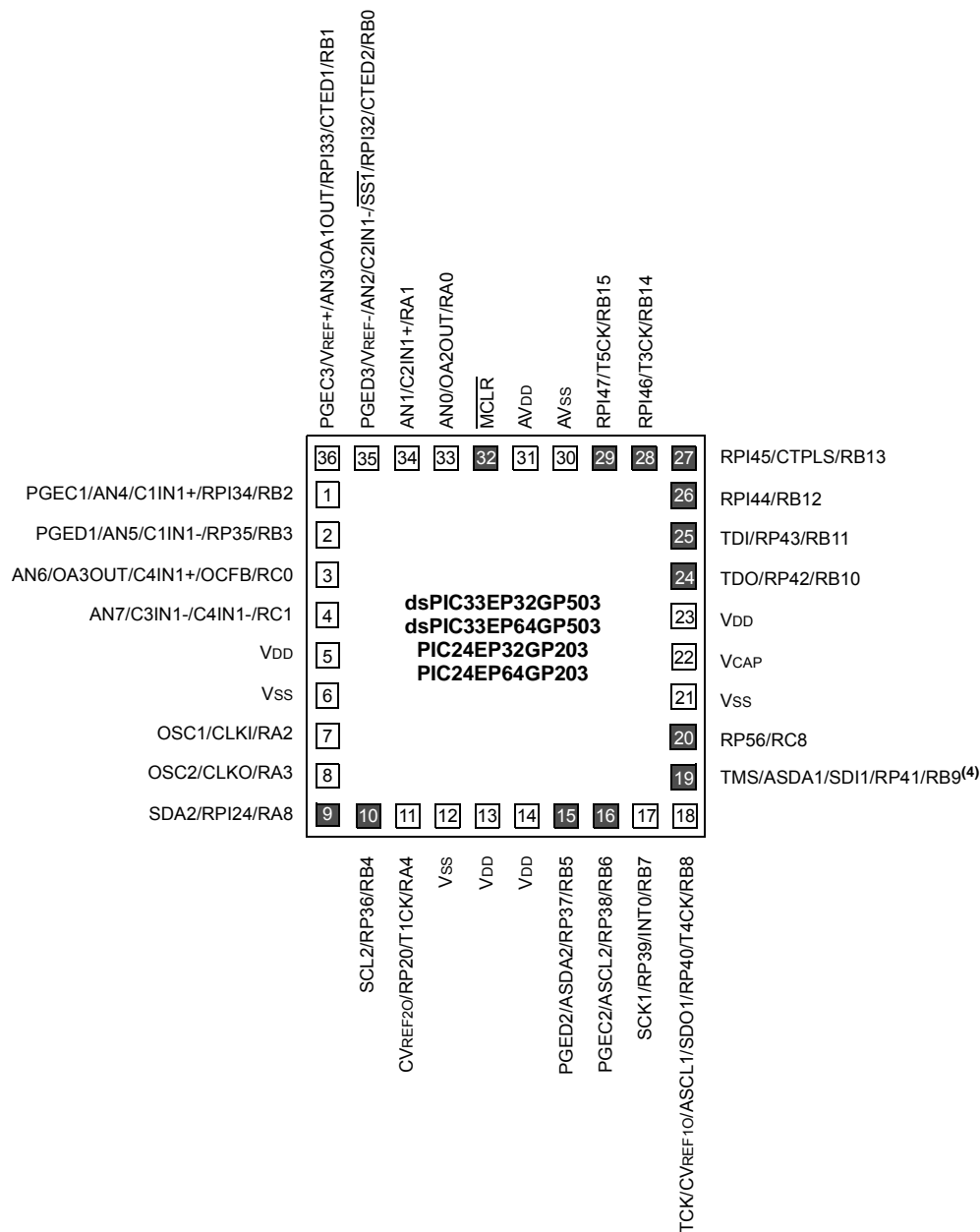## Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512gp204t-i-tl

Pin Diagrams (Continued)

36-Pin VTLA[1,2,3]

⬛ = Pins are up to 5V tolerant

Top pins (left to right, 36 to 27):
- 36 — PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1
- 35 — PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
- 34 — AN1/C2IN1+/RA1
- 33 — AN0/OA2OUT/RA0
- 32 — MCLR
- 31 — AVDD
- 30 — AVSS
- 29 — RPI47/T5CK/RB15
- 28 — RPI46/T3CK/RB14

Left side pins (top to bottom, 1 to 9):
- PGEC1/AN4/C1IN1+/RPI34/RB2 — 1
- PGED1/AN5/C1IN1-/RP35/RB3 — 2
- AN6/OA3OUT/C4IN1+/OCFB/RC0 — 3
- AN7/C3IN1-/C4IN1-/RC1 — 4
- VDD — 5
- VSS — 6
- OSC1/CLKI/RA2 — 7
- OSC2/CLKO/RA3 — 8
- SDA2/RPI24/RA8 — 9

Device center:
dsPIC33EP32GP503
dsPIC33EP64GP503
PIC24EP32GP203
PIC24EP64GP203

Right side pins (top to bottom, 27 to 19):
- 27 — RPI45/CTPLS/RB13
- 26 — RPI44/RB12
- 25 — TDI/RP43/RB11
- 24 — TDO/RP42/RB10
- 23 — VDD
- 22 — VCAP
- 21 — VSS
- 20 — RP56/RC8
- 19 — TMS/ASDA1/SDI1/RP41/RB9[4]

Bottom pins (left to right, 10 to 18):
- 10 — SCL2/RP36/RB4
- 11 — CVREF2O/RP20/T1CK/RA4
- 12 — VSS
- 13 — VDD
- 14 — VDD
- 15 — PGED2/ASDA2/RP37/RB5
- 16 — PGEC2/ASCL2/RP38/RB6
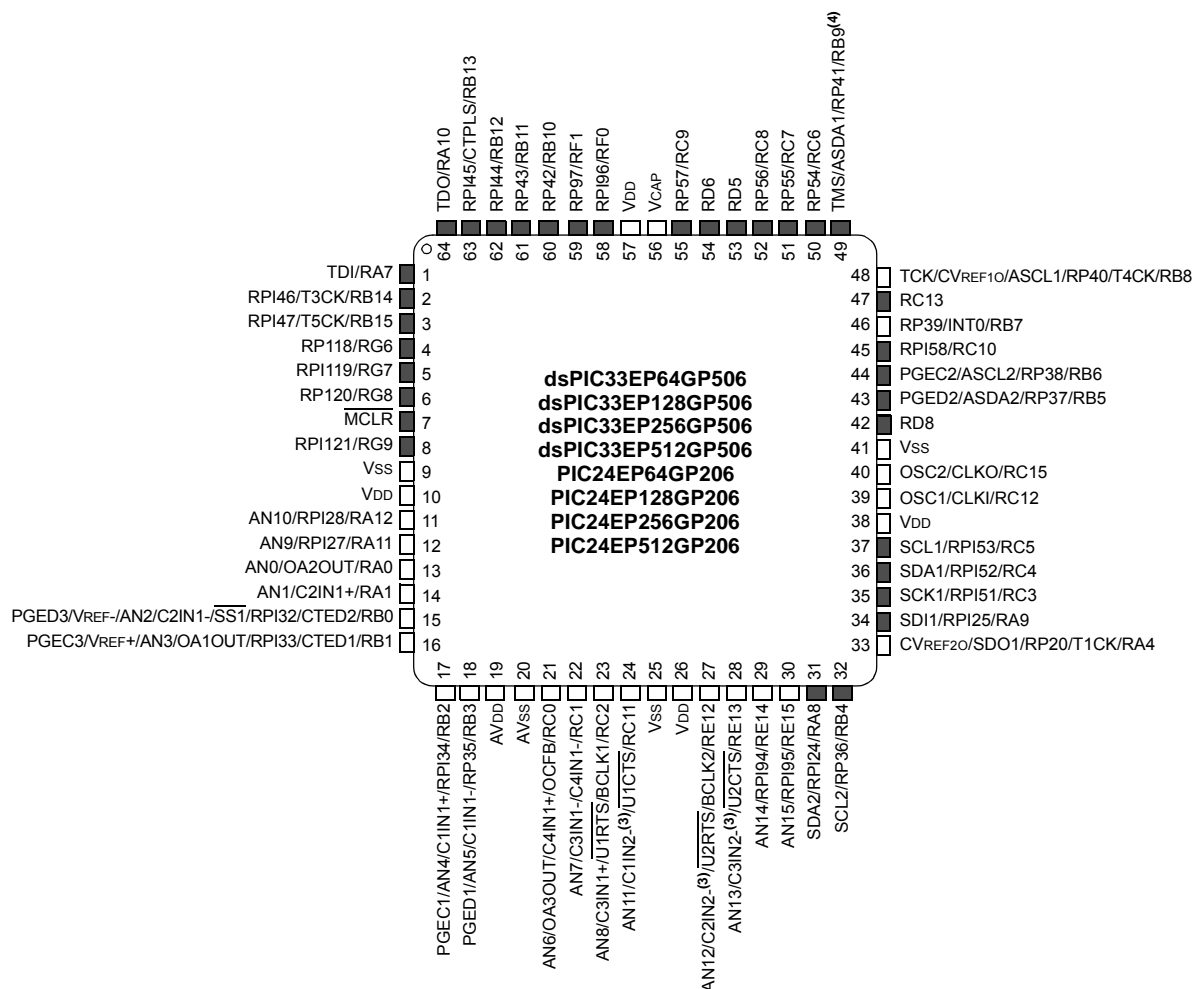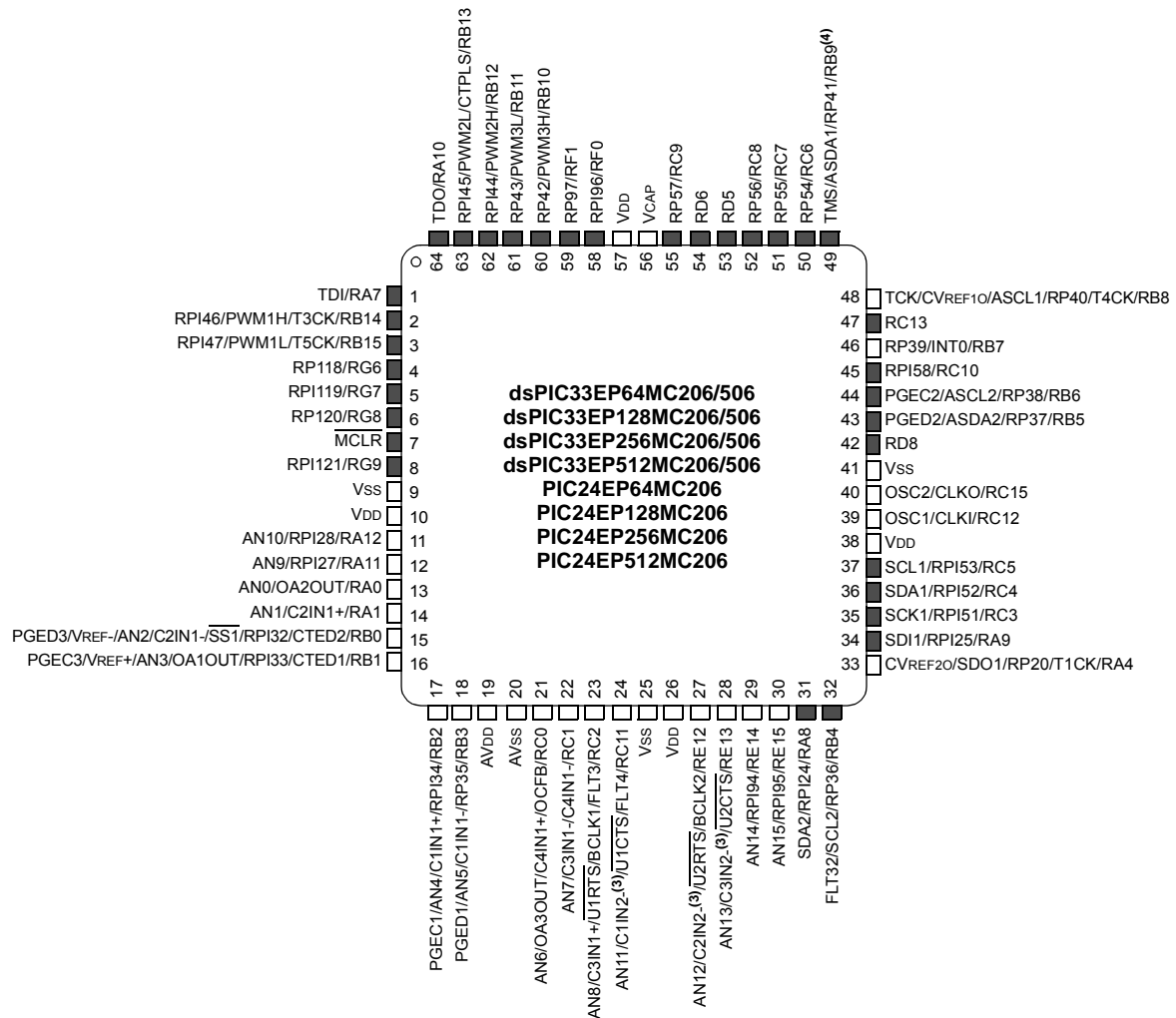- 17 — SCK1/RP39/INT0/RB7
- 18 — TCK/CVREF1O/ASCL1/SDO1/RP40/T4CK/RB8

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Pin Diagrams (Continued)

64-Pin TQFP[1,2,3]

■ = Pins are up to 5V tolerant

dsPIC33EP64GP506
dsPIC33EP128GP506
dsPIC33EP256GP506
dsPIC33EP512GP506
PIC24EP64GP206
PIC24EP128GP206
PIC24EP256GP206
PIC24EP512GP206

Top pins (64–49):
- 64 TDO/RA10
- 63 RPI45/CTPLS/RB13
- 62 RPI44/RB12
- 61 RP43/RB11
- 60 RP42/RB10
- 59 RP97/RF1
- 58 RPI96/RF0
- 57 VDD
- 56 VCAP
- 55 RP57/RC9
- 54 RD6
- 53 RD5
- 52 RP56/RC8
- 51 RP55/RC7
- 50 RP54/RC6
- 49 TMS/ASDA1/RP41/RB9[4]

Left pins (1–16):
- 1 TDI/RA7
- 2 RPI46/T3CK/RB14
- 3 RPI47/T5CK/RB15
- 4 RP118/RG6
- 5 RPI119/RG7
- 6 RP120/RG8
- 7 MCLR
- 8 RPI121/RG9
- 9 VSS
- 10 VDD
- 11 AN10/RPI28/RA12
- 12 AN9/RPI27/RA11
- 13 AN0/OA2OUT/RA0
- 14 AN1/C2IN1+/RA1
- 15 PGED3/VREF-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
- 16 PGEC3/VREF+/AN3/OA1OUT/RPI33/CTED1/RB1

Right pins (48–33):
- 48 TCK/CVREF1O/ASCL1/RP40/T4CK/RB8
- 47 RC13
- 46 RP39/INT0/RB7
- 45 RPI58/RC10
- 44 PGEC2/ASCL2/RP38/RB6
- 43 PGED2/ASDA2/RP37/RB5
- 42 RD8
- 41 VSS
- 40 OSC2/CLKO/RC15
- 39 OSC1/CLKI/RC12
- 38 VDD
- 37 SCL1/RPI53/RC5
- 36 SDA1/RPI52/RC4
- 35 SCK1/RPI51/RC3
- 34 SDI1/RPI25/RA9
- 33 CVREF2O/SDO1/RP20/T1CK/RA4

Bottom pins (17–32):
- 17 PGEC1/AN4/C1IN1+/RPI34/RB2
- 18 PGED1/AN5/C1IN1-/RP35/RB3
- 19 AVDD
- 20 AVSS
- 21 AN6/OA3OUT/C4IN1+/OCFB/RC0
- 22 AN7/C3IN1-/C4IN1-/RC1
- 23 AN8/C3IN1+/U1RTS/BCLK1/RC2
- 24 AN11/C1IN2/U1CTS/RC11
- 25 VSS
- 26 VDD
- 27 AN12/C2IN2-[3]/U2RTS/BCLK2/RE12
- 28 AN13/C3IN2-[3]/U2CTS/RE13
- 29 AN14/RPI94/RE14
- 30 AN15/RPI95/RE15
- 31 SDA2/RPI24/RA8
- 32 SCL2/RP36/RB4

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Pin Diagrams (Continued)

64-Pin TQFP[1,2,3]

■ = Pins are up to 5V tolerant

Top-side pins (64 down to 49):
64 TDO/RA10
63 RPI45/PWM2L/CTPLS/RB13
62 RPI44/PWM2H/RB12
61 RP43/PWM3L/RB11
60 RP42/PWM3H/RB10
59 RP97/RF1
58 RPI96/RF0
57 V$_{DD}$
56 V$_{CAP}$
55 RP57/RC9
54 RD6
53 RD5
52 RP56/RC8
51 RP55/RC7
50 RP54/RC6
49 TMS/ASDA1/RP41/RB9[4]

Left-side pins (1 to 16):
1 TDI/RA7
2 RPI46/PWM1H/T3CK/RB14
3 RPI47/PWM1L/T5CK/RB15
4 RP118/RG6
5 RPI119/RG7
6 RP120/RG8
7 $\overline{MCLR}$
8 RPI121/RG9
9 V$_{SS}$
10 V$_{DD}$
11 AN10/RPI28/RA12
12 AN9/RPI27/RA11
13 AN0/OA2OUT/RA0
14 AN1/C2IN1+/RA1
15 PGED3/V$_{REF}$-/AN2/C2IN1-/$\overline{SS1}$/RPI32/CTED2/RB0
16 PGEC3/V$_{REF}$+/AN3/OA1OUT/RPI33/CTED1/RB1

Center label:
dsPIC33EP64MC206/506
dsPIC33EP128MC206/506
dsPIC33EP256MC206/506
dsPIC33EP512MC206/506
PIC24EP64MC206
PIC24EP128MC206
PIC24EP256MC206
PIC24EP512MC206

Right-side pins (48 to 33):
48 TCK/CV$_{REF1O}$/ASCL1/RP40/T4CK/RB8
47 RC13
46 RP39/INT0/RB7
45 RPI58/RC10
44 PGEC2/ASCL2/RP38/RB6
43 PGED2/ASDA2/RP37/RB5
42 RD8
41 V$_{SS}$
40 OSC2/CLKO/RC15
39 OSC1/CLKI/RC12
38 V$_{DD}$
37 SCL1/RPI53/RC5
36 SDA1/RPI52/RC4
35 SCK1/RPI51/RC3
34 SDI1/RPI25/RA9
33 CV$_{REF2O}$/SDO1/RP20/T1CK/RA4

Bottom-side pins (17 to 32):
17 PGEC1/AN4/C1IN1+/RPI34/RB2
18 PGED1/AN5/C1IN1-/RP35/RB3
19 AV$_{DD}$
20 AV$_{SS}$
21 AN6/OA3OUT/C4IN1+/OCFB/RC0
22 AN7/C3IN1-/C4IN1-/RC1
23 AN8/C3IN1+/U1RTS/BCLK1/FLT3/RC2
24 AN11/C1IN2-/U1CTS/FLT4/RC11
25 V$_{SS}$
26 V$_{DD}$
27 AN12/C2IN2-/U2RTS/BCLK2/RE12
28 AN13/C3IN2-/U2CTS/RE13
29 AN14/RPI94/RE14
30 AN15/RPI95/RE15
31 SDA2/RPI24/RA8
32 FLT32/SCL2/RP36/RB4

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3, or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) DS51765
- *"MPLAB® ICD 3 Design Advisory"* DS51764
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* DS51616
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) DS51749

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator. For details, see **Section 9.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

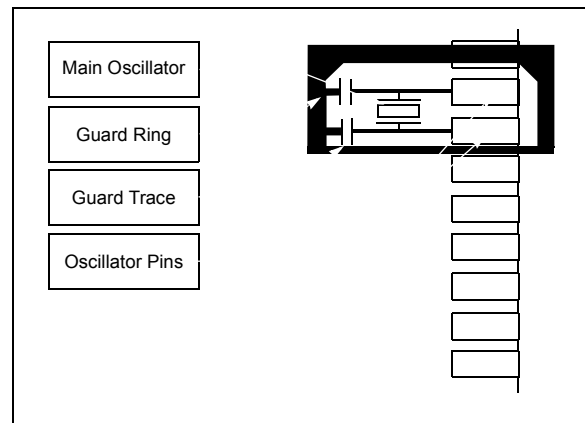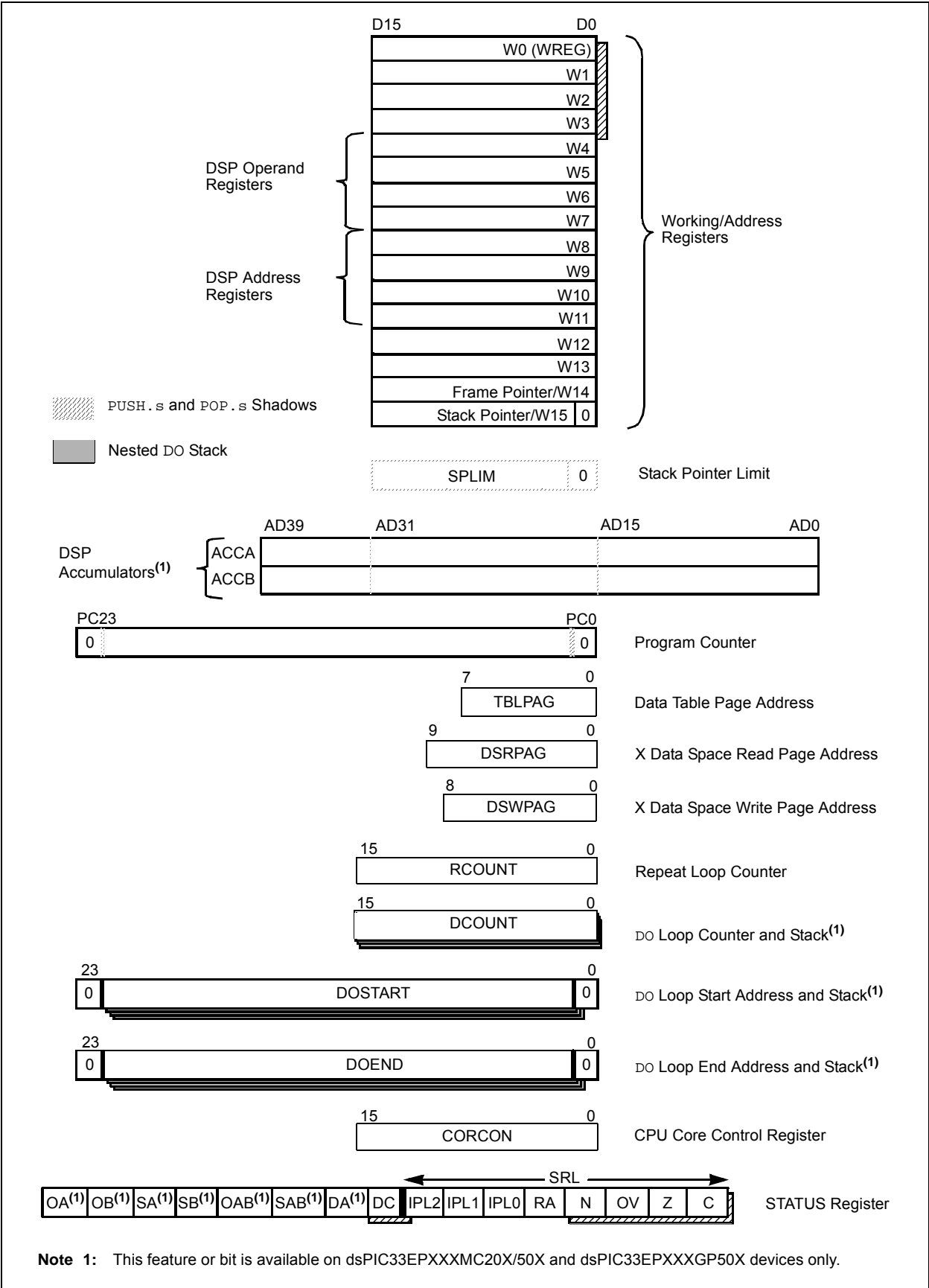**FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT**

FIGURE 3-2: **PROGRAMMER'S MODEL**

Note 1: This feature or bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

3.6   CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/ Devices.aspx?dDocName=en555464

3.6.1   KEY RESOURCES

- **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

4.4.4   SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

> **Note:**   To protect against misaligned stack accesses, W15<0> is fixed to '0' by the hardware.

W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

The Software Stack Pointer always points to the first available free word and fills the software stack working from lower toward higher addresses. Figure 4-19 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-19. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

> **Note 1:**   To maintain system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).
>
> **2:**   As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment

FIGURE 4-19:   **CALL STACK FRAME**
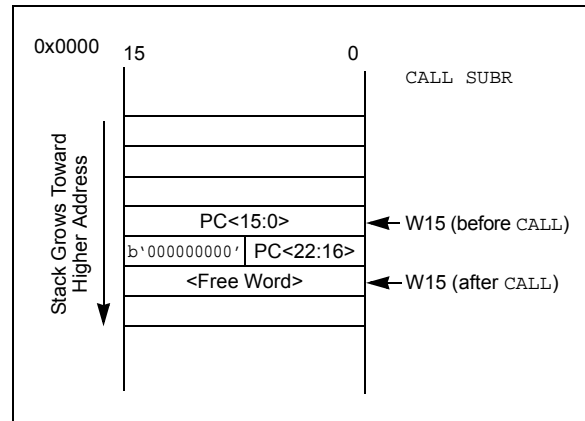
9.1 CPU Clocking System

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency, F_{CY}, is given by Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

$$F_{CY} = F_{osc}/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (F_{IN}) and output frequency (F_{PLLO}). In clock modes S1 and S3, when the PLL output is selected, $F_{OSC} = F_{PLLO}$.

Equation 9-3 provides the relationship between input frequency (F_{IN}) and VCO frequency (F_{VCO}).

FIGURE 9-2: PLL BLOCK DIAGRAM

Note 1: This frequency range must be met at all times.
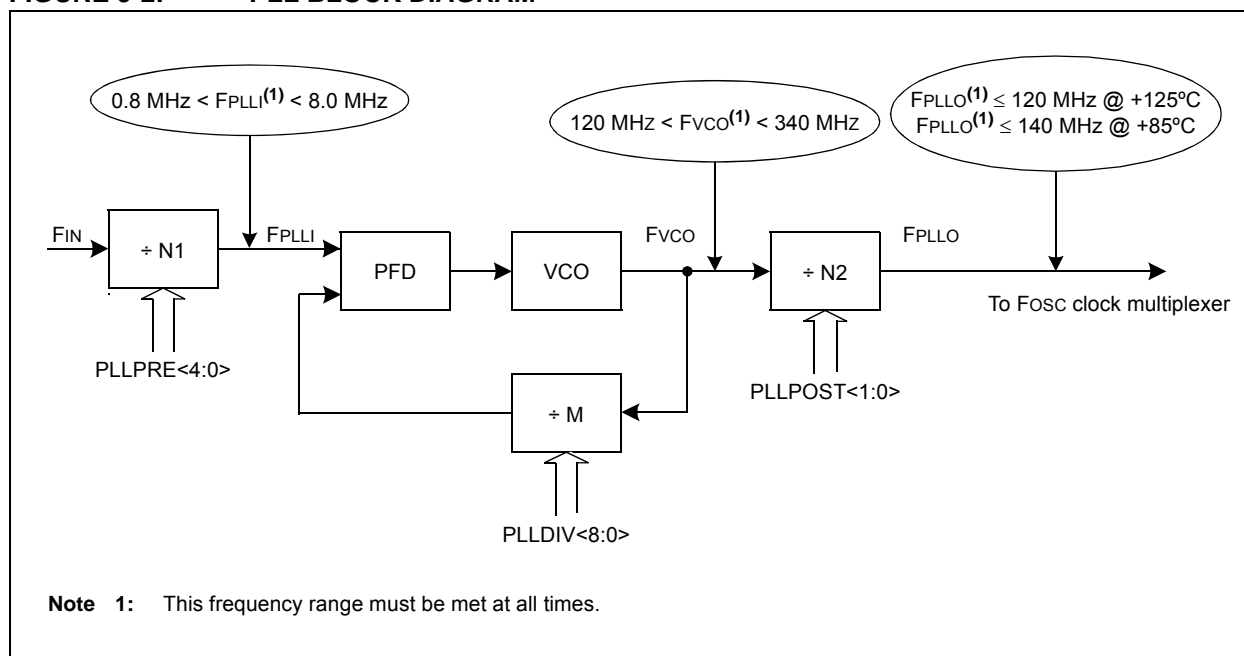
EQUATION 9-2: F_{PLLO} CALCULATION

$$F_{PLLO} = F_{IN} \times \left(\frac{M}{N1 \times N2}\right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)}\right)$$

Where:

$N1 = PLLPRE + 2$

$N2 = 2 \times (PLLPOST + 1)$

$M = PLLDIV + 2$

EQUATION 9-3: F_{VCO} CALCULATION

$$F_{VCO} = F_{IN} \times \left(\frac{M}{N1}\right) = F_{IN} \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)}\right)$$

REGISTER 10-3:   PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	CMPMD	—	—
bit 15							bit 8

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
CRCMD	—	—	—	—	—	I2C2MD	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11   **Unimplemented:** Read as '0'

bit 10   **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled

bit 9-8   **Unimplemented:** Read as '0'

bit 7   **CRCMD:** CRC Module Disable bit
1 = CRC module is disabled
0 = CRC module is enabled

bit 6-2   **Unimplemented:** Read as '0'

bit 1   **I2C2MD:** I2C2 Module Disable bit
1 = I2C2 module is disabled
0 = I2C2 module is enabled

bit 0   **Unimplemented:** Read as '0'

REGISTER 10-4:   PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	—	—	REFOMD	CTMUMD	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4   **Unimplemented:** Read as '0'

bit 3   **REFOMD:** Reference Clock Module Disable bit
1 = Reference clock module is disabled
0 = Reference clock module is enabled

bit 2   **CTMUMD:** CTMU Module Disable bit
1 = CTMU module is disabled
0 = CTMU module is enabled

bit 1-0   **Unimplemented:** Read as '0'

FIGURE 13-3:   TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)

Note 1: The ADC trigger is available on the TMR3:TMR2 andTMR5:TMR4 32-bit timer pairs.
     2: Timerx is a Type B timer (x = 2 and 4).
     3: Timery is a Type C timer (y = 3 and 5).
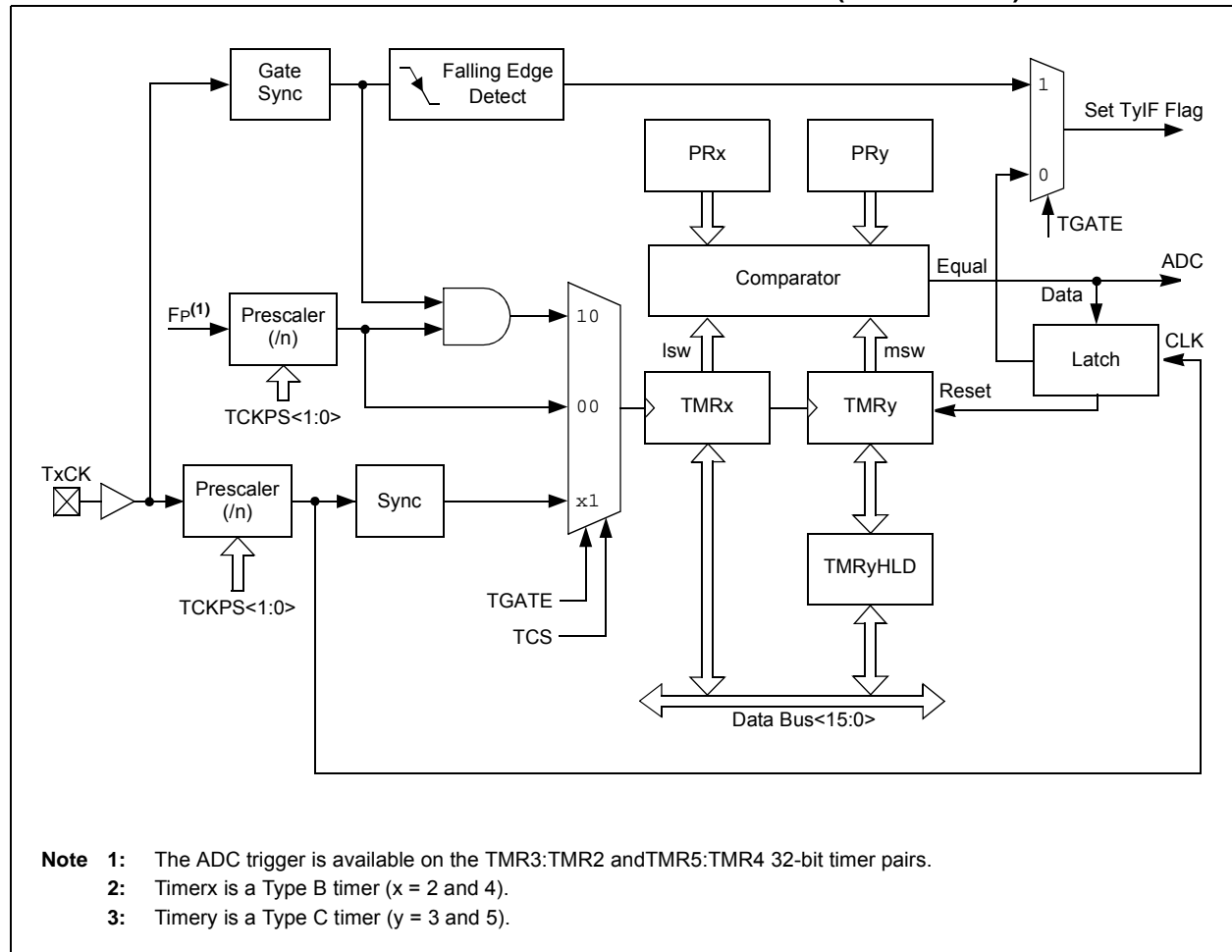
13.1   Timerx/y Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/ wwwproducts/Devices.aspx?d DocName=en555464

13.1.1   KEY RESOURCES

- **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

NOTES:

REGISTER 16-7: **PWMCONx: PWMx CONTROL REGISTER (CONTINUED)**

bit 7-6   **DTC<1:0>:** Dead-Time Control bits

                11 = Dead-Time Compensation mode
                10 = Dead-time function is disabled
                01 = Negative dead time is actively applied for Complementary Output mode
                00 = Positive dead time is actively applied for all output modes

bit 5   **DTCP:** Dead-Time Compensation Polarity bit[3]

                When Set to '1':
                If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened.
                If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened.

                When Set to '0':
                If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened.
                If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.

bit 4   **Unimplemented:** Read as '0'

bit 3   **MTBS:** Master Time Base Select bit

                1 = PWM generator uses the secondary master time base for synchronization and as the clock source for the PWM generation logic (if secondary time base is available)
                0 = PWM generator uses the primary master time base for synchronization and as the clock source for the PWM generation logic

bit 2   **CAM:** Center-Aligned Mode Enable bit[2,4]

                1 = Center-Aligned mode is enabled
                  0 = Edge-Aligned mode is enabled

bit 1   **XPRES:** External PWMx Reset Control bit[5]

                1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
                0 = External pins do not affect PWMx time base

bit 0   **IUE:** Immediate Update Enable bit[2]

                1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate
                0 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.

    2: These bits should not be changed after the PWMx is enabled (PTEN = 1).

    3: DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.

    4: The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.

    5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 23-8:   AD1CSSL: ADC1 INPUT SCAN SELECT REGISTER LOW[1,2]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **CSS<15:0>:** ADC1 Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

Note 1:   On devices with less than 16 analog inputs, all AD1CSSL bits can be selected by the user. However, inputs selected for scan, without a corresponding input on the device, convert V~REFL~.

2:   CSSx = ANx, where x = 0-15.

REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGADJ<15:8>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGADJ<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGADJ<15:0>:** PTG Adjust Register bits

This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGADD command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER[1]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGL0<15:8>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGL0<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGL0<15:0>:** PTG Literal 0 Register bits

This register holds the 16-bit value to be written to the AD1CHS0 register with the PTGCTRL Step command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

29.2   MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an exe-cutable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

• Support for the entire device instruction set
• Support for fixed-point and floating-point data
• Command-line interface
• Rich directive set
• Flexible macro language
• MPLAB X IDE compatibility

29.3   MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

• Integration into MPLAB X IDE projects
• User-defined macros to streamline assembly code
• Conditional assembly for multipurpose source files
• Directives that allow complete control over the assembly process

29.4   MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

• Efficient linking of single libraries instead of many smaller files
• Enhanced code maintainability by grouping related modules together
• Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5   MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

• Support for the entire device instruction set
• Support for fixed-point and floating-point data
• Command-line interface
• Rich directive set
• Flexible macro language
• MPLAB X IDE compatibility

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DI60a	I_{ICL}	**Input Low Injection Current**	0	—	-5[4,7]	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP and RB7
DI60b	I_{ICH}	**Input High Injection Current**	0	—	+5[5,6,7]	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB7 and all 5V tolerant pins[6]
DI60c	ΣI_{ICT}	**Total Input Injection Current (sum of all I/O and control pins)**	-20[8]	—	+20[8]	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ΣI_{ICT}

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

   2: Negative current is defined as current sourced by the pin.

   3: See the **"Pin Diagrams"** section for the 5V tolerant I/O pins.

   4: VIL source < (VSS – 0.3). Characterized but not tested.

   5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

   6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

   7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

   8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 30-25: **SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)**
                TIMING CHARACTERISTICS

Note: Refer to Figure 30-1 for load conditions.
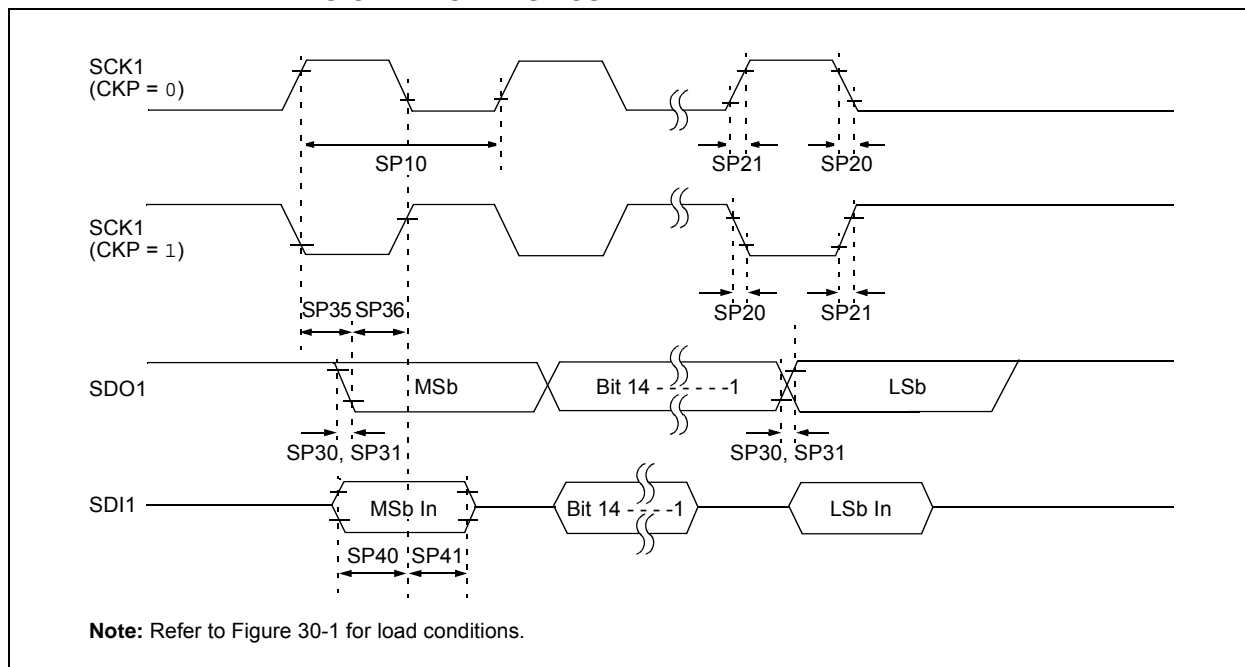
TABLE 30-44: **SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)**
                TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	10	MHz	-40ºC to +125ºC **(Note 3)**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

   2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

   3: The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.

   4: Assumes 50 pF load on all SPI1 pins.

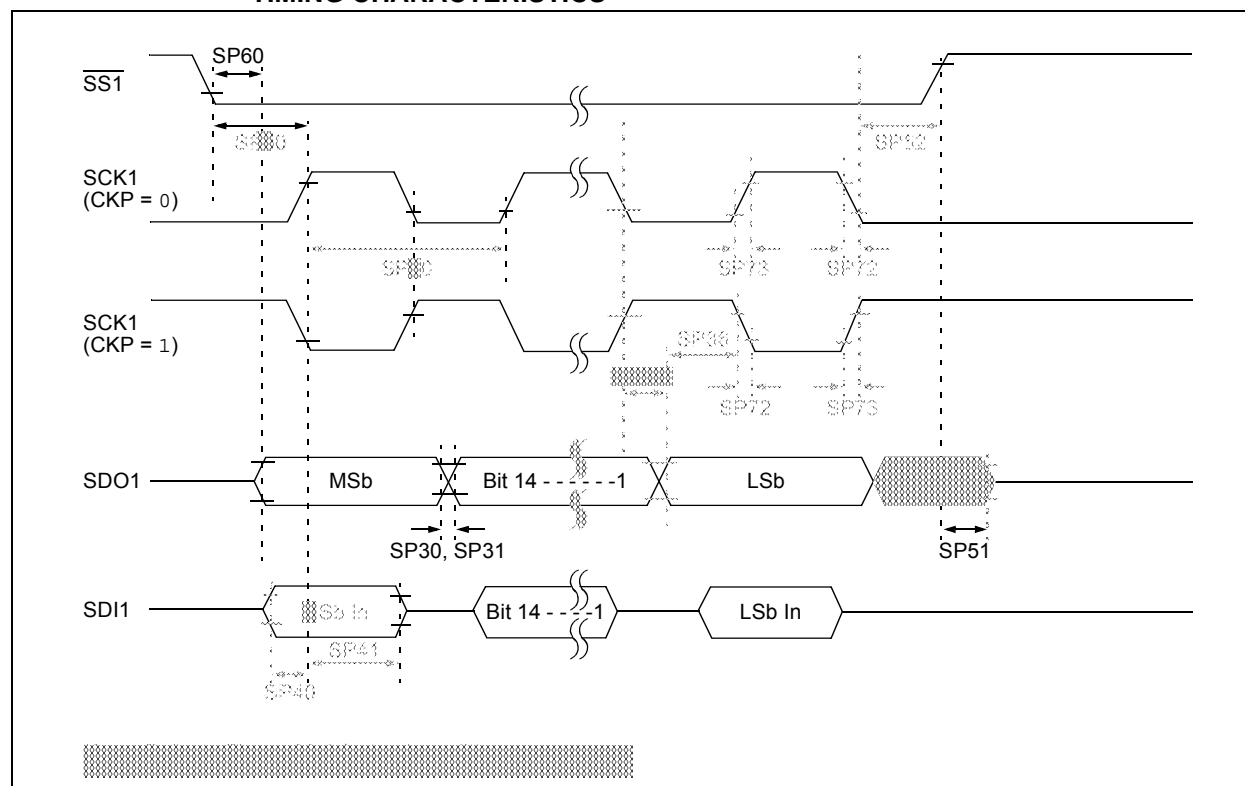**FIGURE 30-26:** **SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**

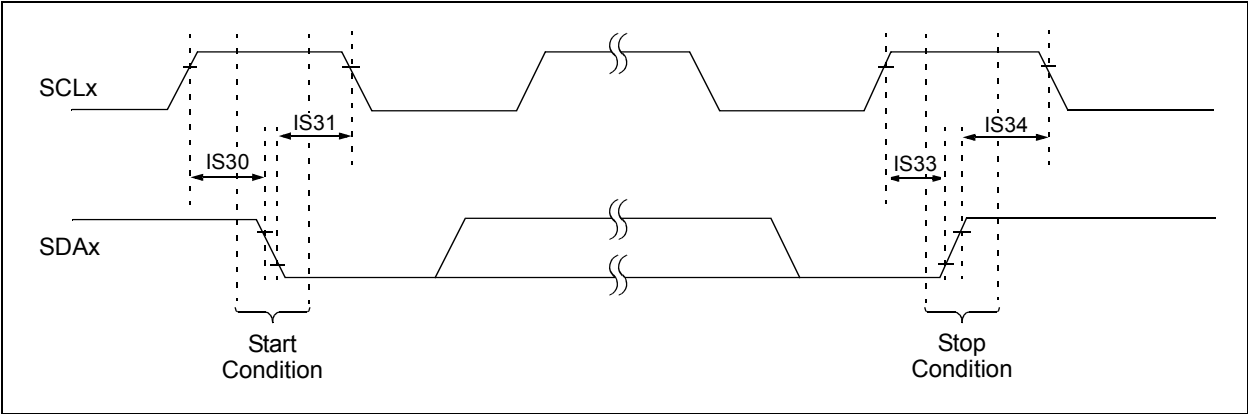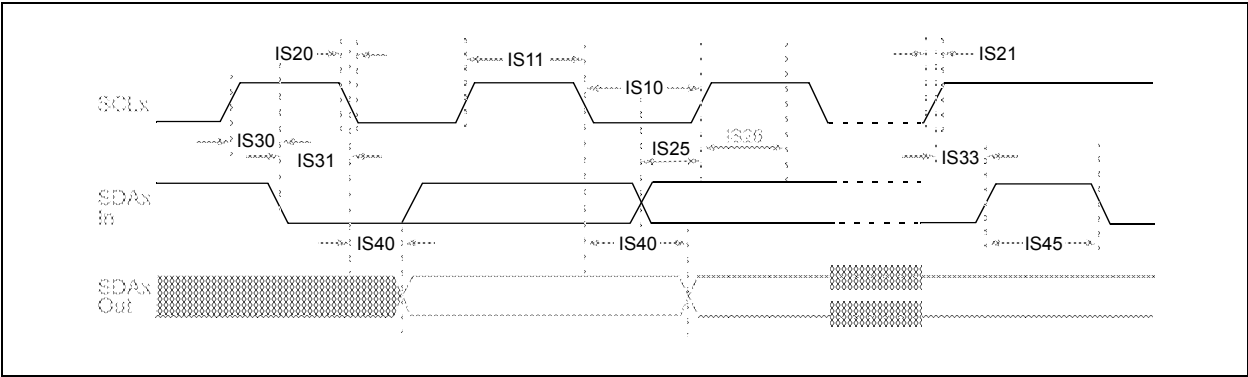**FIGURE 30-32:** **I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**

FIGURE 30-33: **I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**

APPENDIX A: REVISION HISTORY

Revision A (April 2011)

This is the initial released version of the document.

Revision B (July 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-1.

TABLE A-1:   MAJOR SECTION UPDATES

Section Name	Update Description
"High-Performance, 16-bit Digital Signal Controllers and Microcontrollers"	Changed all pin diagrams references of VLAP to TLA.
Section 4.0 "Memory Organization"	Updated the All Resets values for CLKDIV and PLLFBD in the System Control Register Map (see Table 4-35).
Section 5.0 "Flash Program Memory"	Updated "one word" to "two words" in the first paragraph of **Section 5.2 "RTSP Operation"**.
Section 9.0 "Oscillator Configuration"	Updated the PLL Block Diagram (see Figure 9-2).
	Updated the Oscillator Mode, Fast RC Oscillator (FRC) with divide-by-N and PLL (FRCPLL), by changing (FRCDIVN + PLL) to (FRCPLL).
	Changed (FRCDIVN + PLL) to (FRCPLL) for COSC<2:0> = `001` and NOSC<2:0> = `001` in the Oscillator Control Register (see Register 9-1).
	Changed the POR value from 0 to 1 for the DOZE<1:0> bits, from 1 to 0 for the FRCDIV<0> bit, and from 0 to 1 for the PLLPOST<0> bit; Updated the default definitions for the DOZE<2:0> and FRCDIV<2:0> bits and updated all bit definitions for the PLLPOST<1:0> bits in the Clock Divisor Register (see Register 9-2).
	Changed the POR value from 0 to 1 for the PLLDIV<5:4> bits and updated the default definitions for all PLLDIV<8:0> bits in the PLL Feedback Division Register (see Register 9-2).
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Updated the bit definitions for the IRNG<1:0> bits in the CTMU Current Control Register (see Register 22-3).
Section 25.0 "Op amp/ Comparator Module"	Updated the voltage reference block diagrams (see Figure 25-1 and Figure 25-2).