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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512mc202-e-sp">https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512mc202-e-sp</a>

## 2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to  $3 \text{ MHz} < F_{IN} < 5.5 \text{ MHz}$  to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

## 2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

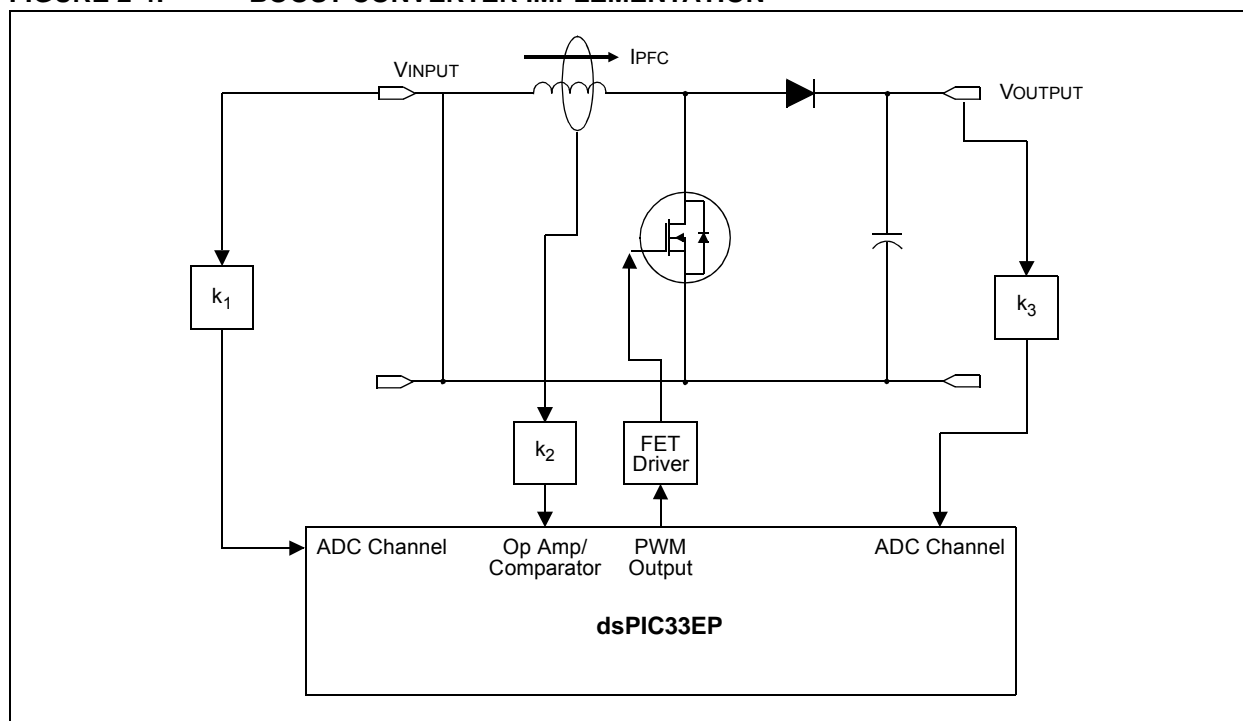
Alternatively, connect a 1k to 10k resistor between Vss and unused pins, and drive the output to logic low.

## 2.9 Application Examples

- Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- Compressor motor control
- Washing machine 3-phase motor control
- BLDC motor control
- Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- Audio and fluid sensor monitoring
- Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- Smart cards and smart card readers

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

**FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION**



**TABLE 4-10: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 4 REGISTER MAP**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
OC1CON1	0900	—	—	OCSIDL	OCTSEL<2:0>			—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000	
OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C	
OC1RS	0904	Output Compare 1 Secondary Register																	xxxx
OC1R	0906	Output Compare 1 Register																	xxxx
OC1TMR	0908	Timer Value 1 Register																	xxxx
OC2CON1	090A	—	—	OCSIDL	OCTSEL<2:0>			—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000	
OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C	
OC2RS	090E	Output Compare 2 Secondary Register																	xxxx
OC2R	0910	Output Compare 2 Register																	xxxx
OC2TMR	0912	Timer Value 2 Register																	xxxx
OC3CON1	0914	—	—	OCSIDL	OCTSEL<2:0>			—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000	
OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C	
OC3RS	0918	Output Compare 3 Secondary Register																	xxxx
OC3R	091A	Output Compare 3 Register																	xxxx
OC3TMR	091C	Timer Value 3 Register																	xxxx
OC4CON1	091E	—	—	OCSIDL	OCTSEL<2:0>			—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000	
OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C	
OC4RS	0922	Output Compare 4 Secondary Register																	xxxx
OC4R	0924	Output Compare 4 Register																	xxxx
OC4TMR	0926	Timer Value 4 Register																	xxxx

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-37: PMD REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	AD1MD	0000
PMD2	0762	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	—	—	CRCMD	—	—	—	—	—	I2C2MD	—	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	CTMUMD	—	—	0000
PMD6	076A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
PMD7	076C	—	—	—	—	—	—	—	—	—	—	—	DMA0MD	PTGMD	—	—	—	0000
													DMA1MD					
													DMA2MD					
													DMA3MD					

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-38: PMD REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QE11MD	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	AD1MD	0000
PMD2	0762	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	—	—	CRCMD	—	—	—	—	—	I2C2MD	—	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	CTMUMD	—	—	0000
PMD6	076A	—	—	—	—	—	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	076C	—	—	—	—	—	—	—	—	—	—	—	DMA0MD	PTGMD	—	—	—	0000
													DMA1MD					
													DMA2MD					
													DMA3MD					

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

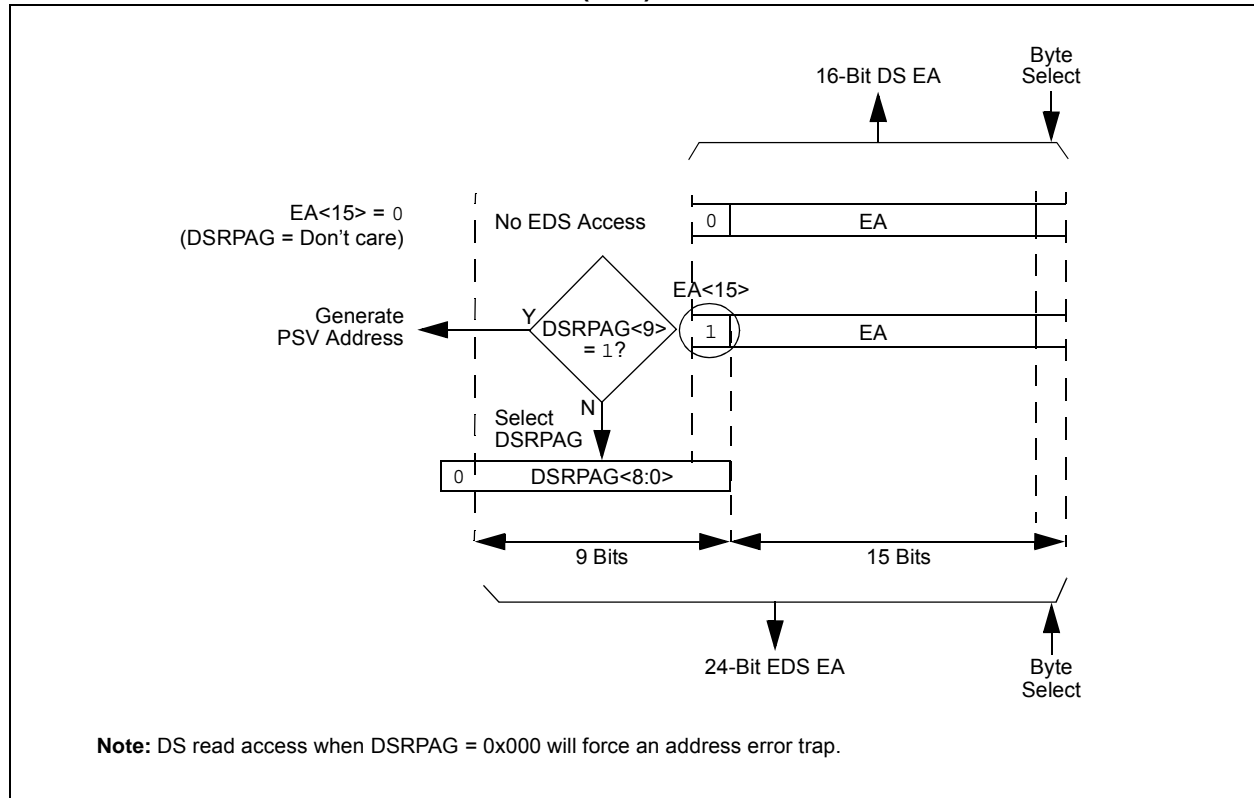
#### 4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre-modified and post-modified Effective Addresses (EA). The upper half of the base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Read Page register (DSRPAG) or the 9-bit Write Page register (DSWPAG), to form an Extended Data Space (EDS)

address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Example 4-1. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when base address bit, EA<15> = 1, DSWPAG<8:0> are concatenated onto EA<14:0> to form the 24-bit EDS write address.

#### EXAMPLE 4-1: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION



#### 4.4.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible regardless of the contents of the Data Space Page registers. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space, in combination with DSRPAG = 0x000 or DSWPAG = 0x000. Consequently, DSRPAG and DSWPAG are initialized to 0x001 at Reset.

**Note 1:** DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.

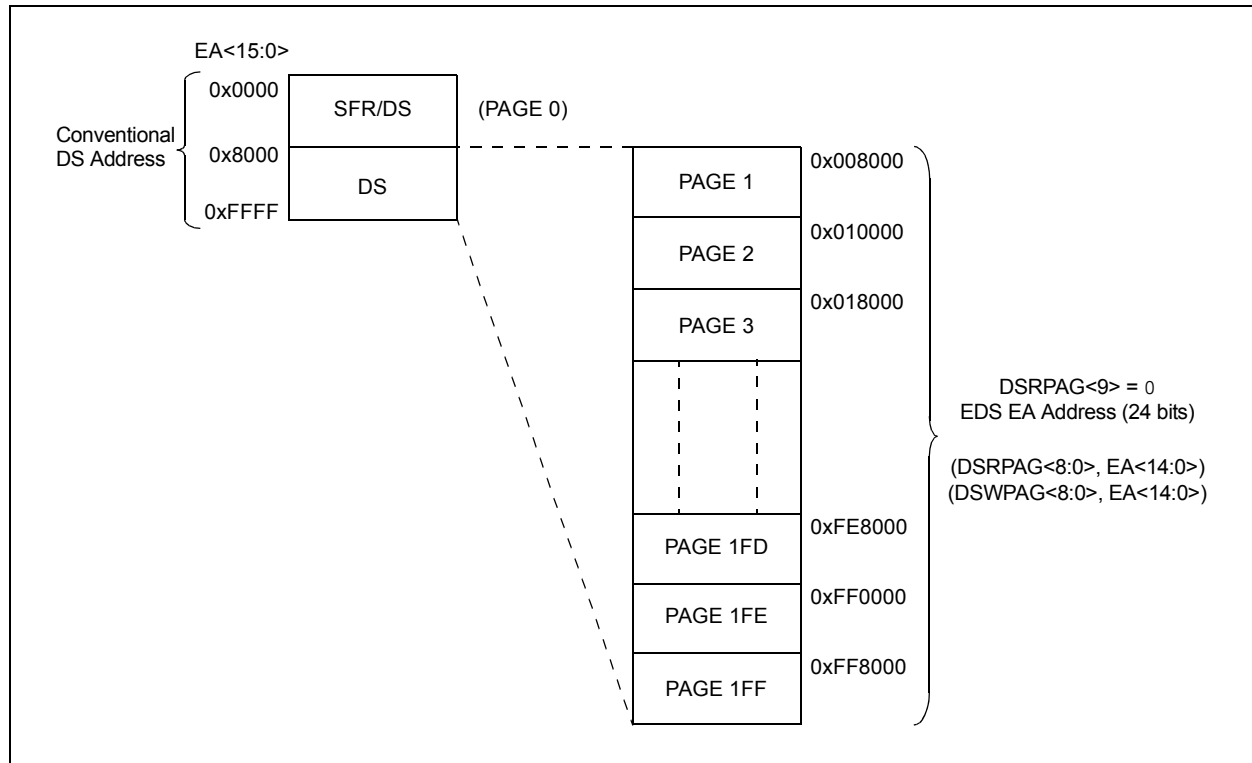
**2:** Clearing the DSxPAG in software has no effect.

The remaining pages, including both EDS and PSV pages, are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA<15> = 1.

For example, when DSRPAG = 0x001 or DSWPAG = 0x001, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF, of the Data Space will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x002 or DSWPAG = 0x002, accesses to the upper 32 Kbytes of the Data Space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-17.

For more information on the PSV page access using Data Space Page registers, refer to the “**Program Space Visibility from Data Space**” section in “**Program Memory**” (DS70613) of the “*dsPIC33/PIC24 Family Reference Manual*”.

**FIGURE 4-17: EDS MEMORY MAP**



**REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

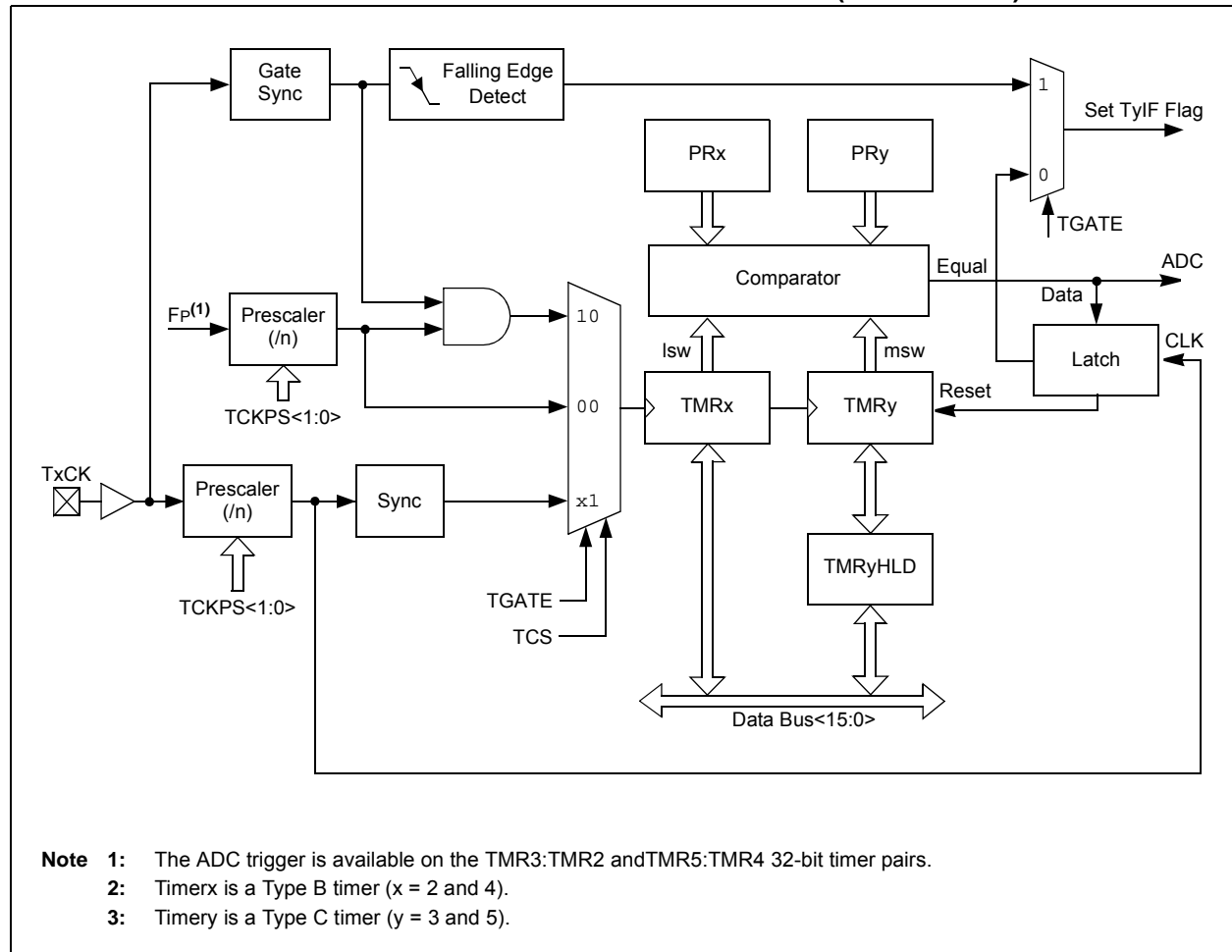
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	RQCOL3	RQCOL2	RQCOL1	RQCOL0
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-4      **Unimplemented:** Read as '0'
- bit 3      **RQCOL3:** DMA Channel 3 Transfer Request Collision Flag bit
  - 1 = User force and interrupt-based request collision is detected
  - 0 = No request collision is detected
- bit 2      **RQCOL2:** DMA Channel 2 Transfer Request Collision Flag bit
  - 1 = User force and interrupt-based request collision is detected
  - 0 = No request collision is detected
- bit 1      **RQCOL1:** DMA Channel 1 Transfer Request Collision Flag bit
  - 1 = User force and interrupt-based request collision is detected
  - 0 = No request collision is detected
- bit 0      **RQCOL0:** DMA Channel 0 Transfer Request Collision Flag bit
  - 1 = User force and interrupt-based request collision is detected
  - 0 = No request collision is detected

FIGURE 13-3: TYPE B/TIME C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)



## 13.1 Timerx/y Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:  
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

### 13.1.1 KEY RESOURCES

- “Timers” (DS70362) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools



**NOTES:**

**REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)**

bit 4-0 **SYNCSEL<4:0>**: Input Source Select for Synchronization and Trigger Operation bits<sup>(4)</sup>

11111 = No Sync or Trigger source for ICx  
 11110 = Reserved  
 11101 = Reserved  
 11100 = CTMU module synchronizes or triggers ICx  
 11011 = ADC1 module synchronizes or triggers ICx<sup>(5)</sup>  
 11010 = CMP3 module synchronizes or triggers ICx<sup>(5)</sup>  
 11001 = CMP2 module synchronizes or triggers ICx<sup>(5)</sup>  
 11000 = CMP1 module synchronizes or triggers ICx<sup>(5)</sup>  
 10111 = Reserved  
 10110 = Reserved  
 10101 = Reserved  
 10100 = Reserved  
 10011 = IC4 module synchronizes or triggers ICx  
 10010 = IC3 module synchronizes or triggers ICx  
 10001 = IC2 module synchronizes or triggers ICx  
 10000 = IC1 module synchronizes or triggers ICx  
 01111 = Timer5 synchronizes or triggers ICx  
 01110 = Timer4 synchronizes or triggers ICx  
 01101 = Timer3 synchronizes or triggers ICx **(default)**  
 01100 = Timer2 synchronizes or triggers ICx  
 01011 = Timer1 synchronizes or triggers ICx  
 01010 = PTGOx module synchronizes or triggers ICx<sup>(6)</sup>  
 01001 = Reserved  
 01000 = Reserved  
 00111 = Reserved  
 00110 = Reserved  
 00101 = Reserved  
 00100 = OC4 module synchronizes or triggers ICx  
 00011 = OC3 module synchronizes or triggers ICx  
 00010 = OC2 module synchronizes or triggers ICx  
 00001 = OC1 module synchronizes or triggers ICx  
 00000 = No Sync or Trigger source for ICx

- Note 1:** The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.
- 2:** The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
- 3:** This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software.
- 4:** Do not use the ICx module as its own Sync or Trigger source.
- 5:** This option should only be selected as a trigger source and not as a synchronization source.
- 6:** Each Input Capture x (ICx) module has one PTG input source. See **Section 24.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
- PTGO8 = IC1  
 PTGO9 = IC2  
 PTGO10 = IC3  
 PTGO11 = IC4

**REGISTER 17-13: QE11LECH: QE11 LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<23:16>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0      **QEILEC<31:16>**: High Word Used to Form 32-Bit Less Than or Equal Compare Register (QE11LEC) bits

**REGISTER 17-14: QE11LECL: QE11 LESS THAN OR EQUAL COMPARE LOW WORD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEILEC<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0      **QEILEC<15:0>**: Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QE11LEC) bits

## 18.0 SERIAL PERIPHERAL INTERFACE (SPI)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Serial Peripheral Interface (SPI)**” (DS70569) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with Motorola® SPI and SIOP interfaces.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device family offers two SPI modules on a single device. These modules, which are designated as SPI1 and SPI2, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

**Note:** In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of the SPI2 module, but results in a lower maximum speed for SPI2. See **Section 30.0 “Electrical Characteristics”** for more information.

The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- SSx/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, SSx is not used. In 2-pin mode, neither SDOx nor SSx is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

### 18.3 SPIx Control Registers

**REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER**

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
SPIEN	—	SPISIDL	—	—	SPIBEC<2:0>		
bit 15							bit 8

R/W-0	R/C-0, HS	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R-0, HS, HC
SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF
bit 7							bit 0

<b>Legend:</b>	C = Clearable bit	HS = Hardware Settable bit	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **SPIEN:** SPIx Enable bit  
1 = Enables the module and configures SCKx, SDOx, SDIx and  $\overline{SSx}$  as serial port pins  
0 = Disables the module
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SPISIDL:** SPIx Stop in Idle Mode bit  
1 = Discontinues the module operation when device enters Idle mode  
0 = Continues the module operation in Idle mode
- bit 12-11 **Unimplemented:** Read as '0'
- bit 10-8 **SPIBEC<2:0>:** SPIx Buffer Element Count bits (valid in Enhanced Buffer mode)  
Master mode:  
Number of SPIx transfers that are pending.  
Slave mode:  
Number of SPIx transfers that are unread.
- bit 7 **SRMPT:** SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode)  
1 = SPIx Shift register is empty and Ready-To-Send or receive the data  
0 = SPIx Shift register is not empty
- bit 6 **SPIROV:** SPIx Receive Overflow Flag bit  
1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register  
0 = No overflow has occurred
- bit 5 **SRXMPT:** SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode)  
1 = RX FIFO is empty  
0 = RX FIFO is not empty
- bit 4-2 **SISEL<2:0>:** SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)  
111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set)  
110 = Interrupt when last bit is shifted into SPIxSR and as a result, the TX FIFO is empty  
101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete  
100 = Interrupt when one data is shifted into the SPIxSR and as a result, the TX FIFO has one open memory location  
011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set)  
010 = Interrupt when the SPIx receive buffer is 3/4 or more full  
001 = Interrupt when data is available in the receive buffer (SRMPT bit is set)  
000 = Interrupt when the last data in the receive buffer is read and as a result, the buffer is empty (SRXMPT bit is set)

**REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)**

bit 4-2      **SPRE<2:0>**: Secondary Prescale bits (Master mode)<sup>(3)</sup>

111 = Secondary prescale 1:1

110 = Secondary prescale 2:1

•

•

•

000 = Secondary prescale 8:1

bit 1-0      **PPRE<1:0>**: Primary Prescale bits (Master mode)<sup>(3)</sup>

11 = Primary prescale 1:1

10 = Primary prescale 4:1

01 = Primary prescale 16:1

00 = Primary prescale 64:1

- Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
- 2:** This bit must be cleared when FRMEN = 1.
- 3:** Do not set both primary and secondary prescalers to the value of 1:1.

## 22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Charge Time Measurement Unit (CTMU)**” (DS70661) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available on the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Charge Time Measurement Unit is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Four Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edges
- Precise Time Measurement Resolution of 1 ns
- Accurate Current Source Suitable for Capacitive Measurement
- On-Chip Temperature Measurement using a Built-in Diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

## 26.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Programmable Cyclic Redundancy Check (CRC)**” (DS70346) of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

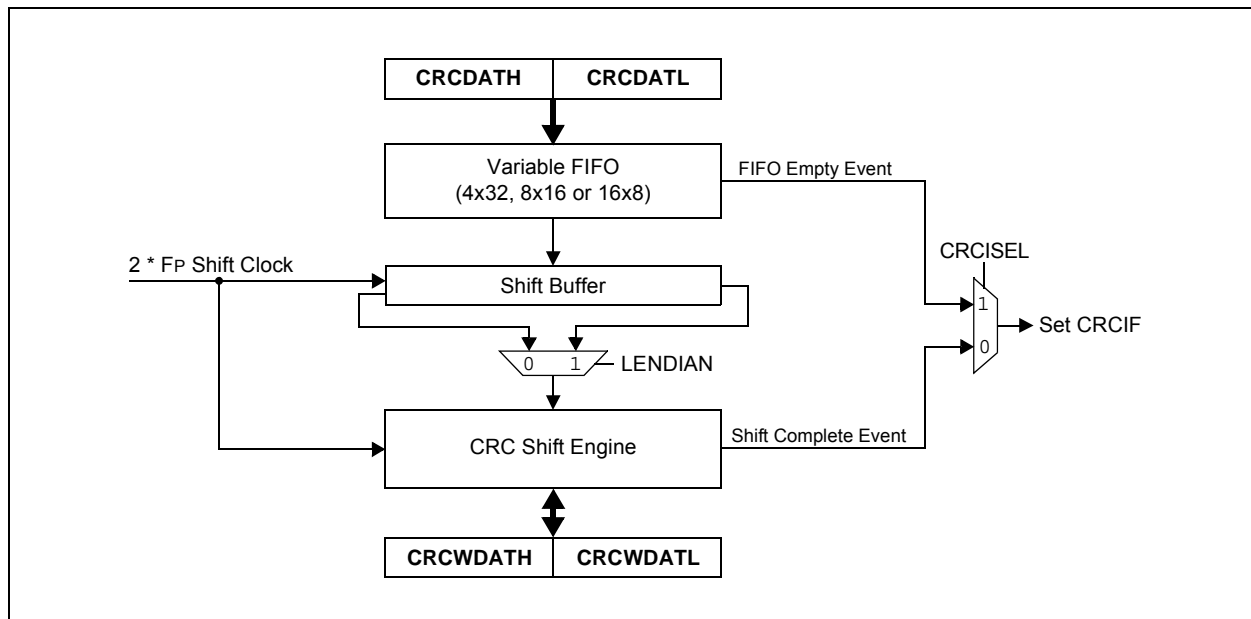
- User-programmable (up to 32nd order) polynomial CRC equation
- Interrupt output
- Data FIFO

The programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 26-1. A simple version of the CRC shift engine is shown in Figure 26-2.

**FIGURE 26-1: CRC BLOCK DIAGRAM**





**TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)**

Bit Field	Description
WDTPRE	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1
WDTWIN<1:0>	Watchdog Window Select bits 11 = WDT window is 25% of WDT period 10 = WDT window is 37.5% of WDT period 01 = WDT window is 50% of WDT period 00 = WDT window is 75% of WDT period
ALTI2C1	Alternate I2C1 pin 1 = I2C1 is mapped to the SDA1/SCL1 pins 0 = I2C1 is mapped to the ASDA1/ASCL1 pins
ALTI2C2	Alternate I2C2 pin 1 = I2C2 is mapped to the SDA2/SCL2 pins 0 = I2C2 is mapped to the ASDA2/ASCL2 pins
JTAGEN <sup>(2)</sup>	JTAG Enable bit 1 = JTAG is enabled 0 = JTAG is disabled
ICS<1:0>	ICD Communication Channel Select bits 11 = Communicate on PGEC1 and PGED1 10 = Communicate on PGEC2 and PGED2 01 = Communicate on PGEC3 and PGED3 00 = Reserved, do not use

**Note 1:** This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**2:** When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles <sup>(2)</sup>	Status Flags Affected
46	MOV	MOV <i>f</i> , <i>Wn</i>	Move <i>f</i> to <i>Wn</i>	1	1	None
		MOV <i>f</i>	Move <i>f</i> to <i>f</i>	1	1	None
		MOV <i>f</i> , WREG	Move <i>f</i> to WREG	1	1	None
		MOV #lit16, <i>Wn</i>	Move 16-bit literal to <i>Wn</i>	1	1	None
		MOV.b #lit8, <i>Wn</i>	Move 8-bit literal to <i>Wn</i>	1	1	None
		MOV <i>Wn</i> , <i>f</i>	Move <i>Wn</i> to <i>f</i>	1	1	None
		MOV <i>Wso</i> , <i>Wdo</i>	Move <i>Ws</i> to <i>Wd</i>	1	1	None
		MOV WREG, <i>f</i>	Move WREG to <i>f</i>	1	1	None
		MOV.D <i>Wns</i> , <i>Wd</i>	Move Double from <i>W(ns):W(ns + 1)</i> to <i>Wd</i>	1	2	None
47	MOVPG	MOVPG #lit10, DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPG #lit9, DSWPAG	Move 9-bit literal to DSWPAG	1	1	None
		MOVPG #lit8, TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPG <i>Ws</i> , DSRPAG	Move <i>Ws</i> <9:0> to DSRPAG	1	1	None
		MOVPG <i>Ws</i> , DSWPAG	Move <i>Ws</i> <8:0> to DSWPAG	1	1	None
		MOVPG <i>Ws</i> , TBLPAG	Move <i>Ws</i> <7:0> to TBLPAG	1	1	None
48	MOVSAC	MOVSAC <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> , AWB <sup>(1)</sup>	Prefetch and store accumulator	1	1	None
49	MPY	MPY <i>Wm</i> * <i>Wn</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> <sup>(1)</sup>	Multiply <i>Wm</i> by <i>Wn</i> to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		MPY <i>Wm</i> * <i>Wm</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> <sup>(1)</sup>	Square <i>Wm</i> to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
50	MPY.N	MPY.N <i>Wm</i> * <i>Wn</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> <sup>(1)</sup>	-(Multiply <i>Wm</i> by <i>Wn</i> ) to Accumulator	1	1	None
51	MSC	MSC <i>Wm</i> * <i>Wm</i> , <i>Acc</i> , <i>Wx</i> , <i>Wxd</i> , <i>Wy</i> , <i>Wyd</i> , AWB <sup>(1)</sup>	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB,SA,SB,SAB

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles <sup>(2)</sup>	Status Flags Affected
72	SL	SL <i>f</i>	<i>f</i> = Left Shift <i>f</i>	1	1	C,N,OV,Z
		SL <i>f</i> , WREG	WREG = Left Shift <i>f</i>	1	1	C,N,OV,Z
		SL <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = Left Shift <i>Ws</i>	1	1	C,N,OV,Z
		SL <i>Wb</i> , <i>Wns</i> , <i>Wnd</i>	<i>Wnd</i> = Left Shift <i>Wb</i> by <i>Wns</i>	1	1	N,Z
		SL <i>Wb</i> , #lit5, <i>Wnd</i>	<i>Wnd</i> = Left Shift <i>Wb</i> by lit5	1	1	N,Z
73	SUB	SUB <i>Acc</i> <sup>(1)</sup>	Subtract Accumulators	1	1	OA,OB,OAB,SA,SB,SAB
		SUB <i>f</i>	<i>f</i> = <i>f</i> – WREG	1	1	C,DC,N,OV,Z
		SUB <i>f</i> , WREG	WREG = <i>f</i> – WREG	1	1	C,DC,N,OV,Z
		SUB #lit10, <i>Wn</i>	<i>Wn</i> = <i>Wn</i> – lit10	1	1	C,DC,N,OV,Z
		SUB <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = <i>Wb</i> – <i>Ws</i>	1	1	C,DC,N,OV,Z
		SUB <i>Wb</i> , #lit5, <i>Wd</i>	<i>Wd</i> = <i>Wb</i> – lit5	1	1	C,DC,N,OV,Z
74	SUBB	SUBB <i>f</i>	<i>f</i> = <i>f</i> – WREG – ( $\overline{C}$ )	1	1	C,DC,N,OV,Z
		SUBB <i>f</i> , WREG	WREG = <i>f</i> – WREG – ( $\overline{C}$ )	1	1	C,DC,N,OV,Z
		SUBB #lit10, <i>Wn</i>	<i>Wn</i> = <i>Wn</i> – lit10 – ( $\overline{C}$ )	1	1	C,DC,N,OV,Z
		SUBB <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = <i>Wb</i> – <i>Ws</i> – ( $\overline{C}$ )	1	1	C,DC,N,OV,Z
		SUBB <i>Wb</i> , #lit5, <i>Wd</i>	<i>Wd</i> = <i>Wb</i> – lit5 – ( $\overline{C}$ )	1	1	C,DC,N,OV,Z
75	SUBR	SUBR <i>f</i>	<i>f</i> = WREG – <i>f</i>	1	1	C,DC,N,OV,Z
		SUBR <i>f</i> , WREG	WREG = WREG – <i>f</i>	1	1	C,DC,N,OV,Z
		SUBR <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = <i>Ws</i> – <i>Wb</i>	1	1	C,DC,N,OV,Z
		SUBR <i>Wb</i> , #lit5, <i>Wd</i>	<i>Wd</i> = lit5 – <i>Wb</i>	1	1	C,DC,N,OV,Z
76	SUBBR	SUBBR <i>f</i>	<i>f</i> = WREG – <i>f</i> – ( $\overline{C}$ )	1	1	C,DC,N,OV,Z
		SUBBR <i>f</i> , WREG	WREG = WREG – <i>f</i> – ( $\overline{C}$ )	1	1	C,DC,N,OV,Z
		SUBBR <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = <i>Ws</i> – <i>Wb</i> – ( $\overline{C}$ )	1	1	C,DC,N,OV,Z
		SUBBR <i>Wb</i> , #lit5, <i>Wd</i>	<i>Wd</i> = lit5 – <i>Wb</i> – ( $\overline{C}$ )	1	1	C,DC,N,OV,Z
77	SWAP	SWAP.b <i>Wn</i>	<i>Wn</i> = nibble swap <i>Wn</i>	1	1	None
		SWAP <i>Wn</i>	<i>Wn</i> = byte swap <i>Wn</i>	1	1	None
78	TBLRDH	TBLRDH <i>Ws</i> , <i>Wd</i>	Read Prog<23:16> to <i>Wd</i> <7:0>	1	5	None
79	TBLRDL	TBLRDL <i>Ws</i> , <i>Wd</i>	Read Prog<15:0> to <i>Wd</i>	1	5	None
80	TBLWTH	TBLWTH <i>Ws</i> , <i>Wd</i>	Write <i>Ws</i> <7:0> to Prog<23:16>	1	2	None
81	TBLWTL	TBLWTL <i>Ws</i> , <i>Wd</i>	Write <i>Ws</i> to Prog<15:0>	1	2	None
82	ULNK	ULNK	Unlink Frame Pointer	1	1	SFA
83	XOR	XOR <i>f</i>	<i>f</i> = <i>f</i> .XOR. WREG	1	1	N,Z
		XOR <i>f</i> , WREG	WREG = <i>f</i> .XOR. WREG	1	1	N,Z
		XOR #lit10, <i>Wn</i>	<i>Wd</i> = lit10 .XOR. <i>Wd</i>	1	1	N,Z
		XOR <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = <i>Wb</i> .XOR. <i>Ws</i>	1	1	N,Z
		XOR <i>Wb</i> , #lit5, <i>Wd</i>	<i>Wd</i> = <i>Wb</i> .XOR. lit5	1	1	N,Z
84	ZE	ZE <i>Ws</i> , <i>Wnd</i>	<i>Wnd</i> = Zero-extend <i>Ws</i>	1	1	C,Z,N

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

**TABLE 30-45: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)  
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	Lesser of FP or 15	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1} \downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1} \uparrow$ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	Tsch2ssH, TscL2ssH	$\overline{SS1} \uparrow$ after SCK1 Edge	1.5 Tcy + 40	—	—	ns	(Note 4)
SP60	TssL2doV	SDO1 Data Output Valid after $\overline{SS1}$ Edge	—	—	50	ns	

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

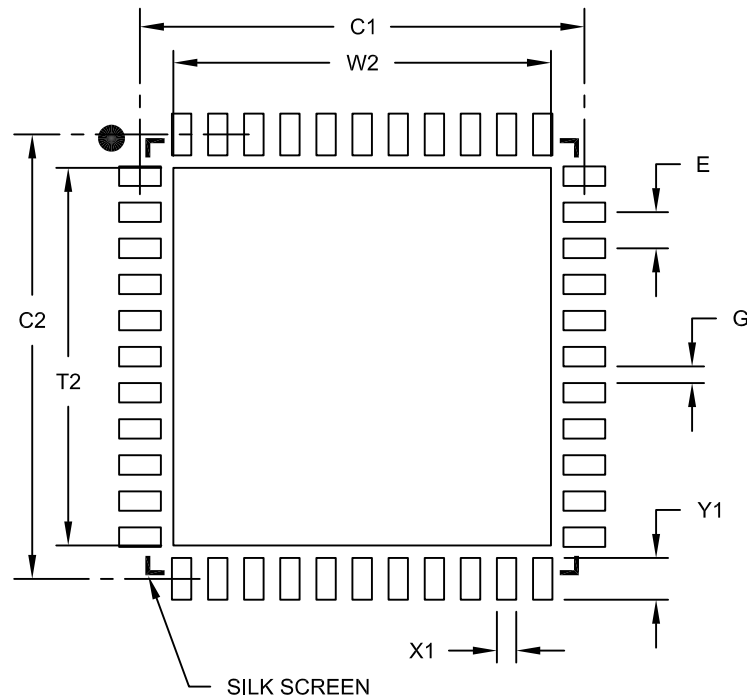
**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



**RECOMMENDED LAND PATTERN**

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (Y44)	Y1			0.85
Distance Between Pads	G	0.25		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B