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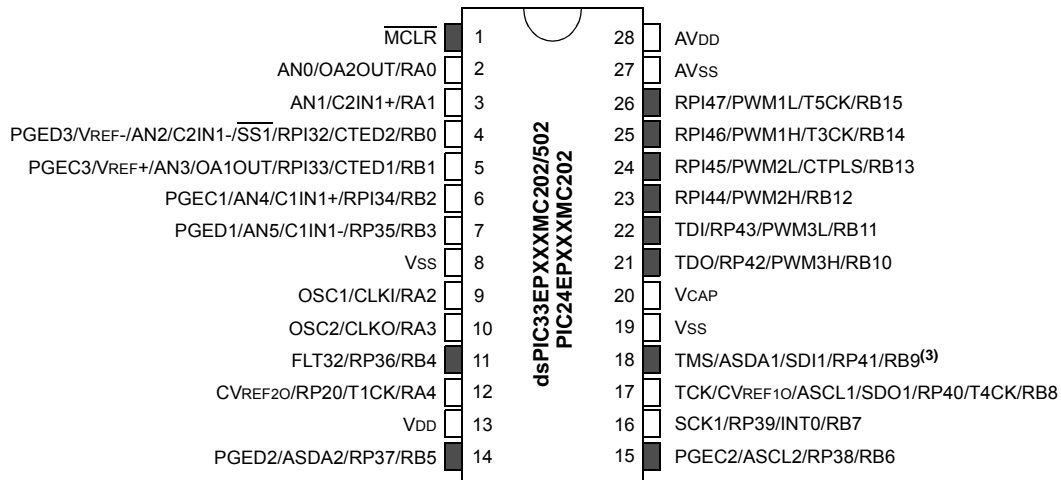
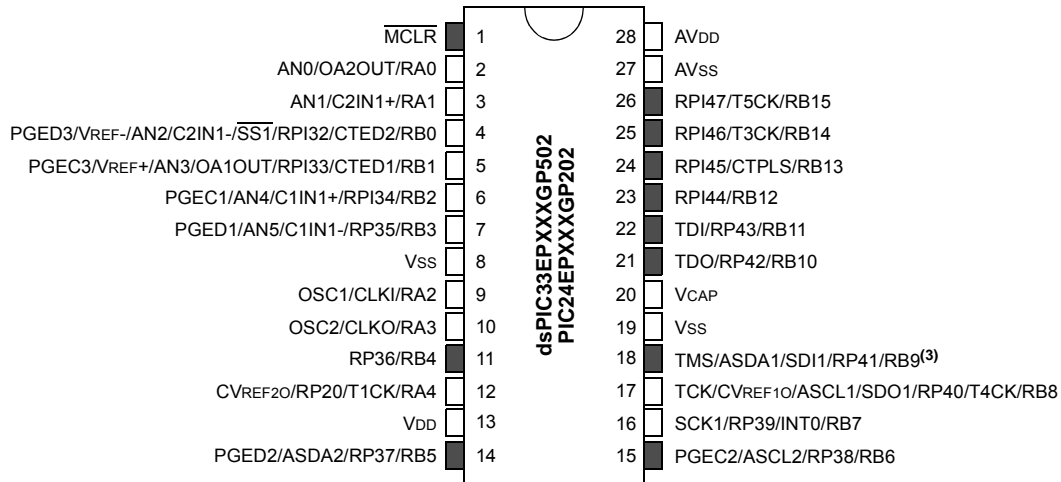
Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512mc202t-e-so

Pin Diagrams

28-Pin SPDIP/SOIC/SSOP^(1,2)

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

- bit 2 **SFA:** Stack Frame Active Status bit
1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space
- bit 1 **RND:** Rounding Mode Select bit⁽¹⁾
1 = Biased (conventional) rounding is enabled
0 = Unbiased (convergent) rounding is enabled
- bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit⁽¹⁾
1 = Integer mode is enabled for DSP multiply
0 = Fractional mode is enabled for DSP multiply

- Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
2: This bit is always read as '0'.
3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	—	—	—	—	—	—	—	—	MI2C2IF	SI2C2IF	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	C1TXIF	—	—	CRCIF	U2EIF	U1EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTIEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	—	—	—	—	—	—	—	—	MI2C2IE	SI2C2IE	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	—	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP<2:0>			—	OC1IP<2:0>			—	IC1IP<2:0>			—	INT0IP<2:0>			4444
IPC1	0842	—	T2IP<2:0>			—	OC2IP<2:0>			—	IC2IP<2:0>			—	DMA0IP<2:0>			4444
IPC2	0844	—	U1RXIP<2:0>			—	SPI1IP<2:0>			—	SPI1EIP<2:0>			—	T3IP<2:0>			4444
IPC3	0846	—	—	—	—	—	DMA1IP<2:0>			—	AD1IP<2:0>			—	U1TXIP<2:0>			0444
IPC4	0848	—	CNIP<2:0>			—	CMIP<2:0>			—	MI2C1IP<2:0>			—	SI2C1IP<2:0>			4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—	INT1IP<2:0>			0004
IPC6	084C	—	T4IP<2:0>			—	OC4IP<2:0>			—	OC3IP<2:0>			—	DMA2IP<2:0>			4444
IPC7	084E	—	U2TXIP<2:0>			—	U2RXIP<2:0>			—	INT2IP<2:0>			—	T5IP<2:0>			4444
IPC8	0850	—	C1IP<2:0>			—	C1RXIP<2:0>			—	SPI2IP<2:0>			—	SPI2EIP<2:0>			4444
IPC9	0852	—	—	—	—	—	IC4IP<2:0>			—	IC3IP<2:0>			—	DMA3IP<2:0>			0444
IPC11	0856	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IPC12	0858	—	—	—	—	—	MI2C2IP<2:0>			—	SI2C2IP<2:0>			—	—	—	—	0440
IPC16	0860	—	CRCIP<2:0>			—	U2EIP<2:0>			—	U1EIP<2:0>			—	—	—	—	4440
IPC17	0862	—	—	—	—	—	C1TXIP<2:0>			—	—	—	—	—	—	—	—	0400
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP<2:0>			—	—	—	—	0040
IPC35	0886	—	JTAGIP<2:0>			—	ICDIP<2:0>			—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP<2:0>			—	PTGWDTIP<2:0>			—	PTGSTIEIP<2:0>			—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP<2:0>			—	PTG2IP<2:0>			—	PTG1IP<2:0>			0444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-41: PMD REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QE1MD	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	—	AD1MD	0000
PMD2	0762	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	—	—	CRCMD	—	—	—	—	—	I2C2MD	—	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	CTMUMD	—	—	0000
PMD6	076A	—	—	—	—	—	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	076C	—	—	—	—	—	—	—	—	—	—	—	DMA0MD	PTGMD	—	—	—	0000
													DMA1MD					
													DMA2MD					
													DMA3MD					

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

NOTES:

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 4	Unimplemented: Read as '0'
bit 3	CF: Clock Fail Detect bit ⁽³⁾ 1 = FSCM has detected clock failure 0 = FSCM has not detected clock failure
bit 2-1	Unimplemented: Read as '0'
bit 0	OSWEN: Oscillator Switch Enable bit 1 = Requests oscillator switch to selection specified by the NOSC<2:0> bits 0 = Oscillator switch is complete

- Note 1:** Writes to this register require an unlock sequence. Refer to “**Oscillator**” (DS70580) in the “*dsPIC33/PIC24 Family Reference Manual*” (available from the Microchip web site) for details.
- 2:** Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.
- 3:** This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Quadrature Encoder Interface (QEI)**” (DS70601) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

- bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I²C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching
- bit 5 **ACKDT:** Acknowledge Data bit (when operating as I²C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge
- bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I²C master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit. Hardware is clear at the end of the master Acknowledge sequence.
0 = Acknowledge sequence is not in progress
- bit 3 **RCEN:** Receive Enable bit (when operating as I²C master)
1 = Enables Receive mode for I²C. Hardware is clear at the end of the eighth bit of the master receive data byte.
0 = Receive sequence is not in progress
- bit 2 **PEN:** Stop Condition Enable bit (when operating as I²C master)
1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of the master Stop sequence.
0 = Stop condition is not in progress
- bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I²C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Repeated Start sequence.
0 = Repeated Start condition is not in progress
- bit 0 **SEN:** Start Condition Enable bit (when operating as I²C master)
1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Start sequence.
0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10
bit 15						bit 8	

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7						bit 0	

Legend:	C = Clearable bit	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I²C™ master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware is set or clear at the end of slave Acknowledge.
- bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
- bit 13-11 **Unimplemented:** Read as '0'
- bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No bus collision detected
Hardware is set at detection of a bus collision.
- bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware is set when address matches general call address. Hardware is clear at Stop detection.
- bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
- bit 7 **IWCOL:** I2Cx Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
- bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register was still holding the previous byte
0 = No overflow
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
- bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.
- bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

21.0 ENHANCED CAN (ECAN™) MODULE (dsPIC33EPXXXGP/ MC50X DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Enhanced Controller Area Network (ECAN™)**” (DS70353) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

21.1 Overview

The Enhanced Controller Area Network (ECAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/protocol was designed to allow communications within noisy environments. The dsPIC33EPXXXGP/MC50X devices contain one ECAN module.

The ECAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details.

The ECAN module features are as follows:

- Implementation of the CAN protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and extended data frames
- 0-8 bytes data length
- Programmable bit rate up to 1 Mbit/sec
- Automatic response to remote transmission requests
- Up to eight transmit buffers with application specified prioritization and abort capability (each buffer can contain up to 8 bytes of data)
- Up to 32 receive buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 full (Standard/Extended Identifier) acceptance filters
- Three full acceptance filter masks
- DeviceNet™ addressing support
- Programmable wake-up functionality with integrated low-pass filter
- Programmable Loopback mode supports self-test operation
- Signaling via interrupt capabilities for all CAN receiver and transmitter error states
- Programmable clock source
- Programmable link to Input Capture (IC2) module for time-stamping and network synchronization
- Low-power Sleep and Idle mode

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

REGISTER 21-3: CxVEC: ECANx INTERRUPT CODE REGISTER

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0
bit 15							bit 8

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
—	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bits

10000-11111 = Reserved

01111 = Filter 15

•
•
•

00001 = Filter 1

00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits

1000101-1111111 = Reserved

1000100 = FIFO almost full interrupt

1000011 = Receiver overflow interrupt

1000010 = Wake-up interrupt

1000001 = Error interrupt

1000000 = No interrupt

•
•
•

0010000-0111111 = Reserved

0001111 = RB15 buffer interrupt

•
•
•

0001001 = RB9 buffer interrupt

0001000 = RB8 buffer interrupt

0000111 = TRB7 buffer interrupt

0000110 = TRB6 buffer interrupt

0000101 = TRB5 buffer interrupt

0000100 = TRB4 buffer interrupt

0000011 = TRB3 buffer interrupt

0000010 = TRB2 buffer interrupt

0000001 = TRB1 buffer interrupt

0000000 = TRB0 buffer interrupt

REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
VCFG2	VCFG1	VCFG0	—	—	CSCNA	CHPS1	CHPS0
bit 15						bit 8	

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7						bit 0	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **VCFG<2:0>:** Converter Voltage Reference Configuration bits

Value	VREFH	VREFL
000	AVDD	Avss
001	External VREF+	Avss
010	AVDD	External VREF-
011	External VREF+	External VREF-
1xx	AVDD	AVSS

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit

1 = Scans inputs for CH0+ during Sample MUXA
 0 = Does not scan inputs

bit 9-8 **CHPS<1:0>:** Channel Select bits

In 12-bit mode (AD21B = 1), the CHPS<1:0> bits are Unimplemented and are Read as '0':

1x = Converts CH0, CH1, CH2 and CH3
 01 = Converts CH0 and CH1
 00 = Converts CH0

bit 7 **BUFS:** Buffer Fill Status bit (only valid when BUFM = 1)

1 = ADC is currently filling the second half of the buffer; the user application should access data in the first half of the buffer
 0 = ADC is currently filling the first half of the buffer; the user application should access data in the second half of the buffer

bit 6-2 **SMPI<4:0>:** Increment Rate bits

When ADDMAEN = 0:

x1111 = Generates interrupt after completion of every 16th sample/conversion operation
 x1110 = Generates interrupt after completion of every 15th sample/conversion operation

•
•
•

x0001 = Generates interrupt after completion of every 2nd sample/conversion operation
 x0000 = Generates interrupt after completion of every sample/conversion operation

When ADDMAEN = 1:

11111 = Increments the DMA address after completion of every 32nd sample/conversion operation
 11110 = Increments the DMA address after completion of every 31st sample/conversion operation

•
•
•

00001 = Increments the DMA address after completion of every 2nd sample/conversion operation
 00000 = Increments the DMA address after completion of every sample/conversion operation

29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

29.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

29.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DI60a	I _{ICL}	Input Low Injection Current	0	—	-5 ^(4,7)	mA	All pins except V _{DD} , V _{SS} , AV _{DD} , AV _{SS} , MCLR, VCAP and RB7
DI60b	I _{ICH}	Input High Injection Current	0	—	+5 ^(5,6,7)	mA	All pins except V _{DD} , V _{SS} , AV _{DD} , AV _{SS} , MCLR, VCAP, RB7 and all 5V tolerant pins ⁽⁶⁾
DI60c	ΣI_{ICT}	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽⁸⁾	—	+20 ⁽⁸⁾	mA	Absolute instantaneous sum of all \pm input injection currents from all I/O pins ($ I_{ICL} + I_{ICH} $) $\leq \Sigma I_{ICT}$

- Note 1:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 2:** Negative current is defined as current sourced by the pin.
- 3:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.
- 4:** V_{IL} source < (V_{SS} – 0.3). Characterized but not tested.
- 5:** Non-5V tolerant pins V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins V_{IH} source > 5.5V. Characterized but not tested.
- 6:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.
- 7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 30-6: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS

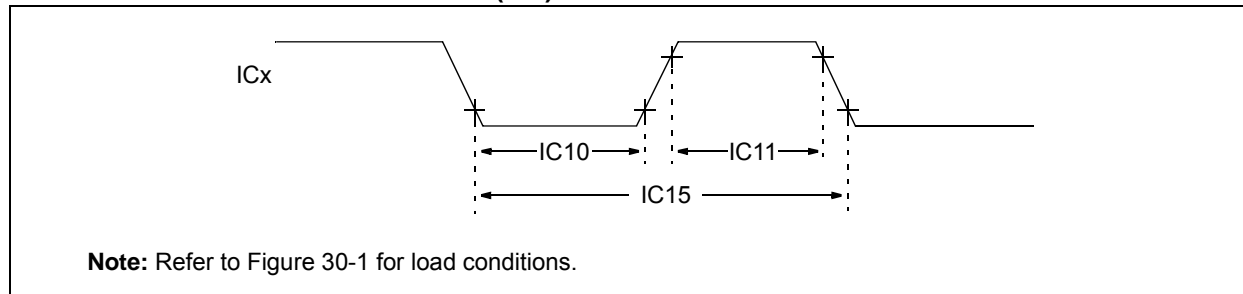


TABLE 30-26: INPUT CAPTURE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Max.	Units	Conditions	
IC10	TccL	ICx Input Low Time	Greater of $12.5 + 25$ or $(0.5 T_{CY}/N) + 25$	—	ns	Must also meet Parameter IC15	N = prescale value (1, 4, 16)
IC11	TccH	ICx Input High Time	Greater of $12.5 + 25$ or $(0.5 T_{CY}/N) + 25$	—	ns	Must also meet Parameter IC15	
IC15	TccP	ICx Input Period	Greater of $25 + 50$ or $(1 T_{CY}/N) + 50$	—	ns		

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE 31-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
HDO10	VOL	Output Low Voltage 4x Sink Driver Pins ⁽²⁾	—	—	0.4	V	$I_{OL} \leq 5 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
		Output Low Voltage 8x Sink Driver Pins ⁽³⁾	—	—	0.4	V	$I_{OL} \leq 8 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
HDO20	VOH	Output High Voltage 4x Source Driver Pins ⁽²⁾	2.4	—	—	V	$I_{OH} \geq -10 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
		Output High Voltage 8x Source Driver Pins ⁽³⁾	2.4	—	—	V	$I_{OH} \geq 15 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
HDO20A	VOH1	Output High Voltage 4x Source Driver Pins ⁽²⁾	1.5	—	—	V	$I_{OH} \geq -3.9 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			2.0	—	—		$I_{OH} \geq -3.7 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			3.0	—	—		$I_{OH} \geq -2 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
		Output High Voltage 8x Source Driver Pins ⁽³⁾	1.5	—	—	V	$I_{OH} \geq -7.5 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			2.0	—	—		$I_{OH} \geq -6.8 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			3.0	—	—		$I_{OH} \geq -3 \text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)

Note 1: Parameters are characterized, but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

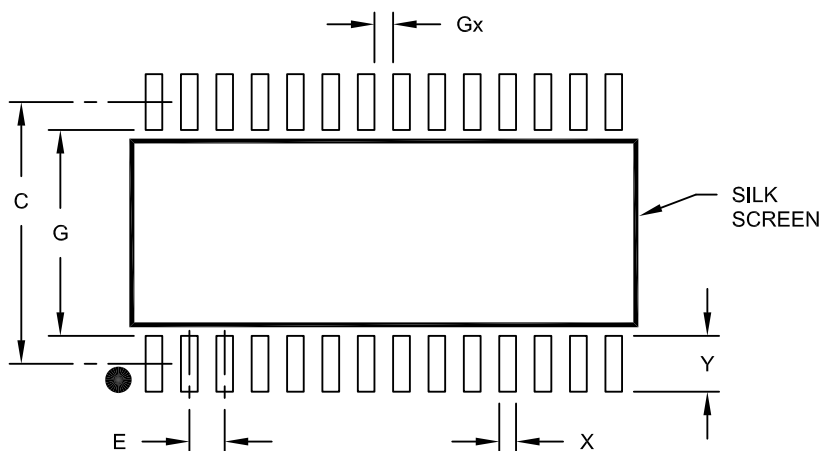
3: Includes the following pins:

For devices with less than 64 pins: RA3, RA4, RA9, RB<15:7> and RC3

For 64-pin devices: RA4, RA9, RB<15:7>, RC3 and RC15

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

APPENDIX A: REVISION HISTORY

Revision A (April 2011)

This is the initial released version of the document.

Revision B (July 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-1.

TABLE A-1: MAJOR SECTION UPDATES

Section Name	Update Description
“High-Performance, 16-bit Digital Signal Controllers and Microcontrollers”	Changed all pin diagrams references of VLAP to TLA.
Section 4.0 “Memory Organization”	Updated the All Resets values for CLKDIV and PLLFBD in the System Control Register Map (see Table 4-35).
Section 5.0 “Flash Program Memory”	Updated “one word” to “two words” in the first paragraph of Section 5.2 “RTSP Operation” .
Section 9.0 “Oscillator Configuration”	<p>Updated the PLL Block Diagram (see Figure 9-2).</p> <p>Updated the Oscillator Mode, Fast RC Oscillator (FRC) with divide-by-N and PLL (FRCPLL), by changing (FRCDIVN + PLL) to (FRCPLL).</p> <p>Changed (FRCDIVN + PLL) to (FRCPLL) for COSC<2:0> = 001 and NOSC<2:0> = 001 in the Oscillator Control Register (see Register 9-1).</p> <p>Changed the POR value from 0 to 1 for the DOZE<1:0> bits, from 1 to 0 for the FRCDIV<0> bit, and from 0 to 1 for the PLLPOST<0> bit; Updated the default definitions for the DOZE<2:0> and FRCDIV<2:0> bits and updated all bit definitions for the PLLPOST<1:0> bits in the Clock Divisor Register (see Register 9-2).</p> <p>Changed the POR value from 0 to 1 for the PLLDIV<5:4> bits and updated the default definitions for all PLLDIV<8:0> bits in the PLL Feedback Division Register (see Register 9-2).</p>
Section 22.0 “Charge Time Measurement Unit (CTMU)”	Updated the bit definitions for the IRNG<1:0> bits in the CTMU Current Control Register (see Register 22-3).
Section 25.0 “Op amp/Comparator Module”	Updated the voltage reference block diagrams (see Figure 25-1 and Figure 25-2).

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