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## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512mc204-i-pt

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TABLE 4	-1:	CPU C	ORE RE	GISTE	R MAP F	OR dsF	PIC33EP	XXXMC	20X/50X	AND d	sPIC33I	EPXXX	GP50X	DEVICE	S ONL	(CON	TINUE	D)
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	С	0000
CORCON	0044	VAR	_	US<	1:0>	EDT		DL<2:0>		SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020
MODCON	0046	XMODEN	YMODEN	_	_		BWM<3:0> YWM<3:0> XWM<3:0>						0000					
XMODSRT	0048	XMODSRT<15:0>								_	0000							
XMODEND	004A	XMODEND<15:0>								_	0001							
YMODSRT	004C							YMC	DSRT<15:0	>								0000
YMODEND	004E							YMC	DEND<15:0	)>								0001
XBREV	0050	BREN							XBF	REV<14:0>								0000
DISICNT	0052	_	_							DISICNT<	13:0>							0000
TBLPAG	0054		_	_	_	_	_	_	_				TBLPA	G<7:0>				0000
MSTRPR	0058	MSTRPR<15:0>								0000								

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0			
GIE	DISI	SWTRAP		_	_	_	—			
bit 15				·			bit 8			
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0			
		_	_	—	INT2EP	INT1EP	INT0EP			
bit 7							bit 0			
Legend:	L:1		L:1			(0)				
R = Readable	DIT	vv = vvritable	DIT		mented bit, read	as '0'				
-n = value at I	POR	"1" = Bit is set		$0^{\circ} = Bit is cle$	eared	x = Bit is unkr	nown			
hit 15		ntorrunt Enable	, hit							
DIL 15		and associate	d IF hits are e	nahled						
	0 = Interrupts	are disabled,	but traps are s	still enabled						
bit 14	DISI: DISI Ir	nstruction Statu	s bit							
	1 = DISI ins	truction is activ	e							
	0 = DISI <b>ins</b> i	truction is not a	ictive							
bit 13	SWTRAP: So	oftware Trap St	atus bit							
	1 = Software	trap is enabled	4							
hit 12-3		ted. Read as '	 							
bit 2	INT2FP: Exte	ernal Interrupt 2	∘ PEdge Detect	Polarity Selec	et bit					
	1 = Interrupt	on negative ed	ae							
	0 = Interrupt	on positive edg	le							
bit 1	INT1EP: Exte	ernal Interrupt ?	Edge Detect	Polarity Selec	ct bit					
	1 = Interrupt on negative edge									
	0 = Interrupt	on positive edg	e							
bit 0	INTOEP: Exte	ernal Interrupt (	) Edge Detect	Polarity Selec	ct bit					
	$\perp$ = interrupt	on negative ed	ye Ie							

## REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

# 12.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

## 12.1.1 KEY RESOURCES

- "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

# REGISTER 16-13: IOCONX: PWMx I/O CONTROL REGISTER<sup>(2)</sup> (CONTINUED)

- bit 1 SWAP: SWAP PWMxH and PWMxL Pins bit
   1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins
   0 = PWMxH and PWMxL pins are mapped to their respective pins
   bit 0 OSYNC: Output Override Synchronization bit
   1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWMx period boundary
  - 0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary
- Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
  - 2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_	
bit 15	1		1		1		bit 8	
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	BCH(")	BCL	BPHH	BPHL	BPLH	BPLL	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown	
bit 15	PHR: PWMxH	Rising Edge	Trigger Enabl	e bit				
	$\perp$ = Rising edg 0 = Leading-E	ge of PyvivixH v Edge Blanking i	anores risina	edge of PWM	anking counter kH			
bit 14	PHF: PWMxH	Falling Edge	Trigger Enabl	e bit				
	1 = Falling ed	ge of PWMxH	will trigger Le	ading-Edge Bla	anking counter			
	0 = Leading-E	Edge Blanking i	gnores falling	g edge of PWM	хH			
bit 13	PLR: PWMxL Rising Edge Trigger Enable bit							
	<ul> <li>1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter</li> <li>0 = Leading-Edge Blanking ignores rising edge of PWMxL</li> </ul>							
bit 12	PLF: PWMxL Falling Edge Trigger Enable bit							
	1 = Falling ed	ge of PWMxL	will trigger Le	ading-Edge Bla	anking counter			
	0 = Leading-Edge Blanking ignores falling edge of PWMxL							
bit 11	1 = Leading-F	-ault Input Lea Edge Blanking i	ding-Edge Bla	anking Enable	bit			
	0 = Leading-E	Edge Blanking i	s not applied	to selected Fa	ult input			
bit 10	CLLEBEN: C	urrent-Limit Le	ading-Edge E	Blanking Enable	e bit			
	1 = Leading-E	Edge Blanking i	s applied to s	selected curren	t-limit input			
hit 0.6	0 = Leading-E	tode Blanking I	s not applied	to selected cul	rrent-limit input			
bit 5	BCH Blankin	a in Selected F	J Blanking Sign	al High Enable	hit(1)			
bit 5	1 = State blan	kina (of curren	t-limit and/or	Fault input sigr	nals) when seled	ted blanking s	ianal is hiah	
	0 = No blankii	ng when select	ed blanking s	signal is high	,	5	0 0	
bit 4	BCL: Blanking	g in Selected B	lanking Signa	al Low Enable I	bit <sup>(1)</sup>			
	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when seled	cted blanking s	ignal is low	
bit 3	BPHH: Blanki	ing in PWMxH	High Enable	hit				
bit o	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when PWN	/IxH output is h	igh	
	0 <b>= No blanki</b>	ng when PWM	xH output is h	nigh			-	
bit 2	BPHL: Blanki	ng in PWMxH	Low Enable b	pit				
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xH output is le	Fault input sigr ow	nals) when PWN	IxH output is lo	W	
bit 1	BPLH: Blanki	ng in PWMxL I	High Enable b	oit				
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xL output is h	Fault input sigr igh	nals) when PWN	/IxL output is hi	igh	
bit 0	BPLL: Blanki	ng in PWMxL L	ow Enable b	it				
	1 = State blan	king (of curren	t-limit and/or	Fault input sigr	nals) when PWN	IxL output is lo	W	
	v = i N o diankii		x∟ output is io	JVV				

# REGISTER 16-16: LEBCONX: PWMx LEADING-EDGE BLANKING CONTROL REGISTER

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

# REGISTER 17-17: INT1TMRH: INTERVAL 1 TIMER HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	INTTMR<31:24>								
bit 15	it 15 bit 8								
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	INTTMR<23:16>								
bit 7							bit 0		
Legend:									
R = Readable bit W = Writable bit U = Unimplemented bit				nented bit, read	d as '0'				
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unkn				nown					

bit 15-0 INTTMR<31:16>: High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

# REGISTER 17-18: INT1TMRL: INTERVAL 1 TIMER LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
			INTTM	1R<15:8>					
bit 15	it 15 bit 8								
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	INTTMR<7:0>								
bit 7							bit 0		
Legend:									
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'						
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unkn				nown					

bit 15-0 INTTMR<15:0>: Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 21-26:	CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER	
	(m = 0,2,4,6; n = 1,3,5,7)	

R/W-0	) R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0		
TXEN	n TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0		
bit 15							bit 8		
R/W-0	) R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0		
TXENr	m TXABTm <sup>(1)</sup>	TXLARBm <sup>(1)</sup>	TXERRm <sup>(1)</sup>	TXREQm	RTRENm	TXmPRI1	TXmPRI0		
bit 7							bit 0		
r									
Legend:									
R = Read	able bit	W = Writable	bit	U = Unimplei	mented bit, read	d as '0'			
-n = Value	e at POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown		
bit 15-8	See Definition	n for bits<7:0>,	Controls Buffe	er n					
bit 7	TXENm: TX/	RX Buffer Sele	ction bit						
	1 = Buffer TR	1 = Buffer TRBn is a transmit buffer							
		0 = Buffer I RBn is a receive buffer							
bit 6	TXABTm: Me	TXABTm: Message Aborted bit'							
	1 = Message	was aborted	nemission succ	ressfully					
hit 5			whitration hit(1)	)					
bit o	1 = Message	lost arbitration	while being se	nt					
	0 = Message	did not lose ar	bitration while	being sent					
bit 4	TXERRm: Er	ror Detected D	uring Transmis	ssion bit <sup>(1)</sup>					
	1 = A bus err	or occurred wh	ile the messag	je was being s	sent				
	0 = A bus error	or did not occu	r while the me	ssage was be	ing sent				
bit 3	TXREQm: Me	essage Send R	equest bit						
	1 = Requests	s that a messag	ge be sent; the	bit automatic	ally clears wher	n the message i	s successfully		
	o = Clearing	the hit to '0' wh	nile set reques	ts a messarie	abort				
hit 2		ito-Remote Tra	ine set reques	hit	abort				
511 2	1 = When a result of the second sec	emote transmit	is received T	XRFQ will be	set				
	0 = When a r	emote transmit	is received, T	XREQ will be	unaffected				
bit 1-0	TXmPRI<1:0	>: Message Tra	ansmission Pri	iority bits					
	11 = Highest	11 = Highest message priority							
	10 = High inte	ermediate mes	sage priority						
	01 = Low interview	01 = Low Intermediate message priority							
		messaye priori	Ly						
Note 1:	This bit is cleared	when TXREQ i	s set.						

Note: The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

# BUFFER 21-7: ECAN™ MESSAGE BUFFER WORD 6

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
			By	te 7					
bit 15							bit 8		
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
	Byte 6								
bit 7							bit 0		
Legend:									
R = Readable bit W = Writable bit			oit	U = Unimplemented bit, read as '0'					
-n = Value at POR '1' = Bit is set				'0' = Bit is clea	ared	x = Bit is unkr	nown		

bit 15-8 Byte 7<15:8>: ECAN Message Byte 7 bits

bit 7-0 Byte 6<7:0>: ECAN Message Byte 6 bits

# BUFFER 21-8: ECAN<sup>™</sup> MESSAGE BUFFER WORD 7

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	_	FILHIT4 <sup>(1)</sup>	FILHIT3 <sup>(1)</sup>	FILHIT2 <sup>(1)</sup>	FILHIT1 <sup>(1)</sup>	FILHITO <sup>(1)</sup>
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—	_	—	_	_	—	—
bit 7							bit 0
Leaend:							

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12-8	FILHIT<4:0>: Filter Hit Code bits <sup>(1)</sup>
	Encodes number of filter that resulted in writing this buffer.
bit 7-0	Unimplemented: Read as '0'

Note 1: Only written by module for receive buffers, unused for transmit buffers.

# 25.3 Op Amp/Comparator Registers

R/W-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
PSIDL				C4EVT <sup>(1)</sup>	C3EVT <sup>(1)</sup>	C2EVT <sup>(1)</sup>	C1EVT <sup>(1)</sup>
bit 15	1			1			bit 8
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
		—		C4OUT <sup>(2)</sup>	C3OUT <sup>(2)</sup>	C2OUT <sup>(2)</sup>	C1OUT <sup>(2)</sup>
bit 7							bit 0
r							
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		0' = Bit is cle	ared	x = Bit is unkn	iown
hit 15		arator Stop in	dla Mada hit				
DIL 15	1 = Discontinu	ues operation of	of all comparat	ors when devi	ce enters Idle n	node	
	0 = Continues	s operation of a	Il comparators	s in Idle mode		1000	
bit 14-12	Unimplement	ted: Read as '	)'				
bit 11	C4EVT: Op A	mp/Comparato	r 4 Event Stat	us bit <sup>(1)</sup>			
	1 = Op amp/c	omparator eve	nt occurred				
L:1 40	0 = Op amp/comparator event did not occur						
DIT 10	1 = Comparat	corator 3 Even	Status Dit				
	0 = Comparat	or event did no	ot occur				
bit 9	C2EVT: Comp	parator 2 Event	: Status bit <sup>(1)</sup>				
	1 = Comparat	or event occur	red				
	0 = Comparat	or event did no	ot occur				
bit 8	C1EVT: Comp	parator 1 Event	Status bit <sup>(1)</sup>				
	1 = Comparat	or event occur	red of occur				
bit 7-4	Unimplement	ted: Read as '	)'				
bit 3	C4OUT: Com	parator 4 Outp	ut Status bit <sup>(2)</sup>				
	When CPOL =	= 0:					
	1 = VIN + > VIN	N-					
	0 = VIN + < VIN	N- - 1·					
	1 = VIN + < VIN	<u></u> N-					
	0 = VIN + > VIN	N-					
bit 2	C3OUT: Com	parator 3 Outp	ut Status bit <sup>(2)</sup>				
	When CPOL = $1 = 1$	<u>= 0:</u>					
	1 = VIN + > VIN $0 = VIN + < VIN$	N- N-					
	When CPOL =	<b>=</b> 1:					
	1 = VIN + < VIN	N-					
	$\cup = VIN + > VIN$	N-					

#### REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

- **Note 1:** Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.
  - 2: Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON<8>.

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		—	DWIDTH4	DWIDTH3	DWIDTH2	DWIDTH1	DWIDTH0
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		—	PLEN4	PLEN3	PLEN2	PLEN1	PLEN0
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown
bit 15-13	Unimplemen	ted: Read as '	0'				
bit 12-8	DWIDTH<4:0	>: Data Width	Select bits				
	These bits se	t the width of th	ne data word (	DWIDTH<4:0>	· + 1).		
bit 7-5	Unimplemen	ted: Read as '	0'				

# REGISTER 26-2: CRCCON2: CRC CONTROL REGISTER 2

bit 4-0 **PLEN<4:0>:** Polynomial Length Select bits

These bits set the length of the polynomial (Polynomial Length = PLEN<4:0> + 1).

# 27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

TABLE 27-3: USER ID WORDS REGISTER MAP

File Name	Address	Bits 23-16	Bits 15-0
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	_	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

**Legend:** — = unimplemented, read as '1'.

# 27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an onchip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

#### FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE

REGULATOR<sup>(1,2,3)</sup>



# 27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles <sup>(2)</sup>	Status Flags Affected
52	MUL	MUL.SS	Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS	Wb,Ws,Acc <sup>(1)</sup>	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU	Wb,Ws,Acc <sup>(1)</sup>	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU	Wb,#lit5,Acc <sup>(1)</sup>	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US	Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US	Wb,Ws,Acc <sup>(1)</sup>	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU	Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU	Wb,#lit5,Acc <sup>(1)</sup>	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU	Wb,Ws,Acc <sup>(1)</sup>	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS	Wb,Ws,Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU	Wb,Ws,Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US	Wb,Ws,Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU	Wb,Ws,Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU	Wb,#lit5,Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
1		MUL.UU	Wb,#lit5,Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL	f	W3:W2 = f * WREG	1	1	None

# TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

# FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS



# TABLE 30-27: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS		$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Тур.	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—			ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

# FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS



## TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Тур.	Max.	Units	Conditions
OC15	TFD	Fault Input to PWMx I/O Change	—	_	Tcy + 20	ns	
OC20	TFLT	Fault Input Pulse Width	Tcy + 20	_	—	ns	

**Note 1:** These parameters are characterized but not tested in manufacturing.



# FIGURE 30-20: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



# FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

# 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Microchip Technology Drawing C04-052C Sheet 1 of 2

# 28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-124C Sheet 1 of 2

# Revision H (August 2013)

This revision includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-6.

TABLE A-6:	MAJOR SECTION UPDATES
------------	-----------------------

Section Name	Update Description
Cover Section	Adds Peripheral Pin Select (PPS) to allow Digital Function Remapping and Change
	Notification Interrupts to Input/Output section
	Adds heading information to 64-Pin TQFP
Section 4.0 "Memory	Corrects Reset values for ANSELE, TRISF, TRISC, ANSELC and TRISA
Organization"	Corrects address range from 0x2FFF to 0x7FFF
	<ul> <li>Corrects DSRPAG and DSWPAG (now 3 hex digits)</li> </ul>
	<ul> <li>Changes Call Stack Frame from &lt;15:1&gt; to PC&lt;15:0&gt;</li> </ul>
	Word length in Figure 4-20 is changed to 50 words for clarity
Section 5.0 "Flash Program Memory"	Corrects descriptions of NVM registers
Section 9.0 "Oscillator	Removes resistor from Figure 9-1
Configuration"	Adds Fast RC Oscillator with Divide-by-16 (FRCDIV16) row to Table 9-1
	Removes incorrect information from ROI bit in Register 9-2
Section 14.0 "Input Capture"	Changes 31 user-selectable Trigger/Sync interrupts to 19 user-selectable Trigger/ Sync interrupts
	Corrects ICTSEL<12:10> bits (now ICTSEL<2:0>)
Section 17.0 "Quadrature Encoder Interface (QEI)	Corrects QCAPEN bit description
Module	
(dsPIC33EPXXXMC20X/50X	
Devices Only)"	
Section 19.0 "Inter-	Adds note to clarify that 100kbit/sec operation of I <sup>2</sup> C is not possible at high processor
Integrated Circuit™ (I <sup>2</sup> C™)"	speeds
Section 22.0 "Charge Time Measurement Unit (CTMU)"	Clarifies Figure 22-1 to accurately reflect peripheral behavior
Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)"	Correct Figure 23-1 (changes CH123x to CH123Sx)
Section 24.0 "Peripheral Trigger Generator (PTG) Module"	<ul> <li>Adds footnote to Register 24-1 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled.</li> </ul>
Section 25.0 "Op Amp/ Comparator Module"	• Adds note to Figure 25-3 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled)
	<ul> <li>Adds footnote to Register 25-2 (COE is not available when OPMODE (CMxCON&lt;10&gt;) = 1)</li> </ul>
Section 27.0 "Special Features"	Corrects the bit description for FNOSC<2:0>
Section 30.0 "Electrical	Corrects 512K part power-down currents based on test data
Characteristics"	Corrects WDT timing limits based on LPRC oscillator tolerance
Section 31.0 "High-	Adds Table 31-5 (DC Characteristics: Idle Current (IIDLE)
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