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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
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### 4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Program Memory" (DS70613) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

#### 4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in Section 4.8 "Interfacing Program and Data Memory Spaces".

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-5.

# FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X AND PIC24EP32GP/MC20X DEVICES



#### 4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in wordaddressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-6).

Program memory addresses are always word-aligned on the lower word and addresses are incremented, or decremented by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

### 4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices reserve the addresses between 0x000000 and 0x000200 for hardcoded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 7.1** "Interrupt Vector Table".



#### FIGURE 4-6: PROGRAM MEMORY ORGANIZATION





TABLE 4	-1:	CPU C	ORE RE	GISTE	R MAP F	OR dsF	PIC33EP	XXXMC	20X/50X	AND d	sPIC33I	EPXXX	GP50X	DEVICE	S ONL	(CON	TINUE	D)
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	С	0000
CORCON	0044	VAR	_	US<	1:0>	EDT DL<2:0>			SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020	
MODCON	0046	XMODEN	YMODEN	_	- BWM<3:0> YWM<3:0> XWM<3:0>								0000					
XMODSRT	0048		XMODSRT<15:0>									_	0000					
XMODEND	004A		XMODEND<15:0>									_	0001					
YMODSRT	004C							YMC	DSRT<15:0	>								0000
YMODEND	004E							YMC	DEND<15:0	)>								0001
XBREV	0050	BREN							XBF	REV<14:0>								0000
DISICNT	0052	_	_							DISICNT<	13:0>							0000
TBLPAG	0054		_	_	_	_	_	_	_				TBLPA	G<7:0>				0000
MSTRPR	0058								MSTRPR<	:15:0>								0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0
I a manuali							

#### REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 Unimplemented: Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits 011111 = Maximum frequency deviation of 1.453% (7.477 MHz) 011110 = Center frequency + 1.406% (7.474 MHz) •••• 000001 = Center frequency + 0.047% (7.373 MHz) 000000 = Center frequency (7.37 MHz nominal) 111111 = Center frequency - 0.047% (7.367 MHz) ••• 100001 = Center frequency - 1.453% (7.263 MHz) 100000 = Minimum frequency deviation of -1.5% (7.259 MHz)

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss	010 1101	I	RPI45
000 0001	I	C1OUT <sup>(1)</sup>	010 1110	I	RPI46
000 0010	I	C2OUT <sup>(1)</sup>	010 1111	I	RPI47
000 0011	I	C3OUT <sup>(1)</sup>	011 0000	_	_
000 0100	I	C4OUT <sup>(1)</sup>	011 0001		—
000 0101	_	_	011 0010		_
000 0110	I	PTGO30 <sup>(1)</sup>	011 0011	I	RPI51
000 0111	I	PTGO31 <sup>(1)</sup>	011 0100	I	RPI52
000 1000	I	FINDX1 <sup>(1,2)</sup>	011 0101	I	RPI53
000 1001	I	FHOME1 <sup>(1,2)</sup>	011 0110	I/O	RP54
000 1010	—	—	011 0111	I/O	RP55
000 1011	_	—	011 1000	I/O	RP56
000 1100	_	—	011 1001	I/O	RP57
000 1101		—	011 1010	I	RPI58
000 1110	_	—	011 1011	—	—
000 1111	_	—	011 1100	_	—
001 0000		—	011 1101		—
001 0001		_	011 1110	_	_
001 0010		_	011 1111	—	_
001 0011		—	100 0000		—
001 0100	I/O	RP20	100 0001	_	—
001 0101	_	—	100 0010	_	—
001 0110	—	—	100 0011	—	_
001 0111	—	—	100 0100	_	—
001 1000	I	RPI24	100 0101	—	—
001 1001	I	RPI25	100 0110	—	—
001 1010			100 0111		—
001 1011	I	RPI27	100 1000	_	—
001 1100	I	RPI28	100 1001	—	—
001 1101	—	—	100 1010	_	—
001 1110	_	—	100 1011	_	—
001 1111	—	—	100 1100	—	—
010 0000	I	RPI32	100 1101		—
010 0001	I	RPI33	100 1110	_	—
010 0010	I	RPI34	100 1111	—	—
010 0011	I/O	RP35	101 0000		
010 0100	I/O	RP36	101 0001	_	_
010 0101	I/O	RP37	101 0010	—	—
010 0110	I/O	RP38	101 0011		—
010 0111	I/O	RP39	101 0100	_	—

#### TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Legend: Shaded rows indicate PPS Input register values that are unimplemented.

Note 1: See Section 11.4.4.1 "Virtual Connections" for more information on selecting this pin assignment.

2: These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

NOTES:

## 15.0 OUTPUT COMPARE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual" for OCxR and OCxRS register restrictions.





## REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3	S: Start bit
	1 = Indicates that a Start (or Repeated Start) bit has been detected last
	0 = Start bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.
bit 2	<b>R_W:</b> Read/Write Information bit (when operating as I <sup>2</sup> C slave)
	1 = Read – Indicates data transfer is output from the slave
	0 = Write – Indicates data transfer is input to the slave
	Hardware is set or clear after reception of an I <sup>2</sup> C device address byte.
bit 1	RBF: Receive Buffer Full Status bit
	1 = Receive is complete, I2CxRCV is full
	0 = Receive is not complete, I2CxRCV is empty
	Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads
	I2CxRCV.
bit 0	TBF: Transmit Buffer Full Status bit
	1 = Transmit in progress, I2CxTRN is full
	0 = Transmit is complete, I2CxTRN is empty
	Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of a data transmission.

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	—	ТХВО	TXBP	RXBP	TXWAR	RXWAR	EWARN
bit 15							bit 8
R/C-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0
IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF
bit 7							bit 0
Legend: C = Writable bit, but only '0' can be written to clear the bit							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							

'0' = Bit is cleared

x = Bit is unknown

#### REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER

'1' = Bit is set

bit 15-14	Unimplemented: Read as '0'
bit 13	TXBO: Transmitter in Error State Bus Off bit
	1 = Transmitter is in Bus Off state
	0 = Transmitter is not in Bus Off state
bit 12	<b>TXBP:</b> Transmitter in Error State Bus Passive bit
	1 = Transmitter is in Bus Passive state
	0 = Transmitter is not in Bus Passive state
bit 11	<b>RXBP:</b> Receiver in Error State Bus Passive bit
	1 = Receiver is in Bus Passive state
	0 = Receiver is not in Bus Passive state
bit 10	TXWAR: Transmitter in Error State Warning bit
	1 = Transmitter is in Error Warning state
	0 = Transmitter is not in Error warning state
bit 9	RXWAR: Receiver in Error State Warning bit
	1 = Receiver is in Error Warning state
<b>h</b> # 0	0 = Receiver is not in Error warning state
DIL 8	EWARN: Transmitter or Receiver in Error State Warning bit
	$\perp$ = Transmitter or receiver is in Error Warning state 0 = Transmitter or receiver is not in Error Warning state
bit 7	IVRIE: Invalid Message Interrupt Elag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 6	WAKIF: Bus Wake-up Activity Interrupt Flag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 5	ERRIF: Error Interrupt Flag bit (multiple sources in CxINTF<13:8>)
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 4	Unimplemented: Read as '0'
bit 3	FIFOIF: FIFO Almost Full Interrupt Flag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred
bit 2	RBOVIF: RX Buffer Overflow Interrupt Flag bit
	1 = Interrupt request has occurred
	0 = Interrupt request has not occurred

-n = Value at POR

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1			
bit 15				·	- -	·	bit 8			
U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
_	—	—	RB0	DLC3	DLC2	DLC1	DLC0			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'						
-n = Value at POR '1' = Bit is set				'0' = Bit is cle	eared	x = Bit is unk	nown			
bit 15-10	EID<5:0>: E>	ktended Identifi	er bits							
bit 9	RTR: Remote	e Transmission	Request bit							
	When IDE =	<u>1:</u>								
	1 = Message	will request re	mote transmis	sion						
		lessage								
	<u>VVnen IDE = (</u> The RTR bit i	<u>0:</u> is ignored								
hit 9	<b>BB1</b> : Boson									
DILO	Llear must so	t this hit to '0'	oor CAN proto							
DIT 7-5	Unimplemen	ted: Read as	0							
bit 4	<b>RB0:</b> Reserve	ed Bit 0	<b></b>							
	User must se	t this bit to '0' p	per CAN proto	COI.						

#### BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2

bit 3-0 DLC<3:0>: Data Length Code bits

#### BUFFER 21-4: ECAN<sup>™</sup> MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
			B	/te 1				
bit 15							bit 8	
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
			B	/te 0				
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'		
-n = Value at POR '1' = Bit is se		'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknown		

bit 15-8 Byte 1<15:8>: ECAN Message Byte 1 bits

bit 7-0 Byte 0<7:0>: ECAN Message Byte 0 bits

#### BUFFER 21-5: ECAN™ MESSAGE BUFFER WORD 4

R = Readable bit $W$ = Writable bit $(1)^2 = R^2 + R^2$			it	U = Unimplen	nented bit, read ared	1 as '0' x = Bit is unkr	
Legend:							
bit 7							bit 0
			Ву	rte 2			
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
bit 15							bit 8
			Ву	rte 3			
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

bit 15-8 Byte 3<15:8>: ECAN Message Byte 3 bits

bit 7-0 Byte 2<7:0>: ECAN Message Byte 2 bits

#### BUFFER 21-6: ECAN™ MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
			Ву	/te 5					
bit 15							bit 8		
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x		
			Ву	/te 4					
bit 7							bit 0		
Legend:									
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'					
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x =			x = Bit is unkr	nown					
-									

bit 15-8 Byte 5<15:8>: ECAN Message Byte 5 bits

bit 7-0 Byte 4<7:0>: ECAN Message Byte 4 bits

## 23.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

- **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. То complement the information in this data sheet. refer to "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have one ADC module. The ADC module supports up to 16 analog input channels.

On ADC1, the AD12B bit (AD1CON1<10>) allows the ADC module to be configured by the user as either a 10-bit, 4 Sample-and-Hold (S&H) ADC (default configuration) or a 12-bit, 1 S&H ADC.

Note: The ADC module needs to be disabled before modifying the AD12B bit.

### 23.1 Key Features

#### 23.1.1 10-BIT ADC CONFIGURATION

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- · Conversion speeds of up to 1.1 Msps
- · Up to 16 analog input pins
- Connections to three internal op amps
- Connections to the Charge Time Measurement Unit (CTMU) and temperature measurement diode
- Channel selection and triggering can be controlled by the Peripheral Trigger Generator (PTG)
- External voltage reference input pins
- · Simultaneous sampling of:
  - Up to four analog input pins
  - Three op amp outputs
  - Combinations of analog inputs and op amp outputs
- Automatic Channel Scan mode
- Selectable conversion Trigger source
- · Selectable Buffer Fill modes
- Four result alignment options (signed/unsigned, fractional/integer)
- Operation during CPU Sleep and Idle modes

#### 23.1.2 12-BIT ADC CONFIGURATION

The 12-bit ADC configuration supports all the features listed above, with the exception of the following:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one S&H amplifier in the 12-bit configuration; therefore, simultaneous sampling of multiple channels is not supported.

Depending on the particular device pinout, the ADC can have up to 16 analog input pins, designated AN0 through AN15. These analog inputs are shared with op amp inputs and outputs, comparator inputs, and external voltage references. When op amp/comparator functionality is enabled, or an external voltage reference is used, the analog input that shares that pin is no longer available. The actual number of analog input pins, op amps and external voltage reference input configuration depends on the specific device.

A block diagram of the ADC module is shown in Figure 23-1. Figure 23-2 provides a diagram of the ADC conversion clock period.

#### REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)

- PTGITM<1:0>: PTG Input Trigger Command Operating Mode bits<sup>(1)</sup>
  - 11 = Single level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
  - 10 = Single level detect with Step delay executed on exit of command
  - 01 = Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
  - 00 = Continuous edge detect with Step delay executed on exit of command
- Note 1: These bits apply to the PTGWHI and PTGWLO commands only.

bit 1-0

- **2:** This bit is only used with the PTGCTRL step command software trigger option.
- **3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

#### REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3) (CONTINUED)

bit 7-6	EVPOL<1:0>: Trigger/Event/Interrupt Polarity Select bits
	<ul> <li>11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)</li> <li>10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)</li> </ul>
	If CPOL = 1 (inverted polarity): Low-to-high transition of the comparator output.
	If CPOL = 0 (non-inverted polarity): High-to-low transition of the comparator output.
	01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity-selected comparator output (while CEVT = 0)
	If CPOL = 1 (inverted polarity): High-to-low transition of the comparator output.
	If CPOL = 0 (non-inverted polarity): Low-to-high transition of the comparator output
	00 = Trigger/event/interrupt generation is disabled
bit 5	Unimplemented: Read as '0'
bit 4	<b>CREF:</b> Comparator Reference Select bit (VIN+ input) <sup>(1)</sup>
	<ul> <li>1 = VIN+ input connects to internal CVREFIN voltage<sup>(2)</sup></li> <li>0 = VIN+ input connects to CxIN1+ pin</li> </ul>
bit 3-2	Unimplemented: Read as '0'
bit 1-0	CCH<1:0>: Op Amp/Comparator Channel Select bits <sup>(1)</sup>
	<ul> <li>11 = Unimplemented</li> <li>10 = Unimplemented</li> <li>01 = Inverting input of the comparator connects to the CxIN2- pin<sup>(2)</sup></li> <li>00 = Inverting input of the op amp/comparator connects to the CxIN1- pin</li> </ul>

- **Note 1:** Inputs that are selected and not available will be tied to Vss. See the "**Pin Diagrams**" section for available inputs for each package.
  - 2: This output is not available when OPMODE (CMxCON<10>) = 1.

Base Instr #	Assembly Mnemonic	Assembly Syntax Description		# of Words	# of Cycles <sup>(2)</sup>	Status Flags Affected	
1	ADD	ADD	Acc <sup>(1)</sup>	Add Accumulators	1	1	OA,OB,SA,SB
		ADD	f f = f + WREG		1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (4)	None
		BRA	GE, Expr	Branch if greater than or equal	1	1 (4)	None
		BRA	GEU, Expr	Branch if unsigned greater than or equal	1	1 (4)	None
		BRA	GT, Expr	Branch if greater than	1	1 (4)	None
		BRA	GTU, Expr	Branch if unsigned greater than	1	1 (4)	None
		BRA	LE, Expr	Branch if less than or equal	1	1 (4)	None
		BRA	LEU, Expr	Branch if unsigned less than or equal	1	1 (4)	None
		BRA	LT,Expr	Branch if less than		1 (4)	None
		BRA	BRA LTU, Expr Branch if unsigned less than		1	1 (4)	None
		BRA N, Expr Branch if Negative		1	1 (4)	None	
		BRA	NC, Expr	Branch if Not Carry	1	1 (4)	None
		BRA	NN, Expr	Branch if Not Negative	1	1 (4)	None
		BRA	NOV, Expr	Branch if Not Overflow	1	1 (4)	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (4)	None
		BRA	OA, Expr(1)	Branch if Accumulator A overflow	1	1 (4)	None
		BRA	OB, Expr(1)	Branch if Accumulator B overflow	1	1 (4)	None
		BRA	OV, Expr(1)	Branch if Overflow	1	1 (4)	None
		BRA	SA, Expr(1)	Branch if Accumulator A saturated	1	1 (4)	None
		BRA	SB, Expr <sup>(1)</sup>	Branch if Accumulator B saturated	1	1 (4)	None
		BRA	Expr	Branch Unconditionally		4	None
		BRA	Z,Expr	Branch if Zero		1 (4)	None
L		BRA	Wn	Computed Branch	1	4	None
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None
		BSET	Ws,#bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	None
		BSW.Z	Ws,Wb	Write Z bit to Ws <wb></wb>	1	1	None

#### TABLE 28-2: INSTRUCTION SET OVERVIEW

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

# FIGURE 30-11: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)



#### TABLE 30-30: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

AC CHARACTERISTICS				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristic <sup>(1)</sup>		Min.	Тур.	Max.	Units	Conditions
TQ10	TtQH	TQCK High Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 TCY/N) + 25			ns	Must also meet Parameter TQ15
TQ11	TtQL	TQCK Low Time	Synchronous, with prescaler	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	_	— ns		Must also meet Parameter TQ15
TQ15	TtQP	TQCP Input Period	Synchronous, with prescaler	Greater of 25 + 50 or (1 Tcy/N) + 50	_	_	ns	
TQ20	TCKEXTMRL	Delay from External TQCK Clock Edge to Timer Increment		_	1	Тсү	—	

**Note 1:** These parameters are characterized but not tested in manufacturing.



#### FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param. No.	Symbol	Characte	eristic <sup>(3)</sup>	Min.	Max.	Units	Conditions	
IS10	TLO:SCL Clock Low Time		100 kHz mode	4.7		μS		
			400 kHz mode	1.3	_	μS		
			1 MHz mode <sup>(1)</sup>	0.5	—	μS		
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	-	μS	Device must operate at a minimum of 1.5 MHz	
			400 kHz mode	0.6	—	μS	Device must operate at a minimum of 10 MHz	
			1 MHz mode <sup>(1)</sup>	0.5		μS		
IS20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be from	
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode <sup>(1)</sup>	—	100	ns		
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from	
			400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF	
			1 MHz mode <sup>(1)</sup>	—	300	ns		
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250		ns		
			400 kHz mode	100		ns		
			1 MHz mode <sup>(1)</sup>	100		ns		
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0		μS		
			400 kHz mode	0	0.9	μS		
			1 MHz mode <sup>(1)</sup>	0	0.3	μS		
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7		μS	Only relevant for Repeated	
			400 kHz mode	0.6		μS	Start condition	
			1 MHz mode <sup>(1)</sup>	0.25	—	μS		
IS31	THD:STA	Start Condition	100 kHz mode	4.0	—	μS	After this period, the first	
		Hold Time	400 kHz mode	0.6	—	μS	clock pulse is generated	
			1 MHz mode <sup>(1)</sup>	0.25	—	μS		
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	μS		
			400 kHz mode	0.6	—	μS		
			1 MHz mode <sup>(1)</sup>	0.6	—	μS		
IS34	THD:STO	Stop Condition	100 kHz mode	4	—	μS		
		Hold Time	400 kHz mode	0.6	—	μS		
			1 MHz mode <sup>(1)</sup>	0.25		μS		
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns		
			400 kHz mode	0	1000	ns		
			1 MHz mode <sup>(1)</sup>	0	350	ns		
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μS	Time the bus must be free	
			400 kHz mode	1.3	—	μS	perore a new transmission	
	<u> </u>		1 MHz mode <sup>(1)</sup>	0.5	—	μS	Call Stall	
IS50	Св	Bus Capacitive Lo	bading	—	400	pF		
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	(Note 2)	

#### TABLE 30-50: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**2:** Typical value for this parameter is 130 ns.

**3:** These parameters are characterized, but not tested in manufacturing.

# 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Number of Pins	N		64		
Pitch	е		0.50 BSC		
Overall Height	A	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3	0.20 REF			
Overall Width	E	9.00 BSC			
Exposed Pad Width	E2	5.30	5.40	5.50	
Overall Length	D	9.00 BSC			
Exposed Pad Length	D2	5.30	5.40	5.50	
Contact Width	b	0.20	0.25	0.30	
Contact Length	L	0.30	0.40	0.50	
Contact-to-Exposed Pad	K	0.20	-	-	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2