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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24К х 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512mc206-e-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### 2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (VIH) and Voltage Input Low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB<sup>®</sup> PICkit<sup>™</sup> 3, MPLAB ICD 3, or MPLAB REAL ICE<sup>™</sup>.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- "Using MPLAB<sup>®</sup> ICD 3" (poster) DS51765
- "MPLAB<sup>®</sup> ICD 3 Design Advisory" DS51764
- "MPLAB<sup>®</sup> REAL ICE<sup>™</sup> In-Circuit Emulator User's Guide" DS51616
- "Using MPLAB<sup>®</sup> REAL ICE™ In-Circuit Emulator" (poster) DS51749

### 2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator. For details, see **Section 9.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.



#### SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



### 3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

### 3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls.

### 3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

### 3.3 Data Space Addressing

The base Data Space can be addressed as 64 Kbytes (32K words).

The Data Space includes two ranges of memory, referred to as X and Y data memory. Each memory range is accessible through its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Spaces have memory locations that are device-specific, and are described further in the data memory maps in **Section 4.2 "Data Address Space"**.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 32-Kbyte aligned program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to the "**Data Memory**" (DS70595) and "**Program Memory**" (DS70613) sections in the "*dsPIC33/PIC24 Family Reference Manual*" for more details on EDS, PSV and table accesses.

On the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reversed Addressing.

### 3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- · Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.





### 4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

### 4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

### 4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- · Register Indirect
- · Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal
- Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

### TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
GIE	DISI	SWTRAP		_	_	_	—
bit 15				·			bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
		_	_	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0
Legend:	L:1		L:1			(0)	
R = Readable	DIT	vv = vvritable	DIT		mented bit, read	as '0'	
-n = value at I	POR	"1" = Bit is set		$0^{\circ} = Bit is cle$	eared	x = Bit is unkr	nown
hit 15		ntorrunt Enable	, hit				
DIL 15		and associate	d IF hits are e	nahled			
	0 = Interrupts	are disabled,	but traps are s	still enabled			
bit 14	DISI: DISI Ir	nstruction Statu	s bit				
	1 = DISI ins	truction is activ	e				
	0 = DISI <b>ins</b> i	truction is not a	ictive				
bit 13	SWTRAP: So	oftware Trap St	atus bit				
	1 = Software	trap is enabled	4				
hit 12-3		ted. Read as '	 				
bit 2	INT2FP: Exte	ernal Interrupt 2	∘ PEdge Detect	Polarity Selec	et bit		
	1 = Interrupt	on negative ed	ae				
	0 = Interrupt	on positive edg	le				
bit 1	INT1EP: Exte	ernal Interrupt ?	Edge Detect	Polarity Selec	ct bit		
	1 = Interrupt	on negative ed	ge				
	0 = Interrupt	on positive edg	e				
bit 0	INTOEP: Exte	ernal Interrupt (	) Edge Detect	Polarity Selec	ct bit		
	$\perp$ = interrupt	on negative ed	ye Ie				

### REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

### 11.4.4.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 11-18 through Register 11-27). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

#### FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUT FOR RPn



### 11.4.4.3 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-toone and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

### TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPxR<5:0>	Output Name
Default PORT	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U2TX	000011	RPn tied to UART2 Transmit
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
SS2	001010	RPn tied to SPI2 Slave Select
C1TX <sup>(2)</sup>	001110	RPn tied to CAN1 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
SYNCO1 <sup>(1)</sup>	101101	RPn tied to PWM Primary Time Base Sync Output
QEI1CCMP <sup>(1)</sup>	101111	RPn tied to QEI 1 Counter Comparator Output
REFCLKO	110001	RPn tied to Reference Clock Output
C4OUT	110010	RPn tied to Comparator Output 4

Note 1: This function is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This function is available in dsPIC33EPXXXGP/MC50X devices only.

### REGISTER 11-15: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

	5444.0	D 44/ 0	<b>D</b> 444 0		D 44/ 0	D 444 0				
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
—		SYNCI1R<6:0>								
bit 15							bit 8			
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
—	—	—		—	—	—	_			
bit 7				-	•		bit 0			
Legend:										
R = Readabl	le bit	W = Writable b	oit	U = Unimplemented bit, read as '0'						
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown				
bit 15	Unimplemer	nted: Read as '0	)'							
bit 14-8	SYNCI1R<6: (see Table 11	• <b>0&gt;:</b> Assign PWI I-2 for input pin :	VI Synchroniz selection nur	zation Input 1 to nbers)	o the Correspon	ding RPn Pin b	its			
	1111001 <b>=  </b>	nput tied to RPI	121							
	•									
	•									
	0000001 = l	nout tied to CME	21							
	0000000 = 1	nput tied to Vss								
bit 7-0	Unimplemer	nted: Read as '0	)'							

### 12.2 Timer1 Control Register

							ı			
R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0			
TON <sup>(1)</sup>	—	TSIDL	—	_	—	—	—			
bit 15							bit 8			
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0			
	TGATE	TCKPS1	TCKPS0	_	TSYNC <sup>(1)</sup>	TCS <sup>(1)</sup>	—			
bit 7 bit 0										
Legend:										
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'				
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own			
		(1)								
bit 15	TON: Timer1	On bit <sup>(1)</sup>								
	1 = Starts 16-	bit Limer1 bit Timer1								
bit 1/	Unimplement	ted: Pead as '	ı'							
bit 13		1 Stop in Idle N	/ode hit							
DIC 15	1 = Discontinu	i stop in lae k	eration when a	device enters l	dle mode					
	0 = Continues	module opera	tion in Idle mo	ode						
bit 12-7	Unimplement	ted: Read as '	)'							
bit 6	TGATE: Time	TGATE: Timer1 Gated Time Accumulation Enable bit								
	When TCS =	<u>1:</u> prod								
	When TCS =	0. 0.								
	1 = Gated tim	<u>e</u> accumulatior	n is enabled							
	0 = Gated tim	e accumulatior	n is disabled							
bit 5-4	TCKPS<1:0>	: Timer1 Input	Clock Prescal	e Select bits						
	11 = 1:256									
	10 = 1:64 01 = 1:8									
	01 = 1.0 00 = 1.1									
bit 3	Unimplement	ted: Read as '	)'							
bit 2	TSYNC: Time	er1 External Clo	ock Input Sync	chronization Se	elect bit <sup>(1)</sup>					
	When TCS =	1:								
	1 = Synchroni	izes external cl	ock input							
	0 = Does not	synchronize ex	ternal clock in	nput						
	This bit is jand	<u>ored</u> .								
bit 1	TCS: Timer1 (	Clock Source S	Select bit <sup>(1)</sup>							
	1 = External c	lock is from pir	n, T1CK (on th	ne rising edge)						
	0 = Internal cl	ock (FP)		5 5-7						
bit 0	Unimplement	ted: Read as '	)'							
Note 1: \	When Timer1 is en attempts by user so	abled in Exterr oftware to write	al Synchrono to the TMR1	us Counter mo register are ig	ode (TCS = 1, T nored.	SYNC = 1, TO	N = 1), any			

### REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

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## REGISTER 16-13: IOCONX: PWMx I/O CONTROL REGISTER<sup>(2)</sup> (CONTINUED)

- bit 1 SWAP: SWAP PWMxH and PWMxL Pins bit
   1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins
   0 = PWMxH and PWMxL pins are mapped to their respective pins
   bit 0 OSYNC: Output Override Synchronization bit
   1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWMx period boundary
  - 0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary
- Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
  - 2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

#### FIGURE 17-1: QEI BLOCK DIAGRAM



U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	_	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0
bit 15							bit 8
U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	_	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 15-14	Unimplemen	ted: Read as '	0'				
bit 13-8	<b>FBP&lt;5:0&gt;:</b> F	IFO Buffer Poir	nter bits				
	011111 = RE	331 buffer					
	•	50 builer					
	•						
	•						
	000001 <b>= TR</b>	B1 buffer					
	000000 = TR	RB0 buffer					
bit 7-6	Unimplemen	ted: Read as '	0'				
bit 5-0	FNRB<5:0>:	FIFO Next Rea	ad Buffer Poin	ter bits			
	011111 <b>= RE</b>	331 buffer					
	011110 <b>= RE</b>	330 buffer					
	•						
	•						
	•						
	000001 = TR	(B1 buffer					
	000000 = TR						

### REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER



dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

### REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)

- PTGITM<1:0>: PTG Input Trigger Command Operating Mode bits<sup>(1)</sup>
  - 11 = Single level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
  - 10 = Single level detect with Step delay executed on exit of command
  - 01 = Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
  - 00 = Continuous edge detect with Step delay executed on exit of command
- Note 1: These bits apply to the PTGWHI and PTGWLO commands only.

bit 1-0

- **2:** This bit is only used with the PTGCTRL step command software trigger option.
- **3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

bit 3-0	Step Command	OPTION<3:0>	Option Description						
	PTGCTRL(1)	0000	Reserved.						
		0001	Reserved.						
		0010	Disable Step Delay Timer (PTGSD).						
		0011	Reserved.						
		0100	Reserved.						
		0101	Reserved.						
		0110	Enable Step Delay Timer (PTGSD).						
		0111	Reserved.						
		1000	Start and wait for the PTG Timer0 to match the Timer0 Limit Register.						
		1001	Start and wait for the PTG Timer1 to match the Timer1 Limit Register.						
		1010	Reserved.						
		1011	Wait for the software trigger bit transition from low-to-high before continuing (PTGSWT = 0 to 1).						
		1100	Copy contents of the Counter 0 register to the AD1CHS0 register.						
		1101	Copy contents of the Counter 1 register to the AD1CHS0 register.						
		1110	Copy contents of the Literal 0 register to the AD1CHS0 register.						
		1111	Generate triggers indicated in the Broadcast Trigger Enable register (PTGBTE).						
	PTGADD(1)	0000	Add contents of the PTGADJ register to the Counter 0 Limit register (PTGC0LIM).						
		0001	Add contents of the PTGADJ register to the Counter 1 Limit register (PTGC1LIM).						
		0010	Add contents of the PTGADJ register to the Timer0 Limit register (PTGT0LIM).						
		0011	Add contents of the PTGADJ register to the Timer1 Limit register (PTGT1LIM).						
		0100	Add contents of the PTGADJ register to the Step Delay Limit register (PTGSDLIM).						
		0101	Add contents of the PTGADJ register to the Literal 0 register (PTGL0).						
		0110	Reserved.						
		0111	Reserved.						
	PTGCOPY(1)	1000	Copy contents of the PTGHOLD register to the Counter 0 Limit register (PTGC0LIM).						
		1001	Copy contents of the PTGHOLD register to the Counter 1 Limit register (PTGC1LIM).						
		1010	Copy contents of the PTGHOLD register to the Timer0 Limit register (PTGT0LIM).						
		1011	Copy contents of the PTGHOLD register to the Timer1 Limit register (PTGT1LIM).						
		1100	Copy contents of the PTGHOLD register to the Step Delay Limit register (PTGSDLIM).						
		1101	Copy contents of the PTGHOLD register to the Literal 0 register (PTGL0).						
		1110	Reserved.						
		1111	Reserved.						

### TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 24-2 for the trigger output descriptions.

3: This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 2	5-3: CM4C	ON: COMPA	RATOR 4 CO	ONTROL RE	GISTER		
R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
CON	COE	CPOL	_			CEVT	COUT
bit 15							bit 8
R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0		CREF <sup>(1)</sup>			CCH1 <sup>(1)</sup>	CCH0 <sup>(1)</sup>
bit 7	•		1				bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	iown
bit 15	CON: Compa	rator Enable bi	t				
	1 = Comparat	tor is enabled					
	0 = Comparat	tor is disabled					
bit 14	COE: Compa	rator Output Er	hable bit				
	1 = Comparat	tor output is pre	esent on the C	xOUT pin			
bit 12		or output is inte	elliai Ulliy Dolority Soloot	hit			
DIL 13	1 = Comparat	tor output is inv		DI			
	0 = Comparat	tor output is not	t inverted				
bit 12-10	Unimplemen	ted: Read as '	כ'				
bit 9	CEVT: Compa	arator Event bit					
	1 = Compara	tor event acco	ording to EVF	POL<1:0> sett	ings occurred;	disables future	triggers and
	interrupts	s until the bit is	cleared				
hit 0		areter Output h					
DILO	When CPOL	= 0 (non-invert	nt ad polarity):				
	1 = VIN + > VII	<u>- 0 (11011-1117C110</u> N-	cu polanty).				
	0 = VIN + < VII	N-					
	When CPOL	= 1 (inverted po	olarity):				
	1 = VIN + < VII	N-					
bit 7.6		<ul> <li>Triagor/Eyopt</li> </ul>		arity Soloct bits	-		
bit 7-0	11 = Trigger/e		nenerated on	any change of	s f the comparato	r output (while (	CEVT = 0
	10 = Trigger/e output (v	event/interrupt g while CEVT = 0	generated only )	on high-to-low	v transition of the	e polarity selecte	ed comparator
	<u>If CPOL</u> Low-to-t	= 1 (inverted p high transition of	olarity): of the compara	ator output.			
	If CPOL High-to-	= 0 (non-inver low transition o	<u>ted polarity):</u> f the compara	ator output.			
	01 = Trigger/e output (v	event/interrupt o while CEVT = 0	generated only )	on low-to-high	n transition of the	e polarity selecte	ed comparator
	<u>If CPOL</u> High-to-	= 1 (inverted p low transition o	<u>olarity):</u> f the compara	ator output.			
	<u>If CPOL</u> Low-to-ł	<u>= 0 (non-inver</u> nigh transition o	ted polarity): of the compara	ator output.			
	00 = Trigger/e	event/interrupt	generation is	disabled			
				1	() ( <b>D</b> ) <b>D</b>		

Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

### 26.3 Programmable CRC Registers

### REGISTER 26-1: CRCCON1: CRC CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0		
CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0		
bit 15							bit 8		
R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0		
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	_	—		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'			
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown		
bit 15 CRCEN: CRC Enable bit 1 = CRC module is enabled 0 = CRC module is disabled; all state machines, pointers and CRCWDAT/CRCDAT are reset, other SERs are not reset									
bit 14	Unimplemen	ted: Read as '	0'						
bit 13	CSIDL: CRC	Stop in Idle Mo	ode bit						
	1 = Discontin 0 = Continue	ues module op s module oper	peration when ation in Idle m	device enters lode	Idle mode				
bit 12-8	VWORD<4:0	>: Pointer Valu	e bits						
	Indicates the or 16 when Pl	number of value $LEN<4:0> \le 7.$	d words in the	FIFO. Has a n	naximum value	of 8 when PLE	N<4:0> > 7		
bit 7	CRCFUL: CR	C FIFO Full bi	t						
	1 = FIFO is fu	ull .							
		ot full							
DIT 6	1 = FIFO is e	C FIFO Empty	/ Bit						
	0 = FIFO is n	ot empty							
bit 5	CRCISEL: CF	RC Interrupt Se	election bit						
	1 = Interrupt 0 = Interrupt	on FIFO is em on shift is com	pty; final word plete and CR(	of data is still CWDAT results	shifting through are ready	CRC			
bit 4	CRCGO: Star	t CRC bit							
	1 = Starts CR 0 = CRC seri	C serial shifte al shifter is tur	r ned off						
bit 3	LENDIAN: Da	ata Word Little-	Endian Config	guration bit					
	1 = Data wor 0 = Data wor	d is shifted into d is shifted into	o the CRC star o the CRC star	rting with the L rting with the M	Sb (little endiar ISb (big endian	1) )			
bit 2-0	Unimplemen	ted: Read as '	0'	-					

## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

DC CHARACTERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)}^{(1)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic	Min.	Тур. <sup>(2)</sup>	Max.	Units	Conditions
Op Am	p DC Chara	cteristics					
CM40	VCMR	Common-Mode Input Voltage Range	AVss	_	AVDD	V	
CM41	CMRR	Common-Mode Rejection Ratio <sup>(3)</sup>	—	40		db	Vсм = AVdd/2
CM42	VOFFSET	Op Amp Offset Voltage <sup>(3)</sup>	—	±5	—	mV	
CM43	Vgain	Open-Loop Voltage Gain <sup>(3)</sup>	—	90		db	
CM44	los	Input Offset Current	—	_	_		See pad leakage currents in Table 30-11
CM45	Ів	Input Bias Current	—	-	_	_	See pad leakage currents in Table 30-11
CM46	Ιουτ	Output Current	—	_	420	μA	With minimum value of RFEEDBACK (CM48)
CM48	RFEEDBACK	Feedback Resistance Value	8	-	_	kΩ	
CM49a	VOADC	Output Voltage Measured at OAx Using ADC <sup>(3,4)</sup>	AVss + 0.077 AVss + 0.037 AVss + 0.018		AVDD – 0.077 AVDD – 0.037 AVDD – 0.018	V V V	Ιουτ = 420 μΑ Ιουτ = 200 μΑ Ιουτ = 100 μΑ
CM49b	Vout	Output Voltage Measured at OAxOUT Pin <sup>(3,4,5)</sup>	AVss + 0.210 AVss + 0.100 AVss + 0.050		AVDD - 0.210 AVDD - 0.100 AVDD - 0.050	V V V	Ιουτ = 420 μΑ Ιουτ = 200 μΑ Ιουτ = 100 μΑ
CM51	RINT1 <sup>(6)</sup>	Internal Resistance 1 (Configuration A and B) <sup>(3,4,5)</sup>	198	264	317	Ω	Min = -40°C Typ = +25°C Max = +125°C

### TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS (CONTINUED)

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

- 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.
- **3:** Parameter is characterized but not tested in manufacturing.
- 4: See Figure 25-6 for configuration information.
- 5: See Figure 25-7 for configuration information.
- 6: Resistances can vary by ±10% between op amps.

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



### **RECOMMENDED LAND PATTERN**

	N	<b>ILLIMETER</b>	S	
Dimension	MIN	NOM	MAX	
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

# 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	е	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	5.30	5.40	5.50
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	5.30	5.40	5.50
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-154A Sheet 2 of 2

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