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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep512mc206t-i-mr

Email: info@E-XFL.COM

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3.8 Arithmetic Logic Unit (ALU)

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X ALU is 16 bits wide, and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the <u>SR register. The C and DC</u> Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.9 DSP Engine (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulatorto-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- · Signed, unsigned or mixed-sign DSP multiply (US)
- · Conventional or convergent rounding (RND)
- · Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

	SOMMAN	
Instruction	Algebraic Operation	ACC Write Back
CLR	A = 0	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	$A = A + (x \bullet y)$	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	$A = x \bullet y$	No
MPY	$A = x^2$	No
MPY.N	$A = -x \bullet y$	No
MSC	$A = A - x \bullet y$	Yes

TABLE 3-2: DSP INSTRUCTIONS SUMMARY

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Program Memory" (DS70613) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in Section 4.8 "Interfacing Program and Data Memory Spaces".

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-5.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X AND PIC24EP32GP/MC20X DEVICES





FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP64MC20X/50X AND dsPIC33EP64GP50X DEVICES

TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC35	0886	_		JTAGIP<2:()>	—		ICDIP<2:0	>	_	—	—	—	—	_	—	—	4400
IPC36	0888			PTG0IP<2:0)>	—	PT	GWDTIP<	2:0>		P	TGSTEPIP<2	:0>	—	—		—	4440
IPC37	088A		_		_	—	F	PTG3IP<2:)>			PTG2IP<2:0	>	—	F	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	_	_				—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4		—		_	_	_				—	DAE	DOOVR	—	—		—	0000
INTCON4	08C6		—		_	_	_				—	—	—	—	—		SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<	3:0> VECNUM<7:0> 00							0000			

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	_	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	_		—		_	—	—	-	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	—	_		—		QEI1IF	PSEMIF	—		_		—		MI2C2IF	SI2C2IF		0000
IFS4	0808	_	-	CTMUIF	_		—	_	_		C1TXIF		_	CRCIF	U2EIF	U1EIF		0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	_	—	—	—	_	—	—	_	0000
IFS6	080C	—	—	—	—	—	—	—	—	_	—	—	—	_	—	—	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF		_		—	_	_		_		_		—	—		0000
IFS9	0812	_	-		_		—	_	_		PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF		0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	_	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	_	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	QEI1IE	PSEMIE	—	_	—	—	—	_	MI2C2IE	SI2C2IE	_	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	_	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	_	0000
IEC5	082A	PWM2IE	PWM1IE	_	—	_	—	—	—	_	—	_	—	_	_	—	_	0000
IEC6	082C	—	—	_	—	_	—	—	—	_	—	_	—	_	_	—	PWM3IE	0000
IEC7	082E	—	—	_	—	_	—	—	—	_	—	_	—	_	—	—	_	0000
IEC8	0830	JTAGIE	ICDIE	_	—	_	—	—	—	_	—	_	—	_	—	—	_	0000
IEC9	0832	—	—	_	—	_	—		—	_	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	_	0000
IPC0	0840	—		T1IP<2:0>		_		OC1IP<2:0)>	_		IC1IP<2:0>		_		INT0IP<2:0>		4444
IPC1	0842	—		T2IP<2:0>		_		OC2IP<2:0)>	_		IC2IP<2:0>		_	1	DMA0IP<2:0>		4444
IPC2	0844	—		U1RXIP<2:0)>	_		SPI1IP<2:0)>	_		SPI1EIP<2:0	>	_		T3IP<2:0>		4444
IPC3	0846	—	—	_	—	_	0)MA1IP<2:	0>	_		AD1IP<2:0>		_		U1TXIP<2:0>		0444
IPC4	0848			CNIP<2:0>		_		CMIP<2:0	>			MI2C1IP<2:0	>	_	:	SI2C1IP<2:0>		4444
IPC5	084A	—	—	_	—	_	—		—	_	—	_	—	_		INT1IP<2:0>		0004
IPC6	084C	—		T4IP<2:0>		_		OC4IP<2:0)>	_		OC3IP<2:0>		_	1	DMA2IP<2:0>		4444
IPC7	084E	—		U2TXIP<2:0	>	_	ι	J2RXIP<2:(0>	_		INT2IP<2:0>		_		T5IP<2:0>		4444
IPC8	0850	—		C1IP<2:0>	-	_	0	C1RXIP<2:(0>	_		SPI2IP<2:0>		_		SPI2EIP<2:0>		4444
IPC9	0852	—	—	_	—	_		IC4IP<2:0	>	_		IC3IP<2:0>		_	1	DMA3IP<2:0>		0444
IPC12	0858	—	—	_	—	_	N	112C2IP<2:	0>	_		SI2C2IP<2:0	>	_	—	—	_	0440
IPC14	085C	—	_	—	—	—	(QEI1IP<2:0)>	_		PSEMIP<2:0	>	—	—	—	—	0440
IPC16	0860	_		CRCIP<2:0	>	_		U2EIP<2:0	>	_		U1EIP<2:0>		_	_	_	_	4440
IPC17	0862	_	—	_	—	_	(C1TXIP<2:0	0>	_	—	—	—	_	_	_	_	0400
IPC19	0866	—	—	_	—	_	—	—	—	_		CTMUIP<2:0	>	_	—	—	_	0040

TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY

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TABLE 4-17: I2C1 AND I2C2 REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	_	—	_	_	—				I2C1 Recei	ve Register				0000
I2C1TRN	0202	_	_	_	_	_	_	_	_				I2C1 Trans	mit Register				00FF
I2C1BRG	0204	_	_	_	_	_	_	_				Bau	d Rate Gen	erator				0000
I2C1CON	0206	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	DISSLW SMEN GCEN STREN ACKDT ACKEN RCEN PEN RSEN SEN 10									1000
I2C1STAT	0208	ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	_	—	_	—						I2C1 Addr	ess Registe	r				0000
I2C1MSK	020C	—	_	—	_	—						I2C1 Ad	dress Mask					0000
I2C2RCV	0210	_	_	_	_	_	_	_	_				I2C2 Recei	ve Register				0000
I2C2TRN	0212	_	_		—	—		_	—				I2C2 Trans	mit Register				00FF
I2C2BRG	0214	—	_	—	_	—		_				Bau	d Rate Gen	erator				0000
I2C2CON	0216	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C2STAT	0218	ACKSTAT	TRSTAT		—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
I2C2ADD	021A	_		_	_	_	_					I2C2 Addr	ess Registe	r				0000
I2C2MSK	021C	_		_	_	_	_					I2C2 Ad	dress Mask					0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18: UART1 AND UART2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN<	<1:0>	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXI	SEL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	_	_	-	_	_	_	_				UART	1 Transmit F	Register				xxxx
U1RXREG	0226	_	_	-	_	_	_	UART1 Receive Register 00							0000			
U1BRG	0228							Baud	Rate Gen	erator Pre	scaler							0000
U2MODE	0230	UARTEN	_	USIDL	IREN	RTSMD	_	UEN<	<1:0>	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSE	L<1:0>	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXI	SEL<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	_	_	—	_	_	_	_				UART	2 Transmit F	Register				xxxx
U2RXREG	0236	_	_	—	_	_	_	_				UART	2 Receive F	Register				0000
U2BRG	0238		Baud Rate Generator Prescaler 0000															
			- ·															

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TADLL 4-2		LUANT	NL GIG I				ICINE	1<02) -	· • • • • .	I I OK US			IC/GFJ					
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	_	—	CSIDL	ABAT	CANCKS	R	EQOP<2:0)>	OPN	NODE<2:0	>	_	CANCAP	_	_	WIN	0480
C1CTRL2	0402	_	—	_	—	—	—	_	_	_	—	_		D	NCNT<4:0	>		0000
C1VEC	0404	_	_	_		F	ILHIT<4:0>			_				ICODE<6:0	>			0040
C1FCTRL	0406	[DMABS<2:0	>	—	—		—	_	_	—	—			FSA<4:0>			0000
C1FIFO	0408	_	_			FBP<	5:0>			_	_			FNRB	<5:0>			0000
C1INTF	040A	_	_	ТХВО	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	_	_	_	—	_	_	_	_	IVRIE	WAKIE	ERRIE	_	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E				TERRCN	T<7:0>							RERRCM	NT<7:0>				0000
C1CFG1	0410	_	_	_	—	_	_	_	_	SJW<	1:0>			BRP	<5:0>			0000
C1CFG2	0412	_	WAKFIL	_	—	_	SI	EG2PH<2:(0>	SEG2PHTS	SAM	S	EG1PH<2	::0>	P	RSEG<2:0	>	0000
C1FEN1	0414	FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8	FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0	FFFF
C1FMSKSEL1	0418	F7MS	K<1:0>	F6MS	K<1:0>	F5MS	K<1:0>	F4MS	K<1:0>	F3MSK	<1:0>	F2MS	K<1:0>	F1MSł	<<1:0>	F0MS	<<1:0>	0000
C1FMSKSEL2	041A	F15MS	SK<1:0>	F14MS	K<1:0>	F13MS	SK<1:0>	F12MS	SK<1:0>	F11MSK	<1:0>	F10MS	K<1:0>	F9MSł	<<1:0>	F8MS	< <1:0>	0000

TABLE 4-21: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 OR 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1<0>) = 0 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E							S	ee definition	when WIN	= x							
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PF	RI<1:0>	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PF	RI<1:0>	0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PF	RI<1:0>	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PF	RI<1:0>	0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PF	RI<1:0>	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PF	RI<1:0>	0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PF	RI<1:0>	TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PF	RI<1:0>	xxxx
C1RXD	0440							E	CAN1 Rece	eive Data Wo	ord							xxxx
C1TXD	0442							E	CAN1 Trans	smit Data W	ord							xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.4.4 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

Note:	То	protec	t	agains	st	misal	lign	ed	st	ack
	acc	esses,	W	15<0>	is	fixed	to	'0'	by	the
	hard	dware.								

W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

The Software Stack Pointer always points to the first available free word and fills the software stack working from lower toward higher addresses. Figure 4-19 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-19. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

- **Note 1:** To maintain system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).
 - 2: As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment

FIGURE 4-19: CALL STACK FRAME



5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory and to program two instruction words at a time. See the General Purpose and Motor Control Family tables (Table 1 and Table 2, respectively) for the page sizes of each device.

For more information on erasing and programming Flash memory, refer to "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual".

5.3 **Programming Operations**

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time) in Table 30-14 in **Section 30.0 "Electrical Characteristics"**.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS.

Refer to **Flash Programming**" (DS70609) in the "*dsPIC33/PIC24 Family Reference Manual*" for details and codes examples on programming using RTSP.

5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

5.4.1 KEY RESOURCES

- "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

5.5 Control Registers

Four SFRs are used to erase and write the program Flash memory: NVMCON, NVMKEY, NVMADRH and NVMADRL.

The NVMCON register (Register 5-1) enables and initiates Flash memory erase and write operations.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRH and NVMADRL. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations or the selected page for erase operations.

The NVMADRH register is used to hold the upper 8 bits of the EA, while the NVMADRL register is used to hold the lower 16 bits of the EA.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	_	—	_	_	_	—
bit 15		L	I	4			bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				INT2R<6:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown
-n = Value at F bit 15-7	POR Unimplemen	<pre>'1' = Bit is set ted: Read as '0</pre>	0'	ʻ0' = Bit is cle	ared	x = Bit is unkr	iown
-n = Value at F bit 15-7 bit 6-0	Unimplement INT2R<6:0>: (see Table 11-	'1' = Bit is set ted: Read as '0 Assign Externa -2 for input pin)' al Interrupt 2 (selection nun	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa -2 for input pin uput tied to RPI	o' al Interrupt 2 (selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	ared	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	OR Unimplemen INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '(Assign Externa -2 for input pin put tied to RPI	o' al Interrupt 2 (selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin uput tied to RPI	o' al Interrupt 2 (selection nun 121	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	POR Unimplement INT2R<6:0>: (see Table 11- 1111001 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin put tied to RPI	o' al Interrupt 2 (selection nun 121 P1	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr Pn Pin bits	iown
-n = Value at F bit 15-7 bit 6-0	Unimplement INT2R<6:0>: (see Table 11- 1111001 = In 0000001 = In 0000000 = In	'1' = Bit is set ted: Read as '0 Assign Externa 2 for input pin put tied to RPI put tied to CMI put tied to Vss	o' al Interrupt 2 (selection nun 121 P1	'0' = Bit is cle (INT2) to the C nbers)	orresponding R	x = Bit is unkr	iown

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_		_				_
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				T2CKR<6:0>			
bit 7							bit 0
Legend:							
R = Readabl	le bit	W = Writable I	bit	U = Unimplem	nented bit, read	as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own
bit 15-7	Unimplemen	ted: Read as 'o)'				
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11	ted: Read as '(: Assign Timer2 -2 for input pin)' 2 External Clo selection nur	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as '(: Assign Timer2 -2 for input pin nput tied to RPI) [;] 2 External Clo selection nur 121	ock (T2CK) to th nbers)	ie Correspondii	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as '(: Assign Timer2 -2 for input pin nput tied to RPI) [;] 2 External Clo selection nur 121	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as ' : Assign Timer2 -2 for input pin nput tied to RPI)' 2 External Cle selection nur 121	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir	ted: Read as 'c : Assign Timer2 -2 for input pin nput tied to RPI)' 2 External Clo selection nur 121 P1	ock (T2CK) to th nbers)	le Correspondi	ng RPn pin bits	
bit 15-7 bit 6-0	Unimplemen T2CKR<6:0> (see Table 11 1111001 = Ir 0000001 = Ir 0000000 = Ir	ted: Read as '(: Assign Timer2 -2 for input pin nput tied to RPI nput tied to CMI nput tied to Vss)' 2 External Clo selection nur 121 P1	ock (T2CK) to th nbers)	e Correspondi	ng RPn pin bits	

12.0 TIMER1

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Timers" (DS70362) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated in Asynchronous Counter mode from an external clock source
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler
- A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- · Gated Timer mode
- Synchronous Counter mode
- · Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit setting for different operating modes are given in the Table 12-1.

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	х
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

TABLE 12-1: TIMER MODE SETTINGS

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	_			DTR)	<13:8>		
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			DTR	2x<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

REGISTER 16-10: DTRx: PWMx DEAD-TIME REGISTER

bit 15-14 Unimplemented: Read as '0'

bit 13-0 DTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 16-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			ALTDTI	Rx<13:8>		
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			ALTDT	Rx<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	W = Writable bit U = Unimplemented bit, read as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-14 Unimplemented: Read as '0'

bit 13-0 ALTDTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB
bit 15					• •		bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
bit 7							bit 0
Legend:	a hit	\// - \//ritabla	h it	II – Unimploy	monted bit read	4 a.a. (0)	
n - Value at		vv = vvii(able	DIL	$0^{\circ} = 0$	nented bit, read	v – Ritic unkn	
		1 - Dit 13 36t			areu		
bit 15	OCAPEN: OF	-I Position Cou	nter Input Cap	ture Enable bit			
	1 = Index ma	tch event trigge	ers a position c	apture event			
	0 = Index ma	tch event does	not trigger a p	osition capture	event		
bit 14	FLTREN: QE	Ax/QEBx/INDX	x/HOMEx Digi	ital Filter Enabl	e bit		
	1 = Input pin	digital filter is e digital filter is d	nabled isabled (bypas	eed)			
hit 13_11			NDXv/HOMEv	Digital Input Fi	ilter Clock Divid	a Salact hits	
511 15-11	111 = 1:128 (clock divide		Digital Input I			
	110 = 1:64 cl	ock divide					
	101 = 1:32 cl	ock divide					
	100 = 1.16 cm 011 = 1:8 clo	ck divide					
	010 = 1:4 clo	ck divide					
	001 = 1:2 clo	ck divide ck divide					
hit 10₋9			Output Functi	ion Mode Sele	rt hits		
bit 10 5	11 = The CTN	VCMPx pin ace	s high when C	$EI1LEC \ge POS$	$S1CNT \ge QEI10$	GEC	
	10 = The CTM	NCMPx pin goe	s high when P	$OS1CNT \leq QE$	EIILEC		
	01 = The CT	NCMPx pin goe	s high when P	$OS1CNT \ge QE$	EI1GEC		
hit 8	SWPAB: Swa	s uisabled an OEA and OE	B Inputs hit				
bit 0	1 = QEAx and	d QEBx are swa	apped prior to	quadrature de	coder logic		
	0 = QEAx and	d QEBx are not	swapped	1			
bit 7	HOMPOL: HO	OMEx Input Po	larity Select bit	t			
	1 = Input is in	iverted					
hit 6		ot inverted Vy Input Dolori	ty Soloot bit				
DILO	1 = Input is in	verted	ly Select bit				
	0 = Input is no	ot inverted					
bit 5	QEBPOL: QE	EBx Input Polar	ity Select bit				
	1 = Input is ir	nverted					
L:1 4		ot inverted	:				
DIT 4		EAX Input Polar	ity Select bit				
	1 = 10000000000000000000000000000000000	not inverted					
bit 3	HOME: Statu	s of HOMEx In	out Pin After P	olarity Control			
	1 = Pin is at I	logic '1'		-			
	0 = Pin is at	logic '0'					

REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	_	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0
bit 15							bit 8
U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
_	_	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 15-14	Unimplemen	ted: Read as '	0'				
bit 13-8	FBP<5:0>: F	IFO Buffer Poir	nter bits				
	011111 = RE	331 buffer					
	•	50 bullet					
	•						
	•						
	000001 = TR	B1 buffer					
	000000 = TR	RB0 buffer					
bit 7-6	Unimplemen	ted: Read as '	0'				
bit 5-0	FNRB<5:0>:	FIFO Next Rea	ad Buffer Poin	ter bits			
	011111 = RE	331 buffer					
	011110 = RE	330 buffer					
	•						
	•						
	•						
	000001 = TR	(B1 buffer					
	$000000 = \mathbf{IR}$						

REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0

REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1

RXOVF4

bit 7			bit 0
Legend:	C = Writable bit, but or	nly '0' can be written to clear the bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	

RXOVF3

RXOVF2

R = Readable bit	vv = vvritable bit	0 = Onimplemented bit, read as 0				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15-0 RXOVF<15:0>: Receive Buffer n Overflow bits

RXOVF6

RXOVF7

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF5

REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF31 | RXOVF30 | RXOVF29 | RXOVF28 | RXOVF27 | RXOVF26 | RXOVF25 | RXOVF24 |
| bit 15 | | | | | | | bit 8 |

| R/C-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RXOVF23 | RXOVF22 | RXOVF21 | RXOVF20 | RXOVF19 | RXOVF18 | RXOVF17 | RXOVF16 |
| bit 7 | | | | | | | bit 0 |

Legend:	C = Writable bit, but only '0' can be written to clear the bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-0 RXOVF<31:16>: Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

RXOVF0

RXOVF1

BUFFER 21-7: ECAN™ MESSAGE BUFFER WORD 6

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Ву	te 7			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			By	te 6			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at PO	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown

bit 15-8 Byte 7<15:8>: ECAN Message Byte 7 bits

bit 7-0 Byte 6<7:0>: ECAN Message Byte 6 bits

BUFFER 21-8: ECAN[™] MESSAGE BUFFER WORD 7

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	_	FILHIT4 ⁽¹⁾	FILHIT3 ⁽¹⁾	FILHIT2 ⁽¹⁾	FILHIT1 ⁽¹⁾	FILHITO ⁽¹⁾
bit 15	- -						bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—		_	_		—	_
bit 7							bit 0
Legend:							

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12-8	FILHIT<4:0>: Filter Hit Code bits ⁽¹⁾
	Encodes number of filter that resulted in writing this buffer.
bit 7-0	Unimplemented: Read as '0'

Note 1: Only written by module for receive buffers, unused for transmit buffers.

REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGA	DJ<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGA	DJ<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable I	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 **PTGADJ<15:0>:** PTG Adjust Register bits This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGADD command.

REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGL0	<15:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGL	0<7:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 PTGL0<15:0>: PTG Literal 0 Register bits

This register holds the 16-bit value to be written to the AD1CHS0 register with the ${\tt PTGCTRL}$ Step command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss ⁽³⁾	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 3.0V^{(3)}$	0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $VDD < 3.0V^{(3)}$	-0.3V to +3.6V
Maximum current out of Vss pin	
Maximum current into VDD pin ⁽²⁾	
Maximum current sunk/sourced by any 4x I/O pin	
Maximum current sunk/sourced by any 8x I/O pin	25 mA
Maximum current sunk by all ports ^(2,4)	200 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).
 - 3: See the "Pin Diagrams" section for the 5V tolerant pins.
 - 4: Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

DC CHARACTI	ERISTICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Parameter No.	Тур.	Max.	Units	Conditions				
Idle Current (II	dle) ⁽¹⁾							
DC40d	3	8	mA	-40°C				
DC40a	3	8	mA	+25°C	2 21/			
DC40b	3	8	mA	+85°C	5.5V	10 1011-5		
DC40c	3	8	mA	+125°C				
DC42d	6	12	mA	-40°C				
DC42a	6	12	mA	+25°C	3 3\/	20 MIPS		
DC42b	6	12	mA	+85°C	5.5 V	20 1011 3		
DC42c	6	12	mA	+125°C				
DC44d	11	18	mA	-40°C				
DC44a	11	18	mA	+25°C	3 3\/			
DC44b	11	18	mA	+85°C	5.5 V	40 1011 3		
DC44c	11	18	mA	+125°C				
DC45d	17	27	mA	-40°C				
DC45a	17	27	mA	+25°C	3 3\/	60 MIRS		
DC45b	17	27	mA	+85°C	5.5V	00 1011-3		
DC45c	17	27	mA	+125°C				
DC46d	20	35	mA	-40°C				
DC46a	20	35	mA	+25°C	3.3V	70 MIPS		
DC46b	20	35	mA	+85°C				

TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (lidle)

Note 1: Base Idle current (IIDLE) is measured as follows:

• CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to Vss
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON<12>) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Symbol	Characteristic	Min. Typ. ⁽¹⁾ Max. Units Conditions						
OS50	Fplli	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	_	8.0	MHz	ECPLL, XTPLL modes		
OS51	Fvco	On-Chip VCO System Frequency	120	_	340	MHz			
OS52 TLOCK PLL Start-up Time (Lock Time)		0.9	1.5	3.1	ms				
OS53	DCLK	CLKO Stability (Jitter) ⁽²⁾	-3	0.5	3	%			

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases, or communication clocks used by the application, use the following formula:

$$Effective Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Time Base or Communication Clock}}}$$

For example, if Fosc = 120 MHz and the SPIx bit rate = 10 MHz, the effective jitter is as follows:

Effective Jitter =
$$\frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

TABLE 30-19: INTERNAL FRC ACCURACY

АС СНА	RACTERISTICS	Standard Operatin	d Operatin g tempera	g Conditi ture -40° -40°	ons: 3.0V °C ≤ Ta ≤ · °C ≤ Ta ≤ ·	to 3.6V (unless otherw ⊦85°C for Industrial ⊦125°C for Extended	vise stated)		
Param No.	Characteristic	Min.	Тур.	Max.	Units	Conditio	ons		
Internal	FRC Accuracy @ FRC Fre	equency =	7.37 MHz	<u>(</u> 1)					
F20a	FRC	-1.5	0.5	+1.5	%	$-40^{\circ}C \le TA \le -10^{\circ}C$	VDD = 3.0-3.6V		
		-1	0.5	+1	%	$-10^{\circ}C \le TA \le +85^{\circ}C \qquad VDD = 3.0-3.6V$			
F20b	FRC	-2	1	+2	%	$+85^{\circ}C \le TA \le +125^{\circ}C$	VDD = 3.0-3.6V		

Note 1: Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

TABLE 30-20: INTERNAL LPRC ACCURACY

AC CH	ARACTERISTICS	Standard Operating	Operating temperation	g Conditic ure -40° -40°	ons: 3.0V C ≤ TA ≤ + C ≤ TA ≤ +	to 3.6V (unless otherw 85°C for Industrial 125°C for Extended	ise stated)
Param No.	Characteristic	Min.	Тур.	Max.	Units	Conditio	ons
LPRC (@ 32.768 kHz ⁽¹⁾						
F21a	LPRC	-30		+30	%	$-40^\circ C \le T A \le -10^\circ C$	VDD = 3.0-3.6V
		-20		+20	%	$-10^{\circ}C \le TA \le +85^{\circ}C$	VDD = 3.0-3.6V
F21b	LPRC	-30		+30	%	$+85^{\circ}C \leq TA \leq +125^{\circ}C$	VDD = 3.0-3.6V

Note 1: The change of LPRC frequency as VDD changes.