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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64gp202-e-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Name ⁽⁴⁾	Pin Type	Buffer Type	PPS	Description	
U2CTS	1	ST	No	UART2 Clear-To-Send.	
U2RTS	0		No	UART2 Ready-To-Send.	
U2RX	I.	ST	Yes	UART2 receive.	
U2TX	Ó	_	Yes	UART2 transmit.	
BCLK2	Ō	ST	No	UART2 IrDA [®] baud clock output.	
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.	
SDI1	I	ST	No	SPI1 data in.	
SDO1	0	—	No	SPI1 data out.	
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.	
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.	
SDI2	I	ST	Yes	SPI2 data in.	
SDO2	0	—	Yes	SPI2 data out.	
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.	
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.	
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.	
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.	
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.	
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.	
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.	
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.	
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.	
TMS ⁽⁵⁾	Ι	ST	No	JTAG Test mode select pin.	
TCK	I	ST	No	JTAG test clock input pin.	
TDI	I	ST	No	JTAG test data input pin.	
TDO	0	_	No	JTAG test data output pin.	
C1RX ⁽²⁾	I	ST	Yes	ECAN1 bus receive pin.	
C1TX ⁽²⁾	0	_	Yes	ECAN1 bus transmit pin.	
FLT1 ⁽¹⁾ , FLT2 ⁽¹⁾	I	ST	Yes	PWM Fault Inputs 1 and 2.	
FLT3 ⁽¹⁾ , FLT4 ⁽¹⁾	I	ST	No	PWM Fault Inputs 3 and 4.	
FLT32 ^(1,3)	I	ST	No	PWM Fault Input 32 (Class B Fault).	
DTCMP1-DTCMP3 ⁽¹⁾	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 through 3.	
PWM1L-PWM3L ⁽¹⁾	0	—	No	PWM Low Outputs 1 through 3.	
PWM1H-PWM3H ⁽¹⁾	0	—	No	PWM High Outputs 1 through 3.	
SYNCI1 ⁽¹⁾	I	ST	Yes	PWM Synchronization Input 1.	
SYNCO1 ⁽¹⁾	0	—	Yes	PWM Synchronization Output 1.	
INDX1 ⁽¹⁾	Ι	ST	Yes	Quadrature Encoder Index1 pulse input.	
HOME1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Home1 pulse input.	
QEA1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer	
(4)				external clock/gate input in Timer mode.	
QEB1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase B input in QEI1 mode. Auxiliary timer	
				external clock/gate input in Timer mode.	
CNTCMP1''	υ	—	Yes	Quadrature Encoder Compare Output 1.	

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

 Legend:
 CMOS = CMOS compatible input or output
 Analog = Analog input

 ST = Schmitt Trigger input with CMOS levels
 O = Output

 PPS = Peripheral Pin Select
 TTL = TTL input buffer

P = Power I = Input

Note 1: This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: This pin is available on dsPIC33EPXXXGP/MC50X devices only.

3: This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)" for more information.

4: Not all pins are available in all packages variants. See the "Pin Diagrams" section for pin availability.

5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

3.6.1 KEY RESOURCES

- "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
GIE	DISI	SWTRAP		_	_	_	—
bit 15				·			bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
		_	_	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0
Legend:	L:1		L:1			(0)	
R = Readable	DIT	vv = vvritable	DIT		mented bit, read	as '0'	
-n = value at I	POR	"1" = Bit is set		$0^{\circ} = Bit is cle$	eared	x = Bit is unkr	nown
hit 15		ntorrunt Enable	, hit				
DIL 15		and associate	d IF hits are e	nahled			
	0 = Interrupts	are disabled,	but traps are s	still enabled			
bit 14	DISI: DISI Ir	nstruction Statu	s bit				
	1 = DISI ins	truction is activ	e				
	0 = DISI ins i	truction is not a	ictive				
bit 13	SWTRAP: So	oftware Trap St	atus bit				
	1 = Software	trap is enabled	4				
hit 12-3		ted. Read as '	 				
bit 2	INT2FP: Exte	ernal Interrupt 2	∘ PEdge Detect	Polarity Selec	et bit		
	1 = Interrupt	on negative ed	ae				
	0 = Interrupt	on positive edg	le				
bit 1	INT1EP: Exte	ernal Interrupt ?	Edge Detect	Polarity Selec	ct bit		
	1 = Interrupt	on negative ed	ge				
	0 = Interrupt	on positive edg	e				
bit 0	INTOEP: Exte	ernal Interrupt () Edge Detect	Polarity Selec	ct bit		
	\perp = interrupt	on negative ed	ye Ie				

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_	—	—	_	—	—	—
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSADR	<23:16>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable bi	t	U = Unimpler	mented bit, read	as '0'	

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 DSADR<23:16>: Most Recent DMA Address Accessed by DMA bits

REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSAI	DR<15:8>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable bit		U = Unimplemer	nted bit, re	ad as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleare	d	x = Bit is unknown	

bit 15-0 DSADR<15:0>: Most Recent DMA Address Accessed by DMA bits

9.0 OSCILLATOR CONFIGURATION

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Oscillator" (DS70580) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X oscillator system provides:

- On-chip Phase-Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources
- On-the-fly clock switching between various clock sources
- · Doze mode for system power savings
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Configuration bits for clock source selection
- A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM



2: The term, FP, refers to the clock source for all peripherals, while FCY refers to the clock source for the CPU. Throughout this document, FCY and FP are used interchangeably, except in the case of Doze mode. FP and FCY will be different when Doze mode is used with a doze ratio of 1:2 or lower.

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON		ROSSLP	ROSEL	RODIV3 ⁽¹⁾	RODIV2 ⁽¹⁾	RODIV1 ⁽¹⁾	RODIV0 ⁽¹⁾
bit 15				•		•	bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
		<u> </u>				<u> </u>	
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	ROON: Refer	ence Oscillato	Output Enab	ole bit			
	1 = Reference 0 = Reference	e oscillator outr e oscillator outr	but is enabled	on the REFCL	.K pin ⁽²⁾		
bit 14	Unimplemen	ted: Read as '	o'				
bit 13	ROSSLP: Re	ference Oscilla	tor Run in Sle	ep bit			
	1 = Reference	e oscillator outp	out continues	to run in Sleep			
	0 = Reference	e oscillator outp	out is disabled	l in Sleep			
bit 12	ROSEL: Refe	erence Oscillato	or Source Sel	ect bit			
	1 = Oscillator	crystal is used	as the refere	nce clock			
hit 11_8		Peference Os	cillator Divide	r hite(1)			
Dit 11-0	1111 = Refer	ence clock divi	ded by 32 76	R			
	1110 = Refer	ence clock divi	ded by 16,384	4			
	1101 = Refer	ence clock divi	ded by 8,192				
	1100 = Refer	ence clock divi	ded by 4,096				
	1011 = Refer	ence clock divi	ded by 2,048				
	1010 = Relef	ence clock divi	ded by 1,024 ded by 512				
	1000 = Refer	ence clock divi	ded by 256				
	0111 = Refer	ence clock divi	ded by 128				
	0110 = Reference clock divided by 64						
	0101 = Reference clock divided by 32						
	0100 = Reference clock divided by 8						
	0011 = Reference clock divided by 8 0010 = Reference clock divided by 4						
	0001 = Refer	ence clock divi	ded by 2				
	0000 = Refer	ence clock	-				
bit 7-0	Unimplemen	ted: Read as '	כי				

REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

- **Note 1:** The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
 - 2: This pin is remappable. See Section 11.4 "Peripheral Pin Select (PPS)" for more information.

14.0 INPUT CAPTURE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Input Capture" (DS70352) in the "dsPIC33/dsPIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices support four input capture channels.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 19 user-selectable Trigger/Sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to six clock sources available for each module, driving a separate internal 16-bit counter





14.2 Input Capture Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture Stop in Idle Control bit
	1 = Input capture will Halt in CPU Idle mode
	0 = Input capture will continue to operate in CPU Idle mode
bit 12-10	ICTSEL<2:0>: Input Capture Timer Select bits
	111 = Peripheral clock (FP) is the clock source of the ICx
	110 = Reserved
	101 = Reserved
	100 - 11 CLR is the clock source of the ICx (only the synchronous clock is supported) 011 = T5CLK is the clock source of the ICx
	010 = T4CLK is the clock source of the ICx
	001 = T2CLK is the clock source of the ICx
	000 = T3CLK is the clock source of the ICx
bit 9-7	Unimplemented: Read as '0'
bit 6-5	ICI<1:0>: Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
	11 = Interrupt on every fourth capture event
	10 = Interrupt on every third capture event
	01 = Interrupt on every second capture event
hit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
Dit 4	1 = Input capture buffer overflow occurred
	0 = No input capture buffer overflow occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	1 = Input capture buffer is not empty, at least one more capture value can be read
	0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture Mode Select bits
	111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
	110 = Unused (module is disabled)
	101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
	100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
	011 = Capture mode, every falling edge (Simple Capture mode)
	001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
	000 = Input capture module is turned off

r							
R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8
R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIC	G TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7							bit 0
r							
Legend:		HS = Hardwa	ire Settable bit				
R = Reada	able bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value	at POR	'1' = Bit is set	['0' = Bit is clea	ared	x = Bit is unkn	own
bit 15	FLTMD: Fault	Mode Select	bit				
	1 = Fault mo	de is maintain	ed until the Fa	ault source is r	removed; the c	orresponding	OCFLTx bit is
	cleared in	n software and	a new PWM pe	eriod starts	loved and a po	N DWM poriod	etarte
hit 14							Starts
DIL 14	1 = PWM out	nut is driven h	iah on a Fault				
	0 = PWM out	put is driven lo	w on a Fault				
bit 13	FLTTRIEN: Fa	ault Output Sta	ate Select bit				
	1 = OCx pin i	s tri-stated on	a Fault conditio	on			
	0 = OCx pin I	/O state is def	ined by the FLT	OUT bit on a F	ault condition		
bit 12	OCINV: Outpu	ut Compare x I	nvert bit				
	1 = OCx outp	out is inverted	bo				
hit 11_9		ted: Read as '	0'				
bit 8	OC32. Casca	de Two OCx M	° Iodules Enable	hit (32-hit oper	ration)		
bit 0	1 = Cascade	module opera	tion is enabled		allony		
	0 = Cascade	module opera	tion is disabled				
bit 7	OCTRIG: Out	put Compare >	k Trigger/Sync S	Select bit			
	1 = Triggers (0 = Synchron	OCx from the s izes OCx with	source designat the source des	ted by the SYN	CSELx bits SYNCSELx bit	s	
bit 6	TRIGSTAT: Ti	mer Trigger St	atus bit	0 ,			
	1 = Timer sou	urce has been	triggered and is	s running			
	0 = Timer sou	urce has not be	een triggered a	nd is being held	d clear		
bit 5	OCTRIS: Out	put Compare x	Coutput Pin Dir	ection Select b	it		
	1 = OCx is tri	-stated					
		ompare x mod	ule drives the C	DCx pin			
Note 1:	Do not use the O	Cx module as i	its own Synchro	nization or Trig	ger source.		
2:	When the OCy module as a Trigg	odule is turned jer source, the	l OFF, it sends a OCy module m	a trigger out sig nust be unseled	gnal. If the OCx	module uses t source prior	he OCy to disabling it.
3:	Each Output Com	ipare x module	e (OCx) has one	e PTG Trigger/S	Synchronization	n source. See S	Section 24.0
	PTGO0 = OC1	Jei Generator			malion.		
	PTGO1 = OC2						
	PTGO2 = OC3						
	PTGO3 = OC4						

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "High-Speed PWM" (DS70645) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support a dedicated Pulse-Width Modulation (PWM) module with up to 6 outputs.

The high-speed PWMx module consists of the following major features:

- Three PWM generators
- Two PWM outputs per PWM generator
- Individual period and duty cycle for each PWM pair
- Duty cycle, dead time, phase shift and frequency resolution of Tcy/2 (7.14 ns at Fcy = 70MHz)
- Independent Fault and current-limit inputs for six PWM outputs
- · Redundant output
- Center-Aligned PWM mode
- Output override control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for input clock
- PWMxL and PWMxH output pin swapping
- Independent PWM frequency, duty cycle and phase-shift changes for each PWM generator
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB) functionality
- Frequency resolution enhancement
- PWM capture functionality

Note: In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 8.32 ns.

The high-speed PWMx module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWMx can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADC module based on either of the two master time bases.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 input pin that utilizes PPS, can synchronize the high-speed PWMx module with an external signal. The SYNCO1 pin is an output pin that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

16.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs to include FLT1 and FLT2 which are remappable using the PPS feature, FLT3 and FLT4 which are available only on the larger 44-pin and 64-pin packages, and FLT32 which has been implemented with Class B safety features, and is available on a fixed pin on all dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

16.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the highspeed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled low externally or the internal pull-down resistor in the CNPDx register can be enabled.

Note: The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCON<1:0>), regardless of the state of FLT32.

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN ⁽¹⁾	UTXBF	TRMT
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7		-			bit 0		
Legend: HC = Hardware Clearab		e Clearable bit	C = Clearable bit				
R = Readable	e bit	W = Writable b	bit	U = Unimplemented bit, read as '0'			

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

		0 – Onimplemented bit, rea	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: UARTx Transmit Polarity Inversion bit
 - If IREN = 0: 1 = UxTX Idle state is '0'
 - 0 = UxTX Idle state is '1'
 - If IREN = 1:
 - 1 = IrDA encoded, UxTX Idle state is '1'
 - 0 = IrDA encoded, UxTX Idle state is '0'
- bit 12 Unimplemented: Read as '0'
- bit 11 UTXBRK: UARTx Transmit Break bit
 - 1 = Sends Sync Break on next transmission Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 - 0 = Sync Break transmission is disabled or completed
- **UTXEN:** UARTx Transmit Enable bit⁽¹⁾ bit 10 1 = Transmit is enabled, UxTX pin is controlled by UARTx
 - 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; UxTX pin is controlled by the PORT
- bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
 - 1 = Transmit buffer is full
 - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
 - 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
 - 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
 - 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
 - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters
- Note 1: Refer to the "UART" (DS70582) section in the "dsPIC33/PIC24 Family Reference Manual" for information on enabling the UARTx module for transmit operation.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	F15B	P<3:0>			F14B	P<3:0>		
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
-	F13B	P<3:0>			F12B	P<3:0>		
bit 7							bit 0	
Legend:								
R = Readab	le bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	'0' = Bit is cleared x = Bit is u		nown	
L								
bit 15-12	F15BP<3:0	>: RX Buffer Ma	sk for Filter 1	5 bits				
	1111 = Filte	er hits received in	n RX FIFO bu	uffer				
	1110 = Filte	r hits received in	n RX Buffer 1	4				
	•							
	•							
	•	n hite needined in						
	0001 = Filte	r hits received ii						
h:+ 44 0				4 h:ta (a a ma a ma)				
DIT 11-8	F14BP<3:0	>: RX Buffer Ma	SK for Fliter 1	4 bits (same va	iues as bits<15):12>)		
bit 7-4	F13BP<3:0>: RX Buffer Mask for Filter 13 bits (same values as bits<15:12>)							
bit 3-0 F12BP<3:0>: RX Buffer Mask for Filter 12 bits (same values as bits<15:12>)								

REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4

BUFFER 21-5: ECAN™ MESSAGE BUFFER WORD 4

R = Readable bit W = Writable bit (1' = Rit is set)		it	U = Unimplemented bit, read as '0'				
Legend:							
bit 7							bit 0
			Ву	rte 2			
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
bit 15							bit 8
			Ву	rte 3			
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x

bit 15-8 Byte 3<15:8>: ECAN Message Byte 3 bits

bit 7-0 Byte 2<7:0>: ECAN Message Byte 2 bits

BUFFER 21-6: ECAN™ MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Ву	/te 5			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Ву	/te 4			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'			
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is			x = Bit is unkr	nown			
-							

bit 15-8 Byte 5<15:8>: ECAN Message Byte 5 bits

bit 7-0 Byte 4<7:0>: ECAN Message Byte 4 bits

26.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Programmable Cyclic Redundancy Check (CRC)" (DS70346) of the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-programmable (up to 32nd order) polynomial CRC equation
- Interrupt output
- Data FIFO

The programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- · Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 26-1. A simple version of the CRC shift engine is shown in Figure 26-2.



FIGURE 26-1: CRC BLOCK DIAGRAM





26.1 Overview

The CRC module can be programmed for CRC polynomials of up to the 32nd order, using up to 32 bits. Polynomial length, which reflects the highest exponent in the equation, is selected by the PLEN<4:0> bits (CRCCON2<4:0>).

The CRCXORL and CRCXORH registers control which exponent terms are included in the equation. Setting a particular bit includes that exponent term in the equation; functionally, this includes an XOR operation on the corresponding bit in the CRC engine. Clearing the bit disables the XOR.

For example, consider two CRC polynomials, one a 16-bit equation and the other a 32-bit equation:

$$\begin{array}{c} x16+x12+x5+1\\ \text{and}\\ x32+x26+x23+x22+x16+x12+x11+x10+x8+x7\\ +x5+x4+x2+x+1 \end{array}$$

To program these polynomials into the CRC generator, set the register bits as shown in Table 26-1.

Note that the appropriate positions are set to '1' to indicate that they are used in the equation (for example, X26 and X23). The 0 bit required by the equation is always XORed; thus, X0 is a don't care. For a polynomial of length N, it is assumed that the *N*th bit will always be used, regardless of the bit setting. Therefore, for a polynomial length of 32, there is no 32nd bit in the CRCxOR register.

TABLE 26-1:CRC SETUP EXAMPLES FOR16 AND 32-BIT POLYNOMIAL

CBC Control	Bit Values					
Bits	16-bit Polynomial	32-bit Polynomial				
PLEN<4:0>	01111	11111				
X<31:16>	0000 0000 0000 000x	0000 0100 1100 0001				
X<15:0>	0001 0000 0010 000x	0001 1101 1011 011x				

26.2 Programmable CRC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

26.2.1 KEY RESOURCES

- "Programmable Cyclic Redundancy Check (CRC)" (DS70346) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

Field	Description
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 working registers ∈ {W0W15}
Wnd	One of 16 destination working registers ∈ {W0W15}
Wns	One of 16 source working registers ∈ {W0W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4W7}

TABLE 28-1:	SYMBOLS USED IN OPCODE DESCRIPTIONS ((CONTINUED)

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				r Industrial pr Extended
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Тур.	Max.	Units	Conditions
ТВ10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (TcY + 20)/N		_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N		_	ns	N = prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

TABLE 30-24:	TIMER2 AND TI	MER4 (TYPE B TIM	ER) EXTERNAL CLOC	K TIMING REQUIREMENTS
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Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Charac	teristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC11	TtxL	TxCK Low Time	Synchronous	Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous, with prescaler	2 Tcy + 40	—	_	ns	N = prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

AC CHARA	HARACTERISTICS Standard Operating Condition (unless otherwise stated) Operating temperature -40°C -40°C				s: 3.0V to 3.6V ≤ TA ≤ +85°C for Industrial ≤ TA ≤ +125°C for Extended		
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	СКЕ	СКР	SMP	
15 MHz	Table 30-33		_	0,1	0,1	0,1	
9 MHz	—	Table 30-34	—	1	0,1	1	
9 MHz	—	Table 30-35	—	0	0,1	1	
15 MHz	—	—	Table 30-36	1	0	0	
11 MHz	—	—	Table 30-37	1	1	0	
15 MHz		_	Table 30-38	0	1	0	
11 MHz	_	_	Table 30-39	0	0	0	

TABLE 30-33: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

FIGURE 30-14: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



TABLE 30-40:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	FscP	Maximum SCK2 Input Frequency	—	—	11	MHz	(Note 3)	
SP72	TscF	SCK2 Input Fall Time	—	-	_	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK2 Input Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO2 Data Output Fall Time			_	ns	See Parameter DO31 (Note 4)	
SP31	TdoR	SDO2 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	_	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	_	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120		—	ns		
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	—		ns	(Note 4)	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.



Temperature (Celsius)

70 80 90 100 110 120

TYPICAL FRC FREQUENCY @ VDD = 3.3V



-40 -30 -20 -10

0 10 20 30 40 50 60

FIGURE 32-9: