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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

·XF

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64gp202-e-sp

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#### 3.7 CPU Control Registers

R/W-0	) R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0				
0A <sup>(1)</sup>	OB <sup>(1)</sup>	SA <sup>(1,4)</sup>	SB <sup>(1,4)</sup>	OAB <sup>(1)</sup>	SAB <sup>(1)</sup>	DA <sup>(1)</sup>	DC				
bit 15							bit 8				
R/W-0 <sup>(2</sup>	R/W-0 <sup>(2,3)</sup>	R/W-0 <sup>(2,3)</sup>	R-0	R/W-0	R/W-0	R/W-0	R/W-0				
IPL2	IPL1	IPL0	RA	N	OV	Z	С				
bit 7							bit 0				
Legend:		C = Clearable	bit								
R = Reada	able bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'					
-n = Value	e at POR	'1'= Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown				
bit 15	OA: Accumu	lator A Overflow	v Status bit <sup>(1)</sup>								
	1 = Accumulator A has overflowed										
	0 = Accumulator A has not overflowed										
bit 14	bit 14 <b>OB:</b> Accumulator B Overflow Status bit(')										
	1 = Accumula	ator B has over	flowed								
hit 13		lator A Saturatio	n 'Sticky' Sta	tue hit(1,4)							
DIL 15	$1 = \Delta c cumula$	ator A is saturat	ed or has her	n saturated at	some time						
	0 = Accumula	ator A is not sat	urated		Some time						
bit 12	SB: Accumu	lator B Saturatio	on 'Sticky' Sta	tus bit <sup>(1,4)</sup>							
	1 = Accumula	ator B is satura	ed or has bee	en saturated at	some time						
	0 = Accumula	ator B is not sat	urated								
bit 11	<b>OAB:</b> OA    (	OB Combined A	ccumulator O	verflow Status	bit <sup>(1)</sup>						
	1 = Accumula	ators A or B have	ve overflowed								
	0 = Neither A	Accumulators A	or B have ove	erflowed	(1)						
bit 10	SAB: SA    S	B Combined A	cumulator 'Si	icky Status bit		<b>1</b>					
	1 = Accumula  0 = Neither A	ators A or B are	or B are satur	nave been sat	urated at some	time					
hit 9		Active hit(1)		alou							
bit 0	1 = DO loop is	s in progress									
	0 = DO loop is	s not in progres	S								
bit 8	DC: MCU AL	U Half Carry/Bo	orrow bit								
	1 = A carry-o	out from the 4th	low-order bit (	for byte-sized o	data) or 8th low-	order bit (for wo	ord-sized data)				
	of the re	sult occurred									
	0 = No carry	-out from the 4	th low-order t	bit (for byte-siz	ed data) or 8th	low-order bit (1	for word-sized				
	uala) U										
Note 1:	This bit is availabl	e on dsPIC33E	PXXXMC20X	/50X and dsPl	C33EPXXXGP	50X devices on	ly.				
2:	The IPL<2:0> bits	are concatenat	ed with the IF	PL<3> bit (COR	RCON<3>) to fo	rm the CPU Inte	errupt Priority				
	Level. The value in parentheses indicates the IPL, if IPL $<3> = 1$ . User interrupts are disabled when IPL $<3> = 1$										

#### REGISTER 3-1: SR: CPU STATUS REGISTER

- 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- **4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.





TABLE 4	4-9:	INPU		URE 1 T	HROUG	SH INPU	IT CAPI	URE 4	REGIST	ER MA	Р							
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1CON1	0140	_	_	ICSIDL		CTSEL<2:0	>	_	_	_	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
IC1CON2	0142	_	—	_	—	—	—	—	IC32	ICTRIG	TRIGSTAT	_		S	/NCSEL<4	:0>		000D
IC1BUF	0144							Inp	ut Capture	1 Buffer Re	gister							xxxx
IC1TMR	0146								Input Cap	ture 1 Time	r							0000
IC2CON1	0148	_	—	ICSIDL		CTSEL<2:0	>	_	—	_	ICI<'	1:0>	ICOV	ICOV ICBNE ICM<2:0>			0000	
IC2CON2	014A	_	—	_	—	—	—	—	IC32	ICTRIG	TRIGSTAT	_		SYNCSEL<4:0> 00				000D
IC2BUF	014C							Inp	ut Capture	2 Buffer Re	gister							xxxx
IC2TMR	014E								Input Cap	ture 2 Time	r							0000
IC3CON1	0150	_	—	ICSIDL		CTSEL<2:0	>	_	—	_	ICI<'	1:0>	ICOV	ICBNE		ICM<2:0>		0000
IC3CON2	0152	_	—	_	—	—	—	—	IC32	ICTRIG	TRIGSTAT	_		S	/NCSEL<4	:0>		000D
IC3BUF	0154							Inp	ut Capture	3 Buffer Re	gister							xxxx
IC3TMR	0156								Input Cap	ture 3 Time	r							0000
IC4CON1	0158	_	_	ICSIDL	I	CTSEL<2:0	>	_	_	_	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>		0000
IC4CON2	015A	_	_		—	_	—	_	IC32	ICTRIG	TRIGSTAT	_		S	/NCSEL<4	:0>		000D
IC4BUF	015C		•	•	•	•	•	Inp	ut Capture	4 Buffer Re	gister	•	•					xxxx
IC4TMR	015E								Input Cap	ture 4 Time	r							0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_	—	—	_	—	—	—
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSADR	<23:16>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable bi	t	U = Unimpler	mented bit, read	as '0'	

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 15-8 Unimplemented: Read as '0'

bit 7-0 DSADR<23:16>: Most Recent DMA Address Accessed by DMA bits

#### REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0					
DSADR<15:8>												
bit 15							bit 8					
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0					
	DSADR<7:0>											
bit 7							bit 0					
Legend:												
R = Readable	bit	W = Writable bit		U = Unimplemer	nted bit, re	ad as '0'						
-n = Value at P	OR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown									

bit 15-0 DSADR<15:0>: Most Recent DMA Address Accessed by DMA bits

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss	010 1101	I	RPI45
000 0001	I	C1OUT <sup>(1)</sup>	010 1110	I	RPI46
000 0010	I	C2OUT <sup>(1)</sup>	010 1111	I	RPI47
000 0011	I	C3OUT <sup>(1)</sup>	011 0000	_	_
000 0100	I	C4OUT <sup>(1)</sup>	011 0001		—
000 0101	_	_	011 0010		_
000 0110	I	PTGO30 <sup>(1)</sup>	011 0011	I	RPI51
000 0111	I	PTGO31 <sup>(1)</sup>	011 0100	I	RPI52
000 1000	I	FINDX1 <sup>(1,2)</sup>	011 0101	I	RPI53
000 1001	I	FHOME1 <sup>(1,2)</sup>	011 0110	I/O	RP54
000 1010	—	—	011 0111	I/O	RP55
000 1011	_	—	011 1000	I/O	RP56
000 1100	_	—	011 1001	I/O	RP57
000 1101		—	011 1010	I	RPI58
000 1110	_	—	011 1011	—	—
000 1111	_	—	011 1100	_	—
001 0000		—	011 1101		—
001 0001		_	011 1110	_	_
001 0010		_	011 1111	—	_
001 0011		—	100 0000		—
001 0100	I/O	RP20	100 0001	_	—
001 0101	_	—	100 0010	_	—
001 0110	—	—	100 0011	—	_
001 0111	—	—	100 0100	_	—
001 1000	I	RPI24	100 0101	—	—
001 1001	I	RPI25	100 0110	—	—
001 1010			100 0111		—
001 1011	I	RPI27	100 1000	_	—
001 1100	I	RPI28	100 1001	—	—
001 1101	—	—	100 1010	_	—
001 1110	_	—	100 1011	_	—
001 1111	—	—	100 1100	—	—
010 0000	I	RPI32	100 1101		—
010 0001	I	RPI33	100 1110	_	—
010 0010	I	RPI34	100 1111	—	—
010 0011	I/O	RP35	101 0000		
010 0100	I/O	RP36	101 0001	_	_
010 0101	I/O	RP37	101 0010	—	—
010 0110	I/O	RP38	101 0011		—
010 0111	I/O	RP39	101 0100	_	—

#### TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Legend: Shaded rows indicate PPS Input register values that are unimplemented.

Note 1: See Section 11.4.4.1 "Virtual Connections" for more information on selecting this pin assignment.

2: These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

#### 18.3 SPIx Control Registers

#### R/W-0 U-0 R/W-0 U-0 R/W-0 R/W-0 R/W-0 U-0 SPIEN SPISIDL SPIBEC<2:0> \_\_\_\_\_ bit 15 R/W-0 R/W-0 R/W-0 R/C-0, HS R/W-0 R/W-0 R-0, HS, HC R-0, HS, HC SRMPT SPIROV SRXMPT SISEL2 SISEL1 SISEL0 SPITBF SPIRBF bit 7 bit 0 Legend: C = Clearable bit HS = Hardware Settable bit HC = Hardware Clearable bit R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 SPIEN: SPIx Enable bit 1 = Enables the module and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as serial port pins 0 = Disables the module bit 14 Unimplemented: Read as '0' bit 13 SPISIDL: SPIx Stop in Idle Mode bit 1 = Discontinues the module operation when device enters Idle mode 0 = Continues the module operation in Idle mode bit 12-11 Unimplemented: Read as '0' bit 10-8 SPIBEC<2:0>: SPIx Buffer Element Count bits (valid in Enhanced Buffer mode) Master mode: Number of SPIx transfers that are pending. Slave mode: Number of SPIx transfers that are unread. **SRMPT:** SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode) bit 7 1 = SPIx Shift register is empty and Ready-To-Send or receive the data 0 = SPIx Shift register is not empty bit 6 SPIROV: SPIx Receive Overflow Flag bit

#### REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register 0 = No overflow has occurred SRXMPT: SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode) bit 5 1 = RX FIFO is empty 0 = RX FIFO is not empty bit 4-2 SISEL<2:0>: SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode) 111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set) 110 = Interrupt when last bit is shifted into SPIxSR and as a result, the TX FIFO is empty 101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete 100 = Interrupt when one data is shifted into the SPIxSR and as a result, the TX FIFO has one open memory location 011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set) 010 = Interrupt when the SPIx receive buffer is 3/4 or more full 001 = Interrupt when data is available in the receive buffer (SRMPT bit is set) 000 = Interrupt when the last data in the receive buffer is read and as a result, the buffer is empty

bit 8

R-0, HSC	R-0, HSC	U-0	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC	
ACKSTAT	TRSTAT			—	BCL	GCSTAT	ADD10	
bit 15					•		bit 8	
R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC	
IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	
bit 7							bit 0	
Legend:		C = Clearab	le bit	HS = Hardwa	re Settable bit	HSC = Hardware Settable/Clearable bit		
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'					
-n = Value at POR		'1' = Bit is se	et	'0' = Bit is clea	ared	x = Bit is unknown		

#### REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

bit 15	<b>ACKSTAT:</b> Acknowledge Status bit (when operating as $I^2C^{TM}$ master, applicable to master transmit operation)
	1 = NACK received from slave 0 = ACK received from slave
	Hardware is set or clear at the end of slave Acknowledge.
bit 14	<b>TRSTAT:</b> Transmit Status bit (when operating as $I^2C$ master, applicable to master transmit operation) 1 = Master transmit is in progress (8 bits + ACK)
	0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.
bit 13-11	Unimplemented: Read as '0'
bit 10	BCL: Master Bus Collision Detect bit
	<ul><li>1 = A bus collision has been detected during a master operation</li><li>0 = No bus collision detected</li></ul>
	Hardware is set at detection of a bus collision.
bit 9	GCSTAT: General Call Status bit
	1 = General call address was received
	0 = General call address was not received
1.11.0	Hardware is set when address matches general call address. Hardware is clear at Stop detection.
DIT 8	ADD10: 10-Bit Address Status bit
	I = 10-bit address was matched 0 = 10-bit address was not matched
	Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.
bit 7	IWCOL: I2Cx Write Collision Detect bit
	1 = An attempt to write to the I2CxTRN register failed because the $I^2$ C module is busy 0 = No collision
	Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).
bit 6	I2COV: I2Cx Receive Overflow Flag bit
	<ul> <li>1 = A byte was received while the I2CxRCV register was still holding the previous byte</li> <li>0 = No overflow</li> </ul>
	Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
bit 5	<b>D_A:</b> Data/Address bit (when operating as I <sup>2</sup> C slave)
	1 = Indicates that the last byte received was data
	<ul> <li>Indicates that the last byte received was a device address</li> <li>Hardware is clear at a device address match. Hardware is set by reception of a slave byte.</li> </ul>
bit 4	P: Stop bit
	1 = Indicates that a Stop bit has been detected last
	0 = Stop bit was not detected last
	Hardware is set or clear when a Start, Repeated Start or Stop is detected.

#### REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER (CONTINUED)

bit 0

**CH123SA:** Channel 1, 2, 3 Positive Input Select for Sample MUXA bit In 12-bit mode (AD21B = 1), CH123SA is Unimplemented and is Read as '0':

Value	ADC Channel							
value	CH1	CH2	CH3					
1 <b>(2)</b>	OA1/AN3	OA2/AN0	OA3/AN6					
0 <b>(1,2)</b>	OA2/AN0	AN1	AN2					

**Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0		
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0		
PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, reac	l as '0'			
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown		
bit 15-13PTGCLK<2:0>: Select PTG Module Clock Source bits111 = Reserved100 = Reserved101 = PTG module clock source will be T3CLK100 = PTG module clock source will be T2CLK011 = PTG module clock source will be T1CLK010 = PTG module clock source will be T1CLK010 = PTG module clock source will be F0SC000 = PTG module clock source will be FPbit 12-8PTGDIV<4:0>: PTG Module Clock Prescaler (divider) bits									
	PiGDIV<4:0>: PiG Module Clock Prescaler (divider) bits 11111 = Divide-by-32 11110 = Divide-by-31 • • • • • • • • • • • • •								
bit 7-4	PTGPWD<3:0	<b>0&gt;:</b> PTG Trigge	er Output Pulse	e-Width bits					
	<pre>PIGPWD&lt;3:0&gt;: PIG Trigger Output Pulse-Width bits 1111 = All trigger outputs are 16 PTG clock cycles wide 1110 = All trigger outputs are 15 PTG clock cycles wide</pre>								
bit 3	Unimplemen	ted: Read as '	0'						
bit 2-0	PTGWDT<2:0	0>: Select PTG	Watchdog Tir	mer Time-out	Count Value bits	3			
	PTGWDT<2:0>: Select PTG Watchdog Timer Time-out Count Value bits 111 = Watchdog Timer will time-out after 512 PTG clocks 110 = Watchdog Timer will time-out after 256 PTG clocks 101 = Watchdog Timer will time-out after 128 PTG clocks 100 = Watchdog Timer will time-out after 64 PTG clocks 011 = Watchdog Timer will time-out after 32 PTG clocks 010 = Watchdog Timer will time-out after 16 PTG clocks 001 = Watchdog Timer will time-out after 8 PTG clocks 001 = Watchdog Timer will time-out after 8 PTG clocks 000 = Watchdog Timer is disabled								

### REGISTER 24-2: PTGCON: PTG CONTROL REGISTER

## REGISTER 24-8: PTGC1LIM: PTG COUNTER 1 LIMIT REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
PTGC1LIM<15:8>											
bit 15							bit 8				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
			PTGC1L	_IM<7:0>							
bit 7							bit 0				
Logond											

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGC1LIM<15:0>:** PTG Counter 1 Limit Register bits May be used to specify the loop count for the PTGJMPC1 Step command or as a limit register for the General Purpose Counter 1.

## REGISTER 24-9: PTGHOLD: PTG HOLD REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
PTGHOLD<15:8>										
bit 15							bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
PTGHOLD<7:0>										
bit 7							bit 0			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGHOLD<15:0>:** PTG General Purpose Hold Register bits Holds user-supplied data to be copied to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGCOPY command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).





#### 26.1 Overview

The CRC module can be programmed for CRC polynomials of up to the 32nd order, using up to 32 bits. Polynomial length, which reflects the highest exponent in the equation, is selected by the PLEN<4:0> bits (CRCCON2<4:0>).

The CRCXORL and CRCXORH registers control which exponent terms are included in the equation. Setting a particular bit includes that exponent term in the equation; functionally, this includes an XOR operation on the corresponding bit in the CRC engine. Clearing the bit disables the XOR.

For example, consider two CRC polynomials, one a 16-bit equation and the other a 32-bit equation:

$$\begin{array}{c} x16+x12+x5+1\\ \text{and}\\ x32+x26+x23+x22+x16+x12+x11+x10+x8+x7\\ +x5+x4+x2+x+1 \end{array}$$

To program these polynomials into the CRC generator, set the register bits as shown in Table 26-1.

Note that the appropriate positions are set to '1' to indicate that they are used in the equation (for example, X26 and X23). The 0 bit required by the equation is always XORed; thus, X0 is a don't care. For a polynomial of length N, it is assumed that the *N*th bit will always be used, regardless of the bit setting. Therefore, for a polynomial length of 32, there is no 32nd bit in the CRCxOR register.

# TABLE 26-1:CRC SETUP EXAMPLES FOR16 AND 32-BIT POLYNOMIAL

CBC Control	Bit V	alues
Bits	16-bit Polynomial	32-bit Polynomial
PLEN<4:0>	01111	11111
X<31:16>	0000 0000 0000 000x	0000 0100 1100 0001
X<15:0>	0001 0000 0010 000x	0001 1101 1011 011x

## 26.2 Programmable CRC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

#### 26.2.1 KEY RESOURCES

- "Programmable Cyclic Redundancy Check (CRC)" (DS70346) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles <sup>(2)</sup>	Status Flags Affected
52	MUL	MUL.SS Wb,Ws,Wnd		{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS	Wb,Ws,Acc <sup>(1)</sup>	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb,Ws,Wnd {Whd+1, unsigned()		{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU	IUL.SU Wb,Ws,Acc <sup>(1)</sup> Accumulator = signed(Wb) * unsigned(Ws)		1	1	None
		MUL.SU	Wb,#lit5,Acc <sup>(1)</sup>	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US Wb,Ws,Wnd {Wnd + 1, Wnd} = unsigned(Wb)* signed(Ws)		1	1	None	
	MUL.US     Wb,Ws,Acc <sup>(1)</sup> Accumula signed(Ws signed(Ws MUL.UU       MUL.UU     Wb,Ws,Wnd     {Wnd + 1, unsigned(		Wb,Ws,Acc <sup>(1)</sup>	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
			{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None	
		MUL.UU Wb, #lit5, Acc <sup>(1)</sup> Accumulator = unsigned(Wb)* unsigned(lit5)		Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU	Wb,Ws,Acc <sup>(1)</sup>	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS	Wb,Ws,Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU	Wb,Ws,Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US	Wb,Ws,Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU	Wb,Ws,Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU	Wb,#lit5,Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU	Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
1		MUL.UU	Wb,#lit5,Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL	f	W3:W2 = f * WREG	1	1	None

#### TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles <sup>(2)</sup>	Status Flags Affected
72	SL	SL	f	f = Left Shift f	1	1	C,N,OV,Z
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
73	SUB	SUB	<sub>Acc</sub> (1)	Subtract Accumulators		1	OA,OB,OAB, SA,SB,SAB
		SUB	f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB	f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB	#lit10,Wn	Wn = Wn - lit10	1	1	C,DC,N,OV,Z
		SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
74	SUBB	SUBB	f	$f = f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	f,WREG	WREG = $f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	#lit10,Wn	Wn = Wn – lit10 – $(\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,Ws,Wd	$Wd = Wb - Ws - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,#lit5,Wd	$Wd = Wb - lit5 - (\overline{C})$	1	1	C,DC,N,OV,Z
75	SUBR	SUBR	f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
76	SUBBR	SUBBR	f	$f = WREG - f - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	f,WREG	WREG = WREG – f – $(\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	Wb,Ws,Wd	$Wd = Ws - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	Wb,#lit5,Wd	$Wd = lit5 - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
77	SWAP	SWAP.b	Wn	Wn = nibble swap Wn	1	1	None
		SWAP	Wn	Wn = byte swap Wn	1	1	None
78	TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	5	None
79	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	5	None
80	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
81	TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
82	ULNK	ULNK		Unlink Frame Pointer	1	1	SFA
83	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
84	ZE	ZE	Ws,Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

#### TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

2: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

DC CH	ARACTE	RISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.	Symbol	Characteristic	Min. Typ. Max. Units Conditions						
	VIL	Input Low Voltage							
DI10		Any I/O Pin and MCLR	Vss	—	0.2 VDD	V			
DI18		I/O Pins with SDAx, SCLx	Vss	_	0.3 VDD	V	SMBus disabled		
DI19		I/O Pins with SDAx, SCLx	Vss	—	0.8	V	SMBus enabled		
	Vih	Input High Voltage							
DI20		I/O Pins Not 5V Tolerant	0.8 VDD	—	Vdd	V	(Note 3)		
		I/O Pins 5V Tolerant and MCLR	0.8 VDD	—	5.5	V	(Note 3)		
		I/O Pins with SDAx, SCLx	0.8 VDD	—	5.5	V	SMBus disabled		
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled		
	ICNPU	Change Notification Pull-up Current							
DI30			150	250	550	μA	VDD = 3.3V, VPIN = VSS		
	ICNPD	Change Notification Pull-Down Current <sup>(4)</sup>							
DI31			20	50	100	μA	VDD = 3.3V, VPIN = VDD		

#### TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

**Note 1:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (VSS 0.3). Characterized but not tested.

**5:** Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.



TADLE 30-23. THVIER I EATERINAL CLOCK THVIING REQUIREIVIEN 13	TABLE 30-23:	TIMER1 EXTERNAL	<b>CLOCK TIMING</b>	<b>REQUIREMENTS</b> <sup>(1)</sup>
---------------------------------------------------------------	--------------	-----------------	---------------------	------------------------------------

AC CHARACTERISTICS			Standard Ope (unless other) Operating tem	rating C vise sta perature	conditions: 3.0 ted) -40°C ≤ TA ≤ -40°C ≤ TA ≤	V to 3.6 +85°C +125°C	V for Industrial C for Extended	
Param No.	Symbol	Characteristic <sup>(2)</sup>		Min.	Тур.	Max.	Units	Conditions
TA10	ТтхН	T1CK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	—	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)
			Asynchronous	35		—	ns	
TA11	ΤτxL	T1CK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256)
			Asynchronous	10	—	—	ns	
TA15	ΤτχΡ	T1CK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	_		ns	N = prescale value (1, 8, 64, 256)
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>))		DC		50	kHz	
TA20	TCKEXTMRL	(I1CON<1>)) Delay from External T1CK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

Note 1: Timer1 is a Type A.

2: These parameters are characterized, but are not tested in manufacturing.

#### 33.1 Package Marking Information (Continued)



### 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Ν	<b>IILLIMETER</b>	S			
Dimension	MIN	NOM	MAX			
Number of Pins	N		44			
Pitch	е	0.65 BSC				
Overall Height	A	0.80 0.90 1.00				
Standoff	A1	0.00 0.02 0.05				
Terminal Thickness	A3	0.20 REF				
Overall Width	E	8.00 BSC				
Exposed Pad Width	E2	6.25 6.45 6.60				
Overall Length	D	8.00 BSC				
Exposed Pad Length	D2	6.25	6.45	6.60		
Terminal Width	b	0.20 0.30 0.35				
Terminal Length	L	0.30 0.40 0.50				
Terminal-to-Exposed-Pad	K	0.20	-	-		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension. usually without tolerance. for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

# 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]



Microchip Technology Drawing C04-154A Sheet 1 of 2

PMD (PIC24EPXXXIVC20X Devices)	
PORTA (PIC24EPXXXGP/MC202,	
dsPIC33EPXXXGP/MC202/502 Devices) 104	
PORTA (PIC24EPXXXGP/MC203,	
dsPIC33EPXXXGP/MC203/503 Devices) 103	
PORTA (PIC24EPXXXGP/MC204,	
dsPIC33EPXXXGP/MC204/504 Devices) 102	
dsPIC33EPXXXGP/MC206/506 Devices)	
PORTB (PIC24EPXXXGP/MC202,	
dsPIC33EPXXXGP/MC202/502 Devices) 104	
PORTB (PIC24EPXXXGP/MC203,	
dsPIC33EPXXXGP/MC203/503 Devices) 103	
PORTB (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices)	
PORTC (PIC23EPXXXGP/MC203,	
dsPIC33EPXXXGP/MC203/503 Devices) 103	
PORTC (PIC24EPXXXGP/MC204	
doDIC22EDXXXCD/MC204/504 Dovideos) 102	
PORTC (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices)	
PORTD (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices) 100	
PORTE (PIC24EPXXXGP/MC206	
doDIC22EDXXXCD/MC206/506 Dovideos) 100	
PORTF (PIC24EPXXXGP/MC206,	
dsPIC33EPXXXGP/MC206/506 Devices) 100	
PORTG (PIC24EPXXXGP/MC206 and	
dsPIC33EPXXXGP/MC206/506 Devices) 101	
PTC 79	
FINI (0	
PWM (dsPIC33EPXXXMC20X/50X,	
PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices)	
PWM (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X/50X,         PIC24EPXXMC20X Devices)       79         PWM Generator 1 (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)         PWM Generator 2 (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)         PU24EPXXMC20X Devices)       80         PWM Generator 3 (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)         80       QEI1 (dsPIC33EPXXXMC20X/50X,         PIC24EPXXXMC20X Devices)       81         Reference Clock       93	
PIG	
PIG       76         PWM (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)         PWM Generator 1 (dsPIC33EPXXXMC20X/50X,       79         PWM Generator 2 (dsPIC33EPXXXMC20X/50X,       79         PWM Generator 2 (dsPIC33EPXXXMC20X/50X,       79         PUC24EPXXXMC20X Devices)       80         PWM Generator 3 (dsPIC33EPXXXMC20X/50X,       80         PUC24EPXXXMC20X Devices)       80         QEI1 (dsPIC33EPXXMC20X/50X,       81         Reference Clock       93         SPI1 and SPI2       83         System Control       93	
PIG       76         PWM (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)         PWM Generator 1 (dsPIC33EPXXXMC20X/50X,       79         PWM Generator 2 (dsPIC33EPXXXMC20X/50X,       79         PWM Generator 2 (dsPIC33EPXXXMC20X/50X,       79         PUC24EPXXXMC20X Devices)       80         PWM Generator 3 (dsPIC33EPXXXMC20X/50X,       81         PIC24EPXXXMC20X Devices)       80         QEI1 (dsPIC33EPXXXMC20X/50X,       81         Reference Clock       93         SPI1 and SPI2       83         System Control       93         Time1 through Time5       75	
PIG       70         PWM (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)         PWM Generator 1 (dsPIC33EPXXXMC20X/50X,       79         PWM Generator 2 (dsPIC33EPXXXMC20X/50X,       79         PWM Generator 2 (dsPIC33EPXXXMC20X/50X,       79         PUC24EPXXXMC20X Devices)       80         PWM Generator 3 (dsPIC33EPXXXMC20X/50X,       81         PIC24EPXXXMC20X Devices)       80         QEI1 (dsPIC33EPXXXMC20X/50X,       81         Reference Clock       93         SPI1 and SPI2       83         System Control       93         Time1 through Time5       75	
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PIG       76         PWM (dsPIC33EPXXMC20X/50X,       PIC24EPXXMC20X Devices)         PWM Generator 1 (dsPIC33EPXXMC20X/50X,       PIC24EPXXMC20X Devices)         PWM Generator 2 (dsPIC33EPXXMC20X/50X,       PIC24EPXXMC20X Devices)         PU24EPXXMC20X Devices)       80         PWM Generator 3 (dsPIC33EPXXMC20X/50X,       PIC24EPXXMC20X Devices)         80       PWM Generator 3 (dsPIC33EPXXMC20X/50X,         PIC24EPXXMC20X Devices)       80         QEI1 (dsPIC33EPXXMC20X/50X,       PIC24EPXXMC20X/50X,         PIC24EPXXXMC20X Devices)       81         Reference Clock       93         SPI1 and SPI2       83         System Control       93         Time1 through Time5       75         UART1 and UART2       82         Registers       AD1CHS0 (ADC1 Input Channel 0 Select)         AD1CHS123 (ADC1 Input	
PIG       76         PWM (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)         PWM Generator 1 (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)         PWM Generator 2 (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)         PUC24EPXXXMC20X Devices)       80         PWM Generator 3 (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)         PIC24EPXXXMC20X Devices)       80         QEI1 (dsPIC33EPXXMC20X/50X,       PIC24EPXXXMC20X/50X,         PIC24EPXXXMC20X Devices)       81         Reference Clock       93         SPI1 and SPI2       83         System Control       93         Time1 through Time5       75         UART1 and UART2       82         Registers       AD1CHS0 (ADC1 Input Channel 0 Select)       333         AD1CHS123 (ADC1 Input       Channel 1, 2, 3 Select)       331	
PIG       70         PWM (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)       79         PWM Generator 1 (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)       79         PWM Generator 2 (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)       80         PWM Generator 3 (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)       80         PWM Generator 3 (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X Devices)       80         QEI1 (dsPIC33EPXXXMC20X/50X,       PIC24EPXXXMC20X/50X,       81         Reference Clock       93       93       81         Reference Clock       93       93       31         System Control       93       93       333         AD1CHS0 (ADC1 Input Channel 0 Select)       333       333         AD1CHS123 (ADC1 Input       331       AD1CHS123 (ADC1 Input       331         Channel 1, 2, 3 Select)       331       331	
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PIC376PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXMC20X Devices)79PWM Generator 1 (dsPIC33EPXXXMC20X/50X, PIC24EPXXMC20X Devices)79PWM Generator 2 (dsPIC33EPXXXMC20X/50X, PIC24EPXXMC20X Devices)80PWM Generator 3 (dsPIC33EPXXXMC20X/50X, PIC24EPXXXMC20X Devices)80QEI1 (dsPIC33EPXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, PIC24EPXXXMC20X/50X, 	
PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXMC20X Devices)79PWM Generator 1 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)79PWM Generator 2 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)80PWM Generator 3 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)80PWM Generator 3 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)80QEI1 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X/50X, PIC24EPXXMC20X/50X, PIC24EPXXMC20X Devices)81Reference Clock93SPI1 and SPI283System Control93Time1 through Time575UART1 and UART282RegistersAD1CHS0 (ADC1 Input Channel 0 Select)333AD1CHS0 (ADC1 Input Channel 0 Select)331AD1CON1 (ADC1 Control 1)325AD1CON3 (ADC1 Control 2)327AD1CON4 (ADC1 Control 4)330AD1CSSH (ADC1 Input Scan Select High)335	
PWM (dsPIC33EPXXXMC20X/50X, PIC24EPXXMC20X Devices)79PWM Generator 1 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)79PWM Generator 2 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)80PWM Generator 3 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)80PWM Generator 3 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)80QEI1 (dsPIC33EPXXMC20X/50X, PIC24EPXXMC20X Devices)81Reference Clock93SPI1 and SPI283System Control93Time1 through Time575UART1 and UART282RegistersAD1CHS0 (ADC1 Input Channel 1, 2, 3 Select)331AD1CON1 (ADC1 Control 1)325AD1CON2 (ADC1 Control 2)327AD1CON3 (ADC1 Control 3)329AD1CON4 (ADC1 Control 4)330AD1CSSH (ADC1 Input Scan Select High)335AD1CSSL (ADC1 Input Scan Select Low)336	
PIG	
PIG	
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