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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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| Details | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | I ² C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 64KB (22K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 6x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 28-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64gp202-i-so |
| | |

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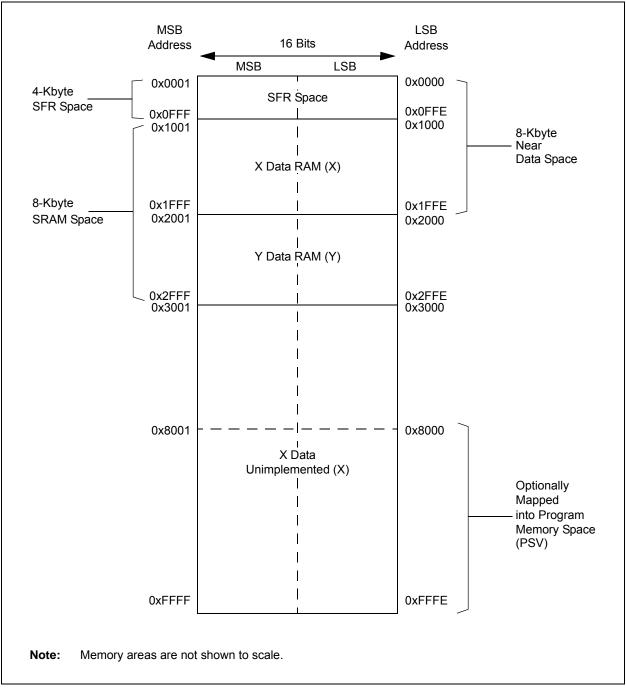
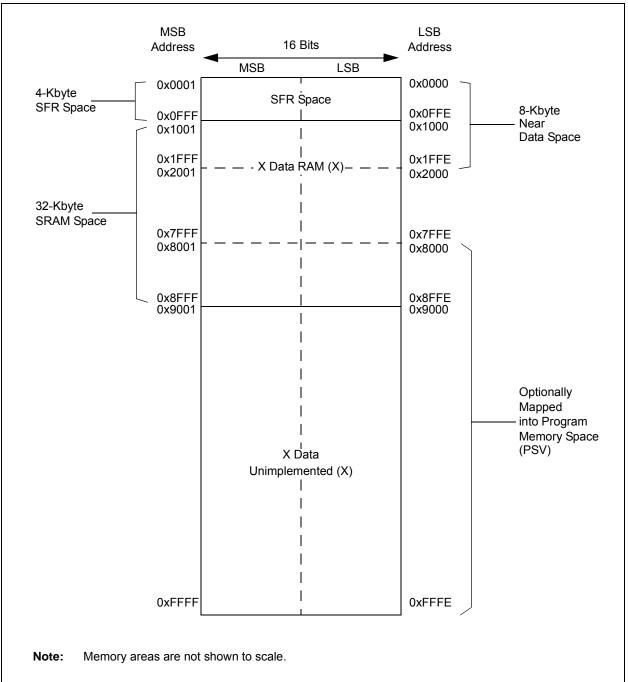


FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP64MC20X/50X AND dsPIC33EP64GP50X DEVICES





| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|--------------|-------|--------|--------|------------|--------|--------|--------|------------|--------|-------|--------|-------------|--------|--------|----------|--------------|---------|---------------|
| IFS0 | 0800 | _ | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INTOIF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | _ | _ | _ | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | _ | | _ | _ | _ | | _ | _ | | IC4IF | IC3IF | DMA3IF | _ | — | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | _ | _ | _ | _ | _ | QEI1IF | PSEMIF | _ | _ | _ | _ | _ | _ | MI2C2IF | SI2C2IF | — | 0000 |
| IFS4 | 0808 | - | _ | CTMUIF | _ | _ | | — | _ | _ | | _ | _ | CRCIF | U2EIF | U1EIF | | 0000 |
| IFS5 | 080A | PWM2IF | PWM1IF | _ | _ | _ | | — | _ | _ | | _ | _ | _ | _ | _ | | 0000 |
| IFS6 | 080C | _ | _ | _ | _ | _ | | — | _ | _ | | _ | _ | _ | _ | _ | PWM3IF | 0000 |
| IFS8 | 0810 | JTAGIF | ICDIF | _ | _ | _ | | — | _ | _ | | _ | _ | _ | _ | _ | _ | 0000 |
| IFS9 | 0812 | _ | _ | _ | | _ | _ | _ | _ | _ | PTG3IF | PTG2IF | PTG1IF | PTG0IF | PTGWDTIF | PTGSTEPIF | | 0000 |
| IEC0 | 0820 | _ | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INTOIE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | — | _ | — | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | _ | _ | — | - | _ | | — | — | _ | IC4IE | IC3IE | DMA3IE | | _ | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | _ | _ | _ | | _ | QEI1IE | PSEMIE | — | _ | _ | — | — | - | MI2C2IE | SI2C2IE | — | 0000 |
| IEC4 | 0828 | _ | _ | CTMUIE | | _ | | — | — | _ | _ | — | _ | CRCIE | U2EIE | U1EIE | | 0000 |
| IEC5 | 082A | PWM2IE | PWM1IE | — | | _ | _ | _ | — | _ | _ | — | _ | | _ | — | | 0000 |
| IEC6 | 082C | _ | _ | _ | | _ | _ | _ | — | _ | _ | — | _ | - | _ | — | PWM3IE | 0000 |
| IEC8 | 0830 | JTAGIE | ICDIE | _ | | _ | _ | _ | — | _ | _ | — | _ | - | _ | — | — | 0000 |
| IEC9 | 0832 | _ | _ | _ | | _ | _ | _ | — | _ | PTG3IE | PTG2IE | PTG1IE | PTG0IE | PTGWDTIE | PTGSTEPIE | | 0000 |
| IPC0 | 0840 | _ | | T1IP<2:0> | | _ | | OC1IP<2:0 |)> | _ | | IC1IP<2:0> | | | | INT0IP<2:0> | | 4444 |
| IPC1 | 0842 | _ | | T2IP<2:0> | | _ | | OC2IP<2:0 |)> | _ | | IC2IP<2:0> | | - | [| DMA0IP<2:0> | | 4444 |
| IPC2 | 0844 | _ | - | U1RXIP<2:0 | > | _ | : | SPI1IP<2:0 |)> | _ | | SPI1EIP<2:0 | > | - | | T3IP<2:0> | | 4444 |
| IPC3 | 0846 | _ | _ | — | — | _ | C | MA1IP<2: | 0> | _ | | AD1IP<2:0> | | - | | U1TXIP<2:0> | | 0444 |
| IPC4 | 0848 | _ | | CNIP<2:0> | | _ | | CMIP<2:0 | > | _ | | MI2C1IP<2:0 | > | - | 5 | SI2C1IP<2:0> | | 4444 |
| IPC5 | 084A | _ | _ | — | — | _ | | — | — | _ | _ | — | — | - | | INT1IP<2:0> | | 0004 |
| IPC6 | 084C | _ | | T4IP<2:0> | | _ | | OC4IP<2:0 |)> | | | OC3IP<2:0> | | | [| DMA2IP<2:0> | | 4444 |
| IPC7 | 084E | _ | | U2TXIP<2:0 | > | _ | ι | J2RXIP<2: | 0> | | | INT2IP<2:0> | • | | | T5IP<2:0> | | 4444 |
| IPC8 | 0850 | _ | _ | — | — | _ | | — | — | _ | | SPI2IP<2:0> | • | - | 5 | SPI2EIP<2:0> | | 0044 |
| IPC9 | 0852 | _ | _ | _ | | _ | | IC4IP<2:0 | > | _ | | IC3IP<2:0> | | - | [| DMA3IP<2:0> | | 0444 |
| IPC12 | 0858 | _ | _ | _ | | _ | N | 112C2IP<2: | 0> | _ | | SI2C2IP<2:0 | > | - | _ | — | | 0440 |
| IPC14 | 085C | _ | _ | _ | _ | _ | (| QEI1IP<2:0 |)> | _ | | PSEMIP<2:0 | > | _ | _ | _ | _ | 0440 |
| IPC16 | 0860 | _ | | CRCIP<2:0 | > | _ | | U2EIP<2:0 | > | _ | | U1EIP<2:0> | | _ | _ | _ | _ | 4440 |
| IPC19 | 0866 | _ | _ | — | — | _ | — | — | _ | _ | | CTMUIP<2:0 | > | _ | _ | _ | _ | 0040 |
| IPC23 | 086E | _ | F | PWM2IP<2:0 |)> | _ | P | WM1IP<2: | 0> | _ | _ | _ | — | _ | _ | _ | _ | 4400 |
| IPC24 | 0870 | _ | _ | | | _ | | _ | | | _ | _ | _ | _ | F | PWM3IP<2:0> | | 4004 |

TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-41: PMD REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|--------------|-------|--------|--------|--------|--------|--------|--------|--------|--------|--------|-------|-------|--------|--------|--------|--------|-------|---------------|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | QEI1MD | PWMMD | — | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | _ | _ | AD1MD | 0000 |
| PMD2 | 0762 | _ | _ | _ | _ | IC4MD | IC3MD | IC2MD | IC1MD | _ | _ | _ | _ | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | _ | _ | — | — | _ | CMPMD | _ | _ | CRCMD | _ | _ | _ | — | — | I2C2MD | _ | 0000 |
| PMD4 | 0766 | _ | | _ | _ | _ | _ | _ | _ | _ | _ | _ | _ | REFOMD | CTMUMD | _ | _ | 0000 |
| PMD6 | 076A | _ | | _ | _ | _ | PWM3MD | PWM2MD | PWM1MD | _ | _ | _ | _ | _ | _ | _ | _ | 0000 |
| | | | | | | | | | | | | | DMA0MD | | | | | |
| PMD7 | 076C | | | | | | | | | | | | DMA1MD | PTGMD | | | | 0000 |
| PIVID7 | 0760 | _ | _ | _ | _ | _ | _ | _ | _ | _ | _ | _ | DMA2MD | FIGMD | _ | _ | _ | 0000 |
| | | | | | | | | | | | | | DMA3MD | | | | | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-52: PORTG REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|--------------|-------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|---------------|
| TRISG | 0E60 | _ | - | _ | _ | - | - | TRISG9 | TRISG8 | TRISG7 | TRISG6 | _ | _ | _ | _ | _ | — | 03C0 |
| PORTG | 0E62 | | | - | _ | _ | _ | RG9 | RG8 | RG7 | RG6 | _ | _ | _ | _ | _ | _ | xxxx |
| LATG | 0E64 | | | - | _ | _ | _ | LATG9 | LATG8 | LATG7 | LATG6 | _ | _ | _ | _ | _ | _ | xxxx |
| ODCG | 0E66 | | | - | _ | _ | _ | ODCG9 | ODCG8 | ODCG7 | ODCG6 | _ | _ | _ | _ | _ | _ | 0000 |
| CNENG | 0E68 | | | - | _ | _ | _ | CNIEG9 | CNIEG8 | CNIEG7 | CNIEG6 | _ | _ | _ | _ | _ | _ | 0000 |
| CNPUG | 0E6A | | | - | _ | _ | _ | CNPUG9 | CNPUG8 | CNPUG7 | CNPUG6 | _ | _ | _ | _ | _ | _ | 0000 |
| CNPDG | 0E6C | _ | _ | _ | _ | | | CNPDG9 | CNPDG8 | CNPDG7 | CNPDG6 | _ | _ | - | _ | _ | | 0000 |

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

| REGISTER 7-5: | INTCON3: INTERRUPT CONTROL REGISTER 3 |
|---------------|---------------------------------------|

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | | |
|--|-------------|-----------------|------------------|------------------|------------------|-----------------|-------|--|--|
| | — | _ | — | — | — | — | _ | | |
| bit 15 | | | | | | • | bit 8 | | |
| | | | | | | | | | |
| U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | | |
| — | — | DAE | DOOVR | — | — | — | — | | |
| bit 7 | | | | | | | bit 0 | | |
| | | | | | | | | | |
| Legend: | | | | | | | | | |
| R = Readab | le bit | W = Writable | bit | U = Unimplei | mented bit, read | as '0' | | | |
| -n = Value a | It POR | '1' = Bit is se | t | '0' = Bit is cle | eared | x = Bit is unkr | nown | | |
| | | | | | | | | | |
| bit 15-6 | Unimplemen | ted: Read as | '0' | | | | | | |
| bit 5 | DAE: DMA A | ddress Error S | Soft Trap Status | s bit | | | | | |
| | 1 = DMA add | ress error soft | trap has occur | red | | | | | |
| | 0 = DMA add | ress error soft | trap has not o | ccurred | | | | | |
| bit 4 | DOOVR: DO | Stack Overflov | v Soft Trap Sta | tus bit | | | | | |
| 1 = DO stack overflow soft trap has occurred | | | | | | | | | |

| I = D0 | Stack Overnow | 3011 11 ap 11 a3 | occurred |
|--------|----------------|------------------|--------------|
| 0 = DO | stack overflow | soft trap has | not occurred |

| bit 3-0 | Unimplemented: Read as '0' |
|---------|----------------------------|
|---------|----------------------------|

REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---------|-----|-----|-----|-----|-----|-----|-------|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | • | | bit 8 |
| | | | | | | | |
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| _ | _ | — | | — | — | — | SGHT |
| bit 7 | | | | | • | | bit 0 |
| | | | | | | | |
| Legend: | | | | | | | |

| 3 | | | |
|-------------------|------------------|------------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, | read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |
| | | | |

bit 0

SGHT: Software Generated Hard Trap Status bit

1 = Software generated hard trap has occurred

0 = Software generated hard trap has not occurred

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---------|-----|-------|-------|-------|-------|-------|-------|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | TUN5 | TUN4 | TUN3 | TUN2 | TUN1 | TUN0 |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |
| Logondi | | | | | | | |

REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER

| Legend: | | | |
|-------------------|------------------|-----------------------|--------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit | , read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-6 Unimplemented: Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits 011111 = Maximum frequency deviation of 1.453% (7.477 MHz) 011110 = Center frequency + 1.406% (7.474 MHz) •••• 000001 = Center frequency + 0.047% (7.373 MHz) 000000 = Center frequency (7.37 MHz nominal) 111111 = Center frequency - 0.047% (7.367 MHz) ••• 100001 = Center frequency - 1.453% (7.263 MHz) 100000 = Minimum frequency deviation of -1.5% (7.259 MHz)

| | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----------------------------------|-------|-----------------|---------------------------------------|--|--|--|
| | | QEIG | EC<31:24> | | | |
| | | | | | | bit 8 |
| | DAM 0 | | | DAMA | DAVO | |
| R/W-U | R/W-U | | | R/W-U | R/W-U | R/W-0 |
| | | QEIGE | EC<23:16> | | | |
| | | | | | | bit (|
| | | | | | | |
| R = Readable bit W = Writable bit | | | U = Unimplem | nented bit, rea | d as '0' | |
| -n = Value at POR | | | '0' = Bit is clea | ared | x = Bit is unkn | iown |
| | | W = Writable bi | R/W-0 R/W-0 QEIGI W = Writable bit | R/W-0 R/W-0 R/W-0 QEIGEC<23:16> W = Writable bit U = Unimplem | R/W-0 R/W-0 R/W-0 QEIGEC<23:16> W = Writable bit U = Unimplemented bit, real | R/W-0 R/W-0 R/W-0 R/W-0 QEIGEC<23:16> U = Unimplemented bit, read as '0' |

REGISTER 17-15: QEI1GECH: QEI1 GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER

bit 15-0 QEIGEC<31:16>: High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 17-16: QEI1GECL: QEI1 GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|------------------------------------|-------|-------|---|---------|-------|-------|-------|
| | | | QEIGE | C<15:8> | | | |
| bit 15 | | | | | | | bit 8 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | | | QEIG | EC<7:0> | | | |
| bit 7 | | | | | | | bit 0 |
| Legend: | | | | | | | |
| R = Readable bit W = Writable bit | | | U = Unimplemented bit, read as '0' | | | | |
| -n = Value at POR '1' = Bit is set | | | '0' = Bit is cleared x = Bit is unknown | | | nown | |

bit 15-0 QEIGEC<15:0>: Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

18.3 SPIx Control Registers

R/W-0 U-0 R/W-0 U-0 R/W-0 R/W-0 R/W-0 U-0 SPIEN SPISIDL SPIBEC<2:0> _____ bit 15 R/W-0 R/W-0 R/W-0 R/C-0, HS R/W-0 R/W-0 R-0, HS, HC R-0, HS, HC SRMPT SPIROV SRXMPT SISEL2 SISEL1 SISEL0 SPITBF SPIRBF bit 7 Legend: C = Clearable bit HS = Hardware Settable bit HC = Hardware Clearable bit R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 SPIEN: SPIx Enable bit 1 = Enables the module and configures SCKx, SDOx, SDIx and \overline{SSx} as serial port pins 0 = Disables the module bit 14 Unimplemented: Read as '0' bit 13 SPISIDL: SPIx Stop in Idle Mode bit 1 = Discontinues the module operation when device enters Idle mode 0 = Continues the module operation in Idle mode bit 12-11 Unimplemented: Read as '0' bit 10-8 SPIBEC<2:0>: SPIx Buffer Element Count bits (valid in Enhanced Buffer mode) Master mode: Number of SPIx transfers that are pending. Slave mode: Number of SPIx transfers that are unread. SRMPT: SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode) bit 7 1 = SPIx Shift register is empty and Ready-To-Send or receive the data 0 = SPIx Shift register is not empty bit 6 SPIROV: SPIx Receive Overflow Flag bit

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register 0 = No overflow has occurred SRXMPT: SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode)

- 1 = RX FIFO is empty
- 0 = RX FIFO is not empty

bit 4-2 SISEL<2:0>: SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)

- 111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set)
 - 110 = Interrupt when last bit is shifted into SPIxSR and as a result, the TX FIFO is empty
 - 101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete
 - 100 = Interrupt when one data is shifted into the SPIxSR and as a result, the TX FIFO has one open memory location
 - 011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set)
 - 010 = Interrupt when the SPIx receive buffer is 3/4 or more full
 - 001 = Interrupt when data is available in the receive buffer (SRMPT bit is set)
 - 000 = Interrupt when the last data in the receive buffer is read and as a result, the buffer is empty (SRXMPT bit is set)

bit 5

bit 8

bit 0

19.0 INTER-INTEGRATED CIRCUIT[™] (I²C[™])

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Inter-Integrated Circuit™ (I²C™)" (DS70330) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.
 - 3: There are minimum bit rates of approximately FCY/512. As a result, high processor speeds may not support 100 Kbit/second operation. See timing specifications, IM10 and IM11, and the "Baud Rate Generator" in the "dsPIC33/PIC24 Family Reference Manual".

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices contains two Inter-Integrated Circuit (I²C) modules: I2C1 and I2C2.

The l^2C module provides complete hardware support for both Slave and Multi-Master modes of the l^2C serial communication standard, with a 16-bit interface.

The I^2C module has a 2-pin interface:

- · The SCLx pin is clock
- The SDAx pin is data

The I²C module offers the following key features:

- I²C interface supporting both Master and Slave modes of operation
- I²C Slave mode supports 7 and 10-bit addressing
- I²C Master mode supports 7 and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation, detects bus collision and arbitrates accordingly
- Intelligent Platform Management Interface (IPMI)
 support
- System Management Bus (SMBus) support

23.2 ADC Helpful Tips

- 1. The SMPIx control bits in the AD1CON2 register:
 - a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
 - b) When the CSCNA bit in the AD1CON2 registers is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
 - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
 - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
- 2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
- 3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
- 4. The DONE bit (AD1CON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (AD1CON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.

5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for ANO, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use AN0-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. Configuration examples are available in the "Analog-to-Digital Converter (ADC)" (DS70621) section in the "dsPIC33/ PIC24 Family Reference Manual".

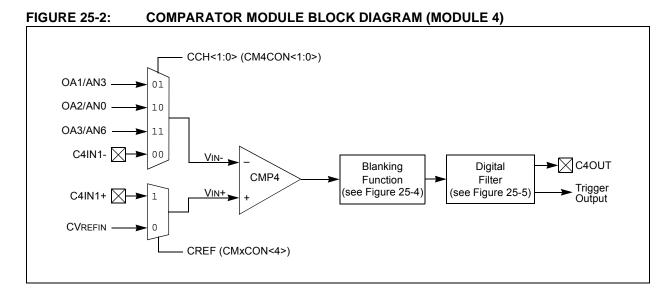
23.3 ADC Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

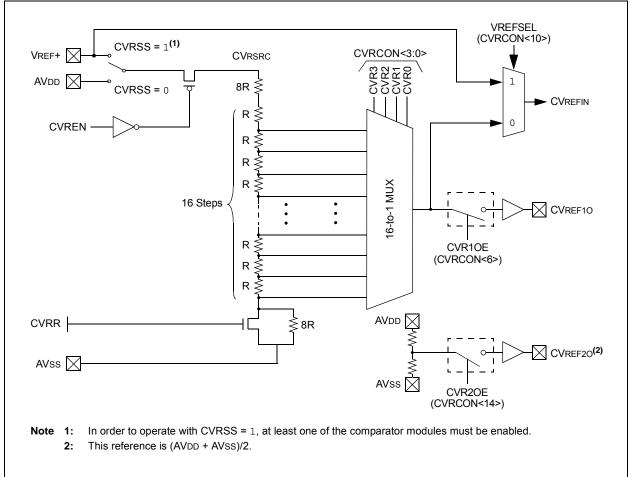
| Note: | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/ |
|-------|---|
| | Devices.aspx?dDocName=en555464 |

23.3.1 KEY RESOURCES

- "Analog-to-Digital Converter (ADC)" (DS70621) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools







REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)

- bit 5 Unimplemented: Read as '0'
- bit 4 **CREF:** Comparator Reference Select bit (VIN+ input)⁽¹⁾
 - 1 = VIN+ input connects to internal CVREFIN voltage
 - 0 = VIN+ input connects to C4IN1+ pin
- bit 3-2 Unimplemented: Read as '0'
- bit 1-0 CCH<1:0>: Comparator Channel Select bits⁽¹⁾
 - 11 = VIN- input of comparator connects to OA3/AN6
 - 10 = VIN- input of comparator connects to OA2/AN0
 - 01 = VIN- input of comparator connects to OA1/AN3
 - 00 = VIN- input of comparator connects to C4IN1-
- Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.



| TABLE 30-23: TIME | 1 EXTERNAL CLOCK TIMING REQUI | REMENTS ⁽¹⁾ |
|-------------------|-------------------------------|------------------------|
|-------------------|-------------------------------|------------------------|

| AC CHARACTERISTICS | | | $\begin{tabular}{lllllllllllllllllllllllllllllllllll$ | | | | for Industrial | |
|--------------------|-----------|--|---|--|------|---------------|----------------|---|
| Param No. | Symbol | Charao | cteristic ⁽²⁾ | Min. | Тур. | Max. | Units | Conditions |
| TA10 | ТтхН | T1CK High Time | Synchronous mode | Greater of: 20 or (Tcy + 20)/N | | _ | ns | Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256) |
| | | | Asynchronous | 35 | _ | — | ns | |
| TA11 | ΤτχL | T1CK Low Time | Synchronous mode | Greater of: 20 or (Tcy + 20)/N | | _ | ns | Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256) |
| | | | Asynchronous | 10 | _ | _ | ns | |
| TA15 | ΤτχΡ | T1CK Input Period | Synchronous mode | Greater of: 40 or (2 Tcy + 40)/N | _ | _ | ns | N = prescale value (1, 8, 64, 256) |
| OS60 | Ft1 | T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON<1>)) | | DC | | 50 | kHz | |
| TA20 | TCKEXTMRL | Delay from E Clock Edge t Increment | xternal T1CK o Timer | 0.75 Tcy + 40 | — | 1.75 Tcy + 40 | ns | |

Note 1: Timer1 is a Type A.

2: These parameters are characterized, but are not tested in manufacturing.

TABLE 30-46:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS

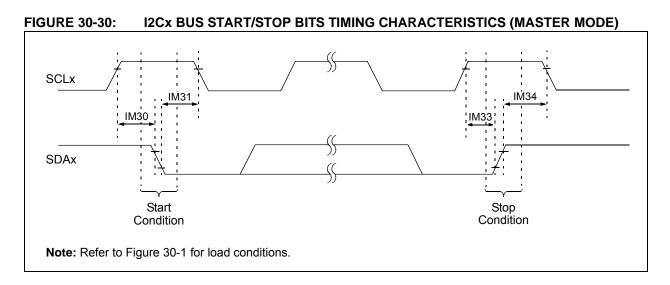
| AC CHARACTERISTICS | | | Standard Op (unless othe Operating ter | erwise st | ated) ⁻ e -40°C | \leq Ta \leq +8 | o 3.6V 85°C for Industrial 125°C for Extended |
|--------------------|-----------------------|---|--|---------------------|--------------------------------------|---------------------|--|
| Param. | Symbol | Characteristic ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Units | Conditions |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | _ | Lesser of FP or 11 | MHz | (Note 3) |
| SP72 | TscF | SCK1 Input Fall Time | _ | _ | _ | ns | See Parameter DO32 (Note 4) |
| SP73 | TscR | SCK1 Input Rise Time | — | _ | _ | ns | See Parameter DO31 (Note 4) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (Note 4) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | _ | — | ns | See Parameter DO31 (Note 4) |
| SP35 | TscH2doV, TscL2doV | SDO1 Data Output Valid after SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | _ | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | SS1 ↑ to SDO1 Output High-Impedance | 10 | — | 50 | ns | (Note 4) |
| SP52 | TscH2ssH, TscL2ssH | SS1 ↑ after SCK1 Edge | 1.5 Tcy + 40 | _ | _ | ns | (Note 4) |
| SP60 | TssL2doV | SDO1 Data Output Valid after | — | — | 50 | ns | |

Note 1: These parameters are characterized, but are not tested in manufacturing.

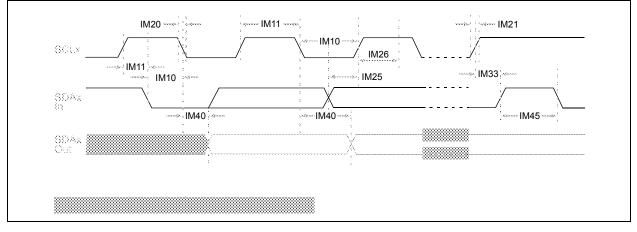
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

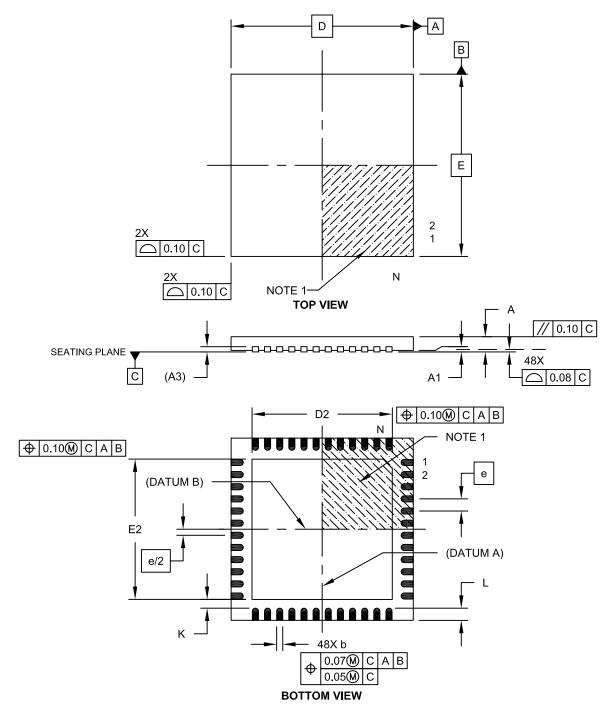
4: Assumes 50 pF load on all SPI1 pins.







NOTES:



48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing C04-153A Sheet 1 of 2

Ρ

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