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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

⊡XFI

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64gp202t-e-mm

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3.8 Arithmetic Logic Unit (ALU)

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X ALU is 16 bits wide, and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the <u>SR register. The C and DC</u> Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned DIV instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.9 DSP Engine (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulatorto-accumulator operations that require no additional data. These instructions are ADD, SUB and NEG.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- · Signed, unsigned or mixed-sign DSP multiply (US)
- · Conventional or convergent rounding (RND)
- · Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

	SOMMAN	
Instruction	Algebraic Operation	ACC Write Back
CLR	A = 0	Yes
ED	$A = (x - y)^2$	No
EDAC	$A = A + (x - y)^2$	No
MAC	$A = A + (x \bullet y)$	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	$A = x \bullet y$	No
MPY	$A = x^2$	No
MPY.N	$A = -x \bullet y$	No
MSC	$A = A - x \bullet y$	Yes

TABLE 3-2: DSP INSTRUCTIONS SUMMARY





SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100								Timer1	Register								xxxx
PR1	0102								Period F	Register 1								FFFF
T1CON	0104	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKP	S<1:0>	_	TSYNC	TCS	—	0000
TMR2	0106								Timer2	Register								xxxx
TMR3HLD	0108						Time	er3 Holding	Register (fo	r 32-bit time	r operations	only)						xxxx
TMR3	010A								Timer3	Register								xxxx
PR2	010C		Period Register 2 FFFF										FFFF					
PR3	010E								Period F	Register 3								FFFF
T2CON	0110	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKP	S<1:0>	T32	_	TCS	—	0000
T3CON	0112	TON	_	TSIDL	_	_	_	_	_	_	TGATE	TCKP	S<1:0>	_	_	TCS	—	0000
TMR4	0114								Timer4	Register								xxxx
TMR5HLD	0116						Т	imer5 Holdii	ng Register	(for 32-bit o	perations on	ly)						xxxx
TMR5	0118								Timer5	Register								xxxx
PR4	011A	Period Register 4										FFFF						
PR5	011C	Period Register 5 FFF										FFFF						
T4CON	011E	TON	_	TSIDL	_	—	—	_	_	_	TGATE	TCKP	S<1:0>	T32	—	TCS	—	0000
T5CON	0120	TON		TSIDL	—	—	—	_	_	_	TGATE	TCKP	S<1:0>	—	_	TCS	—	0000

TABLE 4-8: TIMER1 THROUGH TIMER5 REGISTER MAP

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-53: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00		—	—			TRISA10	TRISA9	TRISA8	TRISA7			TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
PORTA	0E02		—	_			RA10	RA9	RA8	RA7			RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04		—	—	-	-	LATA10	LATA9	LATA8	LATA7	_	-	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	_	_	ODCA10	ODCA9	ODCA8	ODCA7	_	_	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08		—	—			CNIEA10	CNIEA9	CNIEA8	CNIEA7			CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	_	_	CNPUA10	CNPUA9	CNPUA8	CNPUA7	_	_	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	_	_	_	_	_	CNPDA10	CNPDA9	CNPDA8	CNPDA7	_	_	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E	_	_	_	_	_	_	_	_	_	_	_	ANSA4	_	_	ANSA1	ANSA0	0013

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	-	—	—	—	—	—	—	ANSB8	-	—	-	_	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-55: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	—	—	—	—	-	TRISC9	TRISC8	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	03FF
PORTC	0E22	—	_	—	—	—		RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx
LATC	0E24	—	—	—	—	—		LATC9	LATC8	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx
ODCC	0E26	_	_	_	_	_	_	ODCC9	ODCC8	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000
CNENC	0E28	—	—	—	—	—	-	CNIEC9	CNIEC8	CNIEC7	CNIEC6	CNIEC5	CNIEC4	CNIEC3	CNIEC2	CNIEC1	CNIEC0	0000
CNPUC	0E2A	_	_	_	_	_	_	CNPUC9	CNPUC8	CNPUC7	CNPUC6	CNPUC5	CNPUC4	CNPUC3	CNPUC2	CNPUC1	CNPUC0	0000
CNPDC	0E2C	_	_	_	_	_	_	CNPDC9	CNPDC8	CNPDC7	CNPDC6	CNPDC5	CNPDC4	CNPDC3	CNPDC2	CNPDC1	CNPDC0	0000
ANSELC	0E2E	_	_	_	_	_	_	_		_		_	_	_	ANSC2	ANSC1	ANSC0	0007

Legend: x = unknown value on Reset, --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-56: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00			—			—		TRISA8				TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	011F
PORTA	0E02		-	—	-	-	—	-	RA8	_	_	-	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	_	_	_	_	_	_	_	LATA8	_	_	_	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	_	_	_	_	ODCA8	_	_	_	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	_	_	_	_	_	_	_	CNIEA8	_	_	_	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	_	_	_	_	CNPUA8	_	_	_	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	_	_	_	_	_	_	_	CNPDA8	_	_	_	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E			—			—		_	_			ANSA4		-	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-57: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	_	_	_	_	_	_	_	ANSB8	_	_	_	_	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-58: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	_	—	_	—	—	—	TRISC8	_	—	—	—	—	—	TRISC1	TRISC0	0103
PORTC	0E22	—	_	—	_	_	_	_	RC8		—	_	_	_	_	RC1	RC0	xxxx
LATC	0E24	—	_	—	_	—	—	—	LATC8		_	—	—	—	_	LATC1	LATC0	xxxx
ODCC	0E26	—	_	—	_	—	—	—	ODCC8		_	—	—	—	_	ODCC1	ODCC0	0000
CNENC	0E28	—	_	—	_	—	—	—	CNIEC8		_	—	—	—	_	CNIEC1	CNIEC0	0000
CNPUC	0E2A	—	_	—	_	—	—	—	CNPUC8		_	—	—	—	_	CNPUC1	CNPUC0	0000
CNPDC	0E2C	—	_	—	_	—	—	—	CNPDC8		_	—	—	—	_	CNPDC1	CNPDC0	0000
ANSELC	0E2E	_	_	_	_	_	_	_	_	_	_	_	_	_		ANSC1	ANSC0	0003

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE2 ⁽¹⁾	DOZE1 ⁽¹⁾	DOZE0 ⁽¹⁾	DOZEN ^(2,3)	FRCDIV2	FRCDIV1	FRCDIV0
bit 15							bit 8
R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOST	1 PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0
bit 7							bit 0
Legend:						<i>(</i> -)	
R = Readat	ble bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	IOWN
bit 1E		on Interrupt b	.+				
	1 = Interrunte	will clear the	NOZEN bit				
	0 = Interrupts	s have no effect	t on the DOZE	EN bit			
bit 14-12	DOZE<2:0>:	Processor Clo	ck Reduction S	Select bits ⁽¹⁾			
	111 = Fcy div	vided by 128					
	110 = Fcy div	vided by 64					
	101 = FCY div 100 = FCY div	/ided by 32					
	011 = FCY div	vided by 8 (defa	ault)				
	010 = FCY div	vided by 4					
	001 = FCY div	/ided by 2					
bit 11		e Mode Enable	. _{hit} (2,3)				
	1 = DOZER. DOZE < 2:0	0> field specifi	es the ratio be	tween the peri	pheral clocks a	nd the process	or clocks
	0 = Processor	r clock and per	ipheral clock r	atio is forced t	o 1:1		
bit 10-8	FRCDIV<2:0>	Internal Fast	RC Oscillator	Postscaler bit	S		
	111 = FRC di	vided by 256					
	110 = FRC di	vided by 64					
	100 = FRC d i	vided by 32 vided by 16					
	011 = FRC di	vided by 8					
	010 = FRC di	vided by 4					
	001 = FRC di 000 = FRC di	vided by 2 vided by 1 (de	fault)				
bit 7-6	PLLPOST<1:	0>: PLL VCO	Output Divider	r Select bits (al	so denoted as '	N2', PLL posts	caler)
	11 = Output d	livided by 8	,	,		<i>,</i> ,	,
	10 = Reserve	d					
	01 = Output d	livided by 4 (de	etault)				
bit 5	Unimplement	ted: Read as '	0'				
Sito	emplement		•				
Note 1:	The DOZE<2:0> bi DOZE<2:0> are igi	its can only be nored.	written to whe	en the DOZEN	bit is clear. If D	OZEN = 1, any	writes to
2:	This bit is cleared v	when the ROI I	oit is set and a	an interrupt occ	urs.		

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER

The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

13.2 Timer Control Registers

R/M/ 0	11.0		11.0	11.0	11.0	11.0	11.0				
	0-0		0-0	0-0	0-0	0-0	0-0				
bit 15		TOIDE	_								
51115							bit 0				
U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0				
	TGATE	TCKPS1	TCKPS0	T32	_	TCS	_				
bit 7							bit 0				
Legend:											
R = Readable I	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'					
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	iown				
bit 15	When T32 = 1 1 = Starts 32-1 0 = Stops 32-1 When T32 = 0 1 = Starts 16-1 0 = Stops 16-1	On bit L: bit Timerx/y bit Timerx/y <u>):</u> bit Timerx bit Timerx									
bit 14	Unimplement	ted: Read as 'd)'								
bit 13	TSIDL: Timer	x Stop in Idle M	lode bit								
	1 = Discontinu 0 = Continues	ues module opera	eration when o tion in Idle mo	device enters I ode	dle mode						
bit 12-7	Unimplement	ted: Read as '	י)								
bit 6	TGATE: Time When TCS = This bit is igno When TCS = 1 = Gated tim 0 = Gated tim	rx Gated Time <u>1:</u> pred. <u>0:</u> e accumulatior e accumulatior	Accumulation	Enable bit							
bit 5-4	TCKPS<1:0>	: Timerx Input (Clock Prescal	e Select bits							
	11 = 1:256 10 = 1:64 01 = 1:8 00 = 1:1										
bit 3	T32: 32-Bit Timer Mode Select bit 1 = Timerx and Timery form a single 32-bit timer 0 = Timerx and Timery act as two 16-bit timers										
bit 2	Unimplement	ted: Read as 'o	י)								
bit 1	TCS: Timerx Clock Source Select bit 1 = External clock is from pin, TxCK (on the rising edge) 0 = Internal clock (FP)										
bit 0	Unimplement	ted: Read as ')'								

REGISTER 13-1: TxCON: (TIMER2 AND TIMER4) CONTROL REGISTER

NOTES:

REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 7-	6	DTC<1:0>: Dead-Time Control bits
		11 = Dead-Time Compensation mode
		10 = Dead-time function is disabled
		01 = Negative dead time is actively applied for Complementary Output mode
		00 = Positive dead time is actively applied for all output modes
bit 5		DTCP: Dead-Time Compensation Polarity bit ⁽³⁾
		When Set to '1':
		If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened.
		II DI CMPX = 1, PWWXH IS SNOTENED and PWWXL IS lengthened.
		When Set to 0.2. If DTCMPx = 0. PW/MxH is shortened and PW/MxL is lengthened
		If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.
bit 4		Unimplemented: Read as '0'
bit 3		MTBS: Master Time Base Select bit
		1 = PWM generator uses the secondary master time base for synchronization and as the clock source
		for the PWM generation logic (if secondary time base is available)
		0 = PWM generator uses the primary master time base for synchronization and as the clock source
		for the PWM generation logic
bit 2		CAM: Center-Aligned Mode Enable bit ^(2,4)
		1 = Center-Aligned mode is enabled
		0 = Edge-Aligned mode is enabled
bit 1		XPRES: External PWMx Reset Control bit ⁽⁵⁾
		 1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
		0 = External pins do not affect PWMx time base
bit 0		IUE: Immediate Update Enable bit ⁽²⁾
		1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate
		 Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary
Note	1:	Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
	2:	These bits should not be changed after the PWMx is enabled (PTEN = 1).
	3:	DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
	4:	The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.

5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	_	_	
bit 15	1		1		1		bit 8	
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	BCH(")	BCL	BPHH	BPHL	BPLH	BPLL	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown	
bit 15	PHR: PWMxH	Rising Edge	Trigger Enabl	e bit				
	\perp = Rising edg 0 = Leading-E	ge of PyvivixH v Edge Blanking i	anores risina	edge of PWM	anking counter kH			
bit 14	PHF: PWMxH	Falling Edge	Trigger Enabl	e bit				
	1 = Falling ed	ge of PWMxH	will trigger Le	ading-Edge Bla	anking counter			
	0 = Leading-E	Edge Blanking i	gnores falling	g edge of PWM	хH			
bit 13	PLR: PWMxL	. Rising Edge T	rigger Enable	e bit oding Edgo Blo	nking countor			
	0 = Leading-E	Edge Blanking i	gnores rising	edge of PWM	kL			
bit 12	PLF: PWMxL	Falling Edge T	rigger Enable	e bit				
	1 = Falling ed	ge of PWMxL	will trigger Le	ading-Edge Bla	anking counter			
	0 = Leading-E	Edge Blanking i	gnores falling	g edge of PWM	xL			
bit 11	1 = Leading-F	-ault Input Lea Edge Blanking i	ding-Edge Bla	anking Enable	bit			
	0 = Leading-E	Edge Blanking i	s not applied	to selected Fa	ult input			
bit 10	CLLEBEN: C	urrent-Limit Le	ading-Edge E	Blanking Enable	e bit			
	1 = Leading-E	Edge Blanking i	s applied to s	selected curren	t-limit input			
hit 0.6	0 = Leading-E	tode Blanking I	s not applied	to selected cul	rrent-limit input			
bit 5	BCH Blankin	a in Selected F	J Blanking Sign	al High Enable	hit(1)			
bit 5	1 = State blan	kina (of curren	t-limit and/or	Fault input sigr	nals) when seled	ted blanking s	ianal is hiah	
	0 = No blankii	ng when select	ed blanking s	signal is high	,	5	0 0	
bit 4	BCL: Blanking	g in Selected B	lanking Signa	al Low Enable I	bit ⁽¹⁾			
	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when seled	cted blanking s	ignal is low	
bit 3	BPHH: Blanki	ing in PWMxH	High Enable	hit				
bit o	1 = State blan	iking (of curren	t-limit and/or	Fault input sigr	nals) when PWN	/IxH output is h	igh	
	0 = No blanki	ng when PWM	xH output is h	nigh			-	
bit 2	BPHL: Blanki	ng in PWMxH	Low Enable b	pit				
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xH output is le	Fault input sigr ow	nals) when PWN	IxH output is lo	W	
bit 1	BPLH: Blanki	ng in PWMxL I	High Enable b	oit				
	1 = State blan 0 = No blankii	nking (of curren ng when PWM	t-limit and/or xL output is h	Fault input sigr igh	nals) when PWN	/IxL output is hi	igh	
bit 0	BPLL: Blanki	ng in PWMxL L	ow Enable b	it				
	1 = State blan	king (of curren	t-limit and/or	Fault input sigr	nals) when PWN	IxL output is lo	W	
	v = i N o diankii		x∟ output is io	JVV				

REGISTER 16-16: LEBCONX: PWMx LEADING-EDGE BLANKING CONTROL REGISTER

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 17-13: QEI1LECH: QEI1 LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILE	C<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILE	C<23:16>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown			nown				

bit 15-0 **QEILEC<31:16>:** High Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

REGISTER 17-14: QEI1LECL: QEI1 LESS THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILE	C<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEILI	EC<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'							
-n = Value at POR '1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown		
~							

bit 15-0 QEILEC<15:0>: Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "UART" (DS70582) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X family of devices contains two UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins, and also includes an IrDA[®] encoder and decoder.

Note: <u>Hardware</u> flow control using UxRTS and UxCTS is not available on all pin count devices. See the "**Pin Diagrams**" section for availability.

The primary features of the UARTx module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with UxCTS and UxRTS Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- · Transmit and Receive Interrupts
- A Separate Interrupt for all UARTx Error Conditions
- · Loopback mode for Diagnostic Support
- · Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA[®] Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UARTx module is shown in Figure 20-1. The UARTx module consists of these key hardware elements:

- · Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

FIGURE 20-1: UARTx SIMPLIFIED BLOCK DIAGRAM



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BUFFER 21-7: ECAN™ MESSAGE BUFFER WORD 6

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Ву	te 7			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			By	te 6			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplement			nented bit, read	l as '0'			
-n = Value at POR '1' = Bit is set '0' = Bit		'0' = Bit is cle	ared	x = Bit is unkr	iown		

bit 15-8 Byte 7<15:8>: ECAN Message Byte 7 bits

bit 7-0 Byte 6<7:0>: ECAN Message Byte 6 bits

BUFFER 21-8: ECAN[™] MESSAGE BUFFER WORD 7

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	_	FILHIT4 ⁽¹⁾	FILHIT3 ⁽¹⁾	FILHIT2 ⁽¹⁾	FILHIT1 ⁽¹⁾	FILHITO ⁽¹⁾
bit 15	- -						bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—		_	_		—	—
bit 7							bit 0
Legend:							

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12-8	FILHIT<4:0>: Filter Hit Code bits ⁽¹⁾
	Encodes number of filter that resulted in writing this buffer.
bit 7-0	Unimplemented: Read as '0'

Note 1: Only written by module for receive buffers, unused for transmit buffers.

22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Charge Time Measurement Unit (CTMU)" (DS70661) in the "dsPIC33/PIC24 Family Reference Manual", which is available on the Microchip web site (www.microchip.com).
 - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Charge Time Measurement Unit is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Four Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edges
- · Precise Time Measurement Resolution of 1 ns
- Accurate Current Source Suitable for Capacitive Measurement
- On-Chip Temperature Measurement using a Built-in Diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_				—		
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0
bit 7							bit 0
Logondi							
R = Reada	able hit	W = Writable	hit	= Inimpler	mented hit read	ae 'O'	
-n = Value	at POR	(1) = Rit is set	bit	'0' = Bit is cle	ared	x = Rit is unkr	nown
II Value		1 Bit lo oot					
bit 15-7	Unimplemen	nted: Read as '	0'				
bit 6-4	CFSEL<2:0>	Comparator I	-ilter Input Clo	ck Select bits			
	111 = T5CLK	(1) (1)					
	110 = T4CLK	< ⁽²⁾					
	101 = T3CLK	<(1) <(2)					
	100 = 12CLP	ved					
	010 = SYNC	01 ⁽³⁾					
	001 = Fosc ⁽⁴	4)					
	000 = FP ⁽⁴⁾						
bit 3	CFLTREN: C	Comparator Filte	er Enable bit				
	1 = Digital filt	er is enabled					
hit 2-0		Comparator F	ilter Clock Div	ide Select hits			
511 2-0	111 = Clock	Divide 1.128					
	110 = Clock	Divide 1:64					
	101 = Clock Divide 1:32						
	100 = Clock	100 = Clock Divide 1:16					
	011 = Clock	Divide 1:8					
	001 = Clock	Divide 1:2					
	000 = Clock	Divide 1:1					
Note 1:	See the Type C Ti	mer Block Diac	ram (Figure 1	3-2).			
2:	See the Type B Tir	e the Type B Timer Block Diagram (Figure 13-1).					

REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER

- 3: See the High-Speed PWMx Module Register Interconnection Diagram (Figure 16-2).
 - 4: See the Oscillator System Diagram (Figure 9-1).

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss ⁽³⁾	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 3.0V^{(3)}$	0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $VDD < 3.0V^{(3)}$	-0.3V to +3.6V
Maximum current out of Vss pin	
Maximum current into VDD pin ⁽²⁾	
Maximum current sunk/sourced by any 4x I/O pin	
Maximum current sunk/sourced by any 8x I/O pin	25 mA
Maximum current sunk by all ports ^(2,4)	200 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).
 - 3: See the "Pin Diagrams" section for the 5V tolerant pins.
 - 4: Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

FIGURE 30-6: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS



TABLE 30-26: INPUT CAPTURE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operati (unless otherwise Operating temperation	ng Con e stated ature	ditions:) -40°C ≤ -40°C ≤	3.0V to 3.6V TA \leq +85°C for Indu TA \leq +125°C for Ext	strial ended		
Param. No. Symbol Characteristics ⁽¹⁾			Min.	Max.	Units	its Conditions		
IC10	TccL	ICx Input Low Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15		
IC11	ТссН	ICx Input High Time	Greater of 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15	N = prescale value (1, 4, 16)	
IC15	TccP	ICx Input Period	Greater of 25 + 50 or (1 Tcy/N) + 50	_	ns			

Note 1: These parameters are characterized, but not tested in manufacturing.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

TABLE 31-11: INTERNAL RC ACCURACY

AC CH	ARACTERISTICS	Standar Operatir	d Operating temper	i ng Con o ature -	ditions: 3 40°C ≤ T	8.0V to 3.6V (unless otherwise stated) $A \le +150^{\circ}C$
Param No.	Characteristic	Min Typ Max Units Conditions				
	LPRC @ 32.768 kHz ^(1,2)					
HF21	LPRC	-30	_	+30	%	$-40^{\circ}C \le TA \le +150^{\circ}C VDD = 3.0-3.6V$

Note 1: Change of LPRC frequency as VDD changes.

2: LPRC accuracy impacts the Watchdog Timer Time-out Period (TwDT). See Section 27.5 "Watchdog Timer (WDT)" for more information.

Revision C (December 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see Section 20.1 "UART Helpful Tips" and Section 3.6 "CPU Resources". All occurrences of TLA were updated to VTLA throughout the document, with the exception of the pin diagrams (updated diagrams were not available at time of publication).

A new chapter, Section 31.0 "DC and AC Device Characteristics Graphs", was added.

All other major changes are referenced by their respective section in Table A-2.

Section Name	Update Description
"16-bit Microcontrollers and Digital Signal Controllers (up to 256-Kbyte Flash and 32-Kbyte SRAM) with High- Speed PWM, Op amps, and Advanced Analog"	The content on the first page of this section was extensively reworked to provide the reader with the key features and functionality of this device family in an "at-a-glance" format.
Section 1.0 "Device Overview"	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X Block Diagram (see Figure 1-1), which now contains a CPU block and a reference to the CPU diagram. Updated the description and Note references in the Pinout I/O Descriptions for these pins: C1IN2- C2IN2- C3IN2- OA1OUT OA2OUT and OA3OUT (see Table 1-1)
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"	Updated the Recommended Minimum Connection diagram (see Figure 2-1).
Section 3.0 "CPU"	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X CPU Block Diagram (see Figure 3-1). Updated the Status register definition in the Programmer's Model (see Figure 3-2).
Section 4.0 "Memory Organization"	Updated the Data Memory Maps (see Figure 4-6 and Figure 4-11). Removed the DCB<1:0> bits from the OC1CON2, OC2CON2, OC3CON2, and OC4CON2 registers in the Output Compare 1 Through Output Compare 4 Register Map (see Table 4-10). Added the TRIG1 and TRGCON1 registers to the PWM Generator 1 Register Map (see Table 4-13). Added the TRIG2 and TRGCON2 registers to the PWM Generator 2 Register Map (see Table 4-14). Added the TRIG3 and TRGCON3 registers to the PWM Generator 3 Register Map (see Table 4-15). Updated the second note in Section 4.7.1 "Bit-Reversed Addressing Implementation".
Section 8.0 "Direct Memory Access (DMA)"	Updated the DMA Controller diagram (see Figure 8-1).
Section 14.0 "Input Capture"	Updated the bit values for the ICx clock source of the ICTSEL<12:10> bits in the ICxCON1 register (see Register 14-1).
Section 15.0 "Output Compare"	Updated the bit values for the OCx clock source of the OCTSEL<2:0> bits in the OCxCON1 register (see Register 15-1). Removed the DCB<1:0> bits from the Output Compare x Control Register 2 (see Register 15-2).

TABLE A-2: MAJOR SECTION UPDATES

Revision F (November 2012)

Removed "Preliminary" from data sheet footer.

Revision G (March 2013)

This revision includes the following global changes:

- changes "FLTx" pin function to "FLTx" on all occurrences
- adds Section 31.0 "High-Temperature Electrical Characteristics" for high-temperature (+150°C) data

This revision also includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-5.

Section Name	Update Description
Cover Section	 Changes internal oscillator specification to 1.0% Changes I/O sink/source values to 12 mA or 6 mA Corrects 44-pin VTLA pin diagram (pin 32 now shows as 5V tolerant)
Section 4.0 "Memory Organization"	 Deletes references to Configuration Shadow registers Corrects the spelling of the JTAGIP and PTGWDTIP bits throughout Corrects the Reset value of all IOCON registers as C000h Adds footnote to Table 4-42 to indicate the absence of Comparator 3 in 28-pin devices
Section 6.0 "Resets"	 Removes references to cold and warm Resets, and clarifies the initial configuration of the device clock source on all Resets
Section 7.0 "Interrupt Controller"	Corrects the definition of GIE as "Global Interrupt Enable" (not "General")
Section 9.0 "Oscillator Configuration"	 Clarifies the behavior of the CF bit when cleared in software Removes POR behavior footnotes from all control registers Corrects the tuning range of the TUN<5:0> bits in Register 9-4 to an overall range ±1.5%
Section 13.0 "Timer2/3 and Timer4/5"	Clarifies the presence of the ADC Trigger in 16-bit Timer3 and Timer5, as well as the 32-bit timers
Section 15.0 "Output Compare"	Corrects the first trigger source for SYNCSEL<4:0> (OCxCON2<4:0>) as OCxRS match
Section 16.0 "High-Speed PWM Module"	 Clarifies the source of the PWM interrupts in Figure 16-1 Corrects the Reset states of IOCONx<15:14> in Register 16-13 as '11'
Section 17.0 "Quadrature Encoder Interface (QEI) Module"	 Clarifies the operation of the IMV<1:0> bits (QEICON<9:8>) with updated text and additional notes Corrects the first prescaler value for QFVDIV<2:0> (QEI10C<13:11>), now 1:128
Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)"	 Adds note to Figure 23-1 that Op Amp 3 is not available in 28-pin devices Changes "sample clock" to "sample trigger" in AD1CON1 (Register 23-1) Clarifies footnotes on op amp usage in Registers 23-5 and 23-6
Section 25.0 "Op Amp/ Comparator Module"	 Adds Note text to indicate that Comparator 3 is unavailable in 28-pin devices Splits Figure 25-1 into two figures for clearer presentation (Figure 25-1 for Op amp/ Comparators 1 through 3, Figure 25-2 for Comparator 4). Subsequent figures are renumbered accordingly. Corrects reference description in xxxxx (now (AVDD+AVss)/2) Changes CMSTAT<15> in Register 25-1 to "PSIDL"
Section 27.0 "Special Features"	Corrects the addresses of all Configuration bytes for 512 Kbyte devices

TABLE A-5: MAJOR SECTION UPDATES