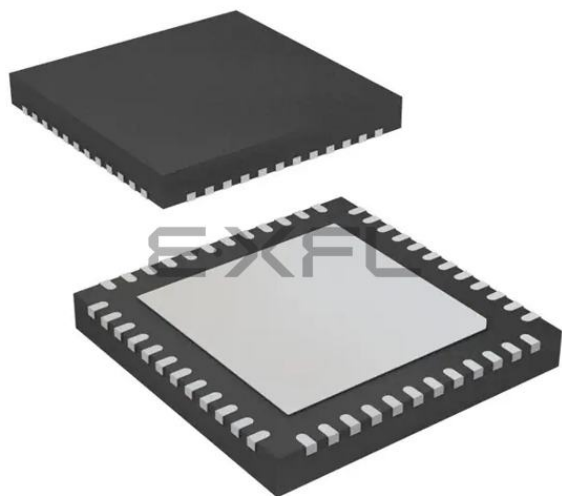




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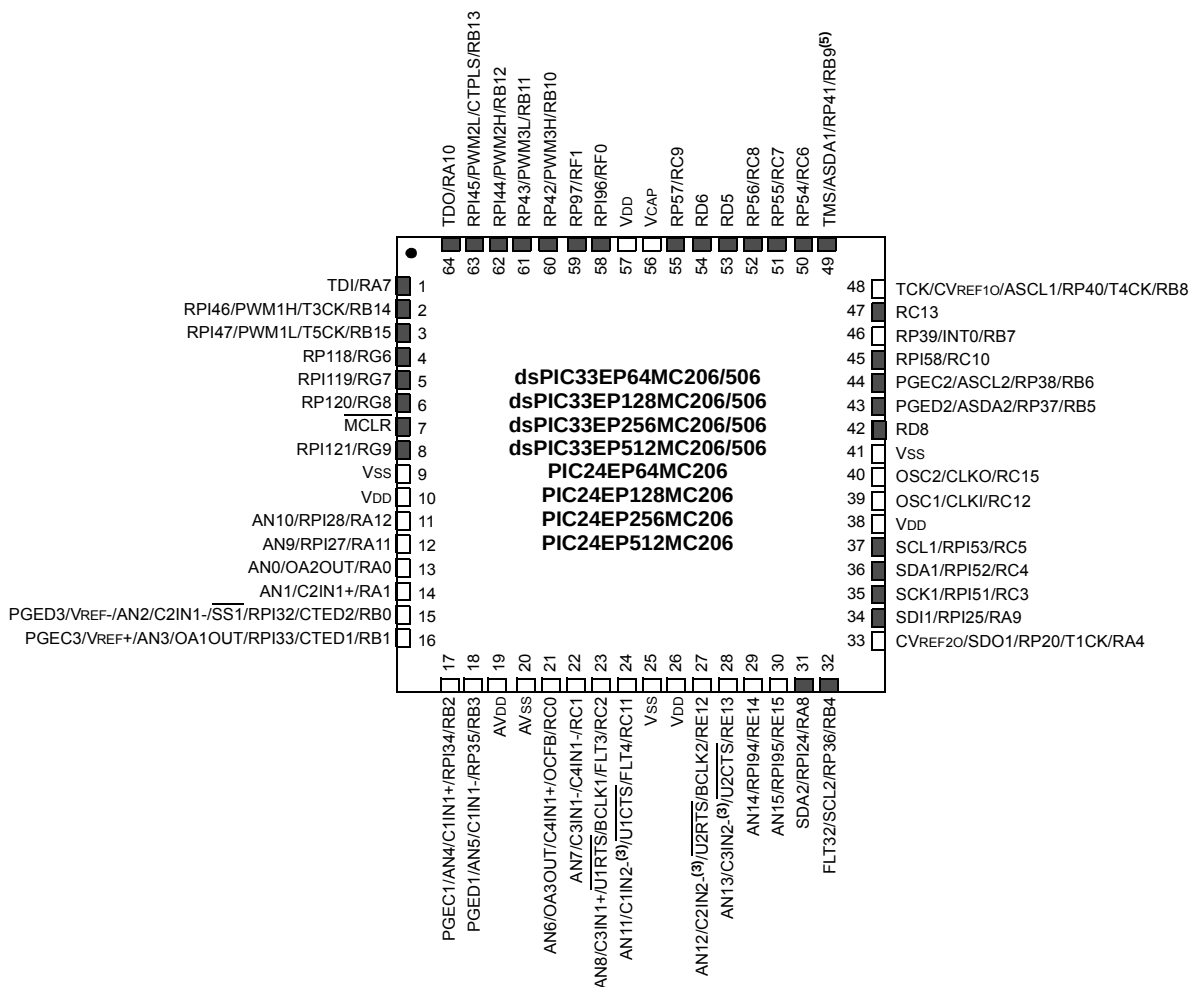
Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64gp204-i-mv

Pin Diagrams (Continued)

64-Pin QFN^(1,2,3,4)

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
 - 3: This pin is not available as an input when OPMODE (CMxCON<10>) = 1.
 - 4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
 - 5: There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

Table of Contents

1.0	Device Overview	25
2.0	Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers	29
3.0	CPU	35
4.0	Memory Organization	45
5.0	Flash Program Memory	119
6.0	Resets	123
7.0	Interrupt Controller	127
8.0	Direct Memory Access (DMA)	139
9.0	Oscillator Configuration	153
10.0	Power-Saving Features	163
11.0	I/O Ports	173
12.0	Timer1	203
13.0	Timer2/3 and Timer4/5	207
14.0	Input Capture	213
15.0	Output Compare	219
16.0	High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)	225
17.0	Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)	249
18.0	Serial Peripheral Interface (SPI)	265
19.0	Inter-Integrated Circuit™ (I ² C™)	273
20.0	Universal Asynchronous Receiver Transmitter (UART)	281
21.0	Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)	287
22.0	Charge Time Measurement Unit (CTMU)	315
23.0	10-Bit/12-Bit Analog-to-Digital Converter (ADC)	321
24.0	Peripheral Trigger Generator (PTG) Module	337
25.0	Op Amp/Comparator Module	355
26.0	Programmable Cyclic Redundancy Check (CRC) Generator	373
27.0	Special Features	379
28.0	Instruction Set Summary	387
29.0	Development Support	397
30.0	Electrical Characteristics	401
31.0	High-Temperature Electrical Characteristics	467
32.0	DC and AC Device Characteristics Graphs	475
33.0	Packaging Information	479
	Appendix A: Revision History	507
	Index	517
	The Microchip Web Site	525
	Customer Change Notification Service	525
	Customer Support	525
	Product Identification System	527

1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com)

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM

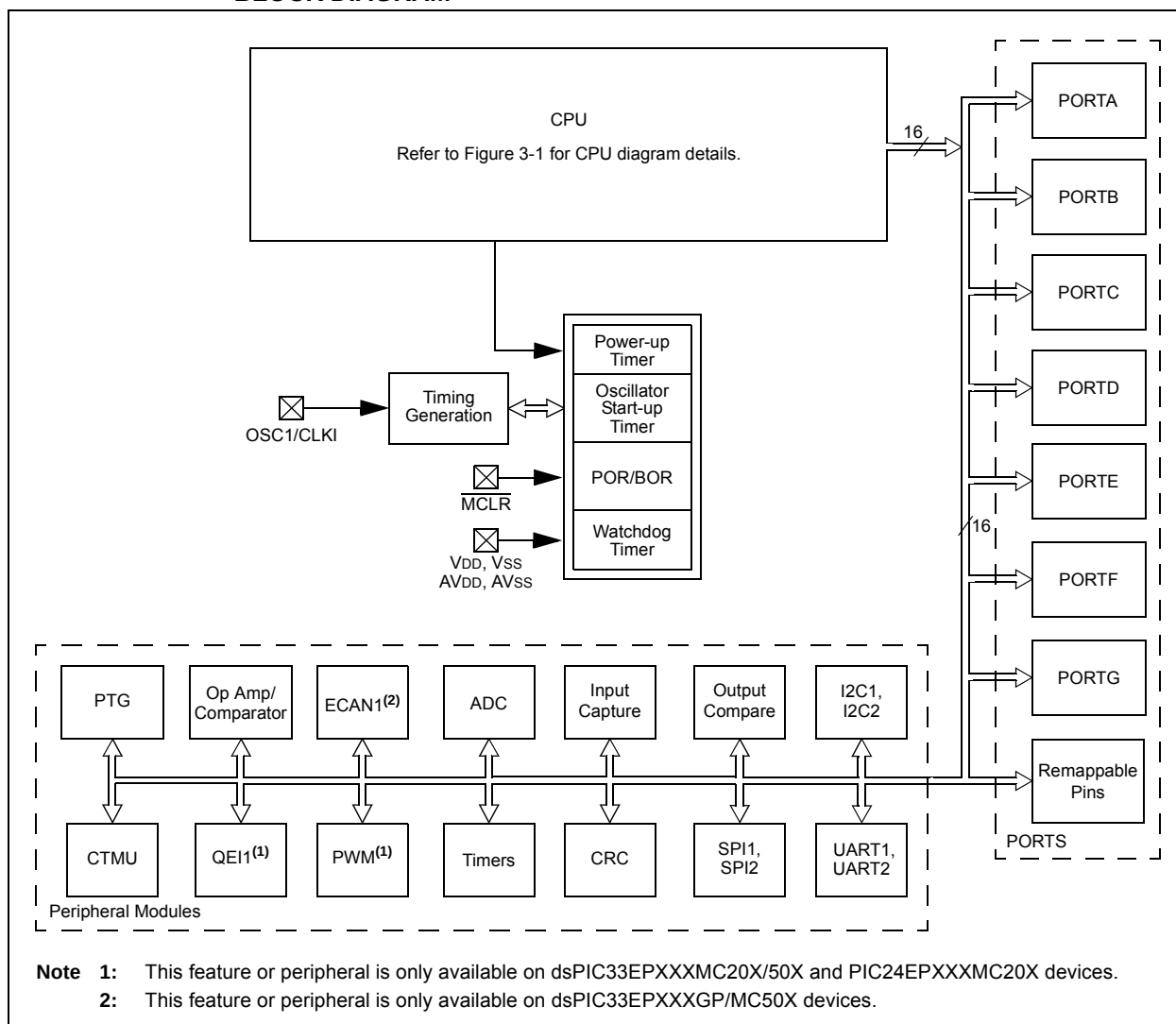
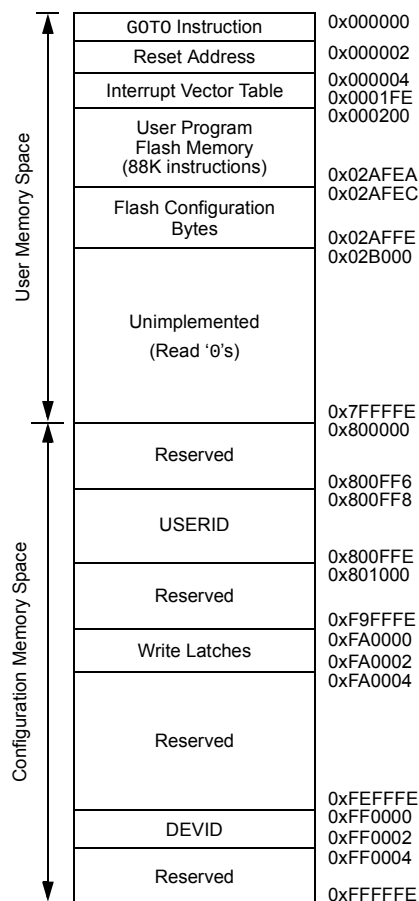


FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X AND PIC24EP256GP/MC20X DEVICES



Note: Memory areas are not shown to scale.

7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Interrupts**” (DS70600) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 246 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3⁽²⁾	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
 1 = Variable exception processing is enabled
 0 = Fixed exception processing is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3⁽²⁾
 1 = CPU Interrupt Priority Level is greater than 7
 0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see Register 3-2.

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 4	MATHERR: Math Error Status bit 1 = Math error trap has occurred 0 = Math error trap has not occurred
bit 3	ADDRERR: Address Error Trap Status bit 1 = Address error trap has occurred 0 = Address error trap has not occurred
bit 2	STKERR: Stack Error Trap Status bit 1 = Stack error trap has occurred 0 = Stack error trap has not occurred
bit 1	OSCFAIL: Oscillator Failure Trap Status bit 1 = Oscillator failure trap has occurred 0 = Oscillator failure trap has not occurred
bit 0	Unimplemented: Read as '0'

Note 1: These bits are available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC4R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC3R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC4R<6:0>:** Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC3R<6:0>:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 17-2: QE1IOC: QE1 I/O CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **QCAPEN:** QE1 Position Counter Input Capture Enable bit
1 = Index match event triggers a position capture event
0 = Index match event does not trigger a position capture event
- bit 14 **FLTREN:** QEAx/QEBx/INDXx/HOMEx Digital Filter Enable bit
1 = Input pin digital filter is enabled
0 = Input pin digital filter is disabled (bypassed)
- bit 13-11 **QFDIV<2:0>:** QEAx/QEBx/INDXx/HOMEx Digital Input Filter Clock Divide Select bits
111 = 1:128 clock divide
110 = 1:64 clock divide
101 = 1:32 clock divide
100 = 1:16 clock divide
011 = 1:8 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide
- bit 10-9 **OUTFNC<1:0>:** QE1 Module Output Function Mode Select bits
11 = The CTNCMPx pin goes high when $QE1LEC \geq POS1CNT \geq QE1GEC$
10 = The CTNCMPx pin goes high when $POS1CNT \leq QE1LEC$
01 = The CTNCMPx pin goes high when $POS1CNT \geq QE1GEC$
00 = Output is disabled
- bit 8 **SWPAB:** Swap QEA and QEB Inputs bit
1 = QEAx and QEBx are swapped prior to quadrature decoder logic
0 = QEAx and QEBx are not swapped
- bit 7 **HOMPOL:** HOMEx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted
- bit 6 **IDXPOL:** INDXx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted
- bit 5 **QEBPOL:** QEBx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted
- bit 4 **QEAPOL:** QEAx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted
- bit 3 **HOME:** Status of HOMEx Input Pin After Polarity Control
1 = Pin is at logic '1'
0 = Pin is at logic '0'

REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER (CONTINUED)

bit 2	INDEX: Status of INDXx Input Pin After Polarity Control 1 = Pin is at logic '1' 0 = Pin is at logic '0'
bit 1	QEB: Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1' 0 = Pin is at logic '0'
bit 0	QEA: Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping 1 = Pin is at logic '1' 0 = Pin is at logic '0'

REGISTER 17-3: QE11STAT: QE11 STATUS REGISTER

U-0	U-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
bit 15							bit 8

HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
PCIIRQ ⁽¹⁾	PCIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
bit 7							bit 0

Legend:	HS = Hardware Settable bit	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **PCHEQIRQ:** Position Counter Greater Than or Equal Compare Status bit
1 = POS1CNT ≥ QE11GEC
0 = POS1CNT < QE11GEC
- bit 12 **PCHEQIEN:** Position Counter Greater Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled
- bit 11 **PCLEQIRQ:** Position Counter Less Than or Equal Compare Status bit
1 = POS1CNT ≤ QE11LEC
0 = POS1CNT > QE11LEC
- bit 10 **PCLEQIEN:** Position Counter Less Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled
- bit 9 **POSOVIRQ:** Position Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred
- bit 8 **POSOVIEN:** Position Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled
- bit 7 **PCIIRQ:** Position Counter (Homing) Initialization Process Complete Status bit⁽¹⁾
1 = POS1CNT was reinitialized
0 = POS1CNT was not reinitialized
- bit 6 **PCIEN:** Position Counter (Homing) Initialization Process Complete interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled
- bit 5 **VELOVIRQ:** Velocity Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has not occurred
- bit 4 **VELOVIEN:** Velocity Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled
- bit 3 **HOMIRQ:** Status Flag for Home Event Status bit
1 = Home event has occurred
0 = No Home event has occurred

Note 1: This status bit is only applicable to PIMOD<2:0> modes, '011' and '100'.

REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2	SPRE<2:0> : Secondary Prescale bits (Master mode) ⁽³⁾ 111 = Secondary prescale 1:1 110 = Secondary prescale 2:1 • • • 000 = Secondary prescale 8:1
bit 1-0	PPRE<1:0> : Primary Prescale bits (Master mode) ⁽³⁾ 11 = Primary prescale 1:1 10 = Primary prescale 4:1 01 = Primary prescale 16:1 00 = Primary prescale 64:1

- Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
- 2:** This bit must be cleared when FRMEN = 1.
- 3:** Do not set both primary and secondary prescalers to the value of 1:1.

REGISTER 21-16: CxRXFnSID: ECANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDE	—	EID17	EID16
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-5 **SID<10:0>**: Standard Identifier bits
 1 = Message address bit, SIDx, must be '1' to match filter
 0 = Message address bit, SIDx, must be '0' to match filter

bit 4 **Unimplemented**: Read as '0'

bit 3 **EXIDE**: Extended Identifier Enable bit
 If MIDE = 1:
 1 = Matches only messages with Extended Identifier addresses
 0 = Matches only messages with Standard Identifier addresses
 If MIDE = 0:
 Ignores EXIDE bit.

bit 2 **Unimplemented**: Read as '0'

bit 1-0 **EID<17:16>**: Extended Identifier bits
 1 = Message address bit, EIDx, must be '1' to match filter
 0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)

bit 1-0 **PTGITM<1:0>**: PTG Input Trigger Command Operating Mode bits⁽¹⁾

- 11 = Single level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
- 10 = Single level detect with Step delay executed on exit of command
- 01 = Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
- 00 = Continuous edge detect with Step delay executed on exit of command

- Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.
- 2:** This bit is only used with the PTGCTRL step command software trigger option.
- 3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

FIGURE 25-2: COMPARATOR MODULE BLOCK DIAGRAM (MODULE 4)

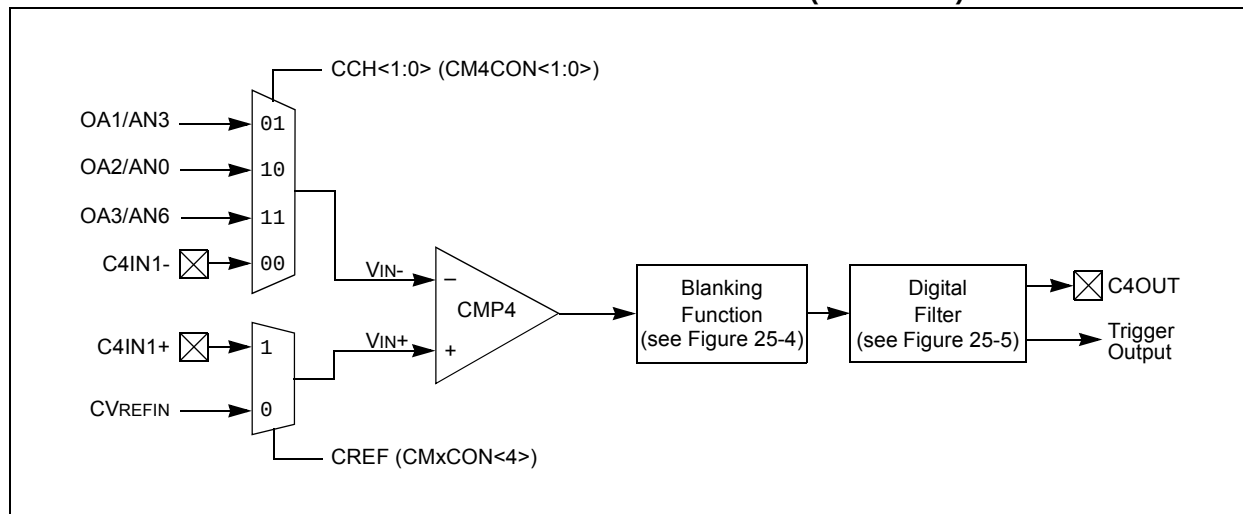


FIGURE 25-3: OP AMP/COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

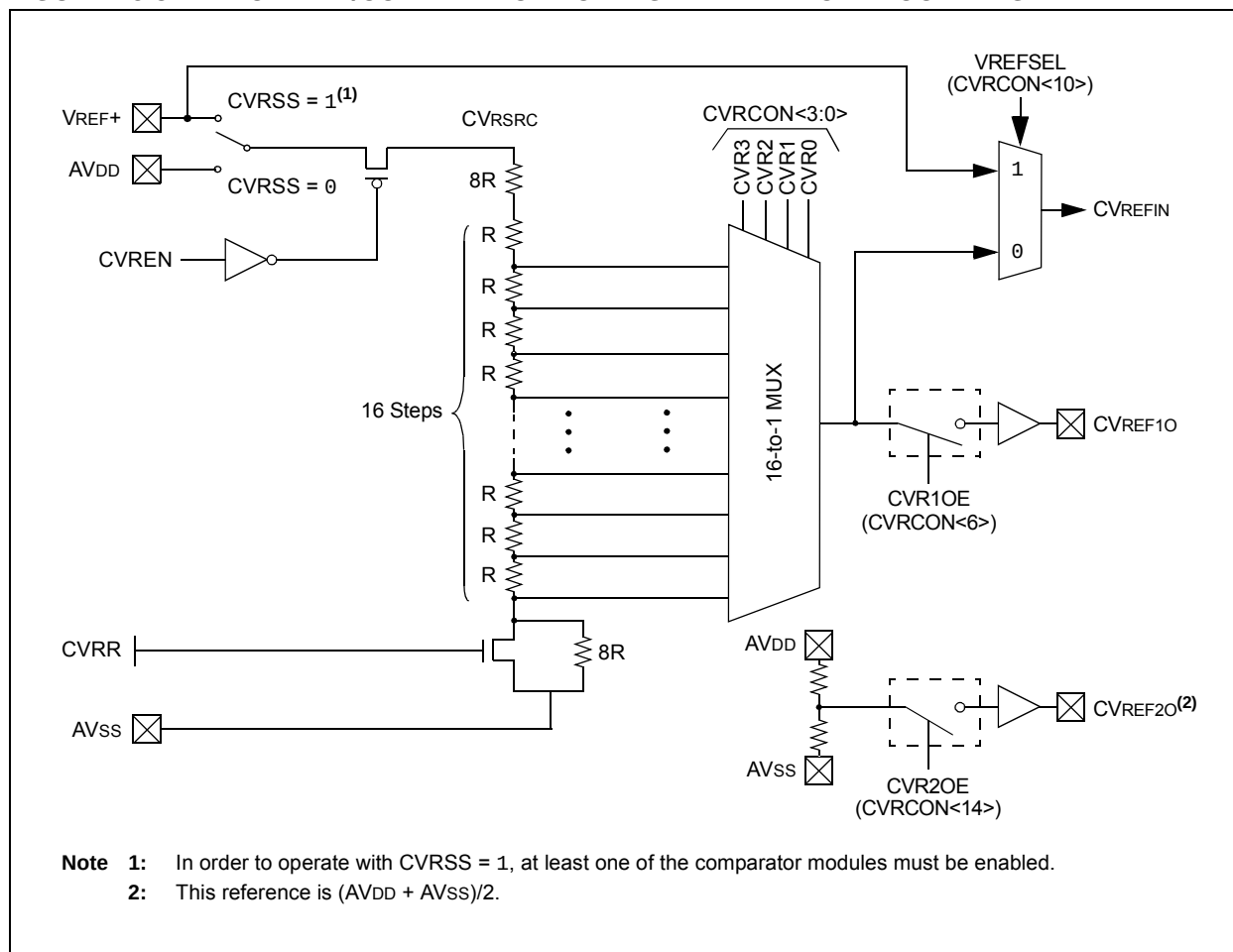


FIGURE 30-3: I/O TIMING CHARACTERISTICS

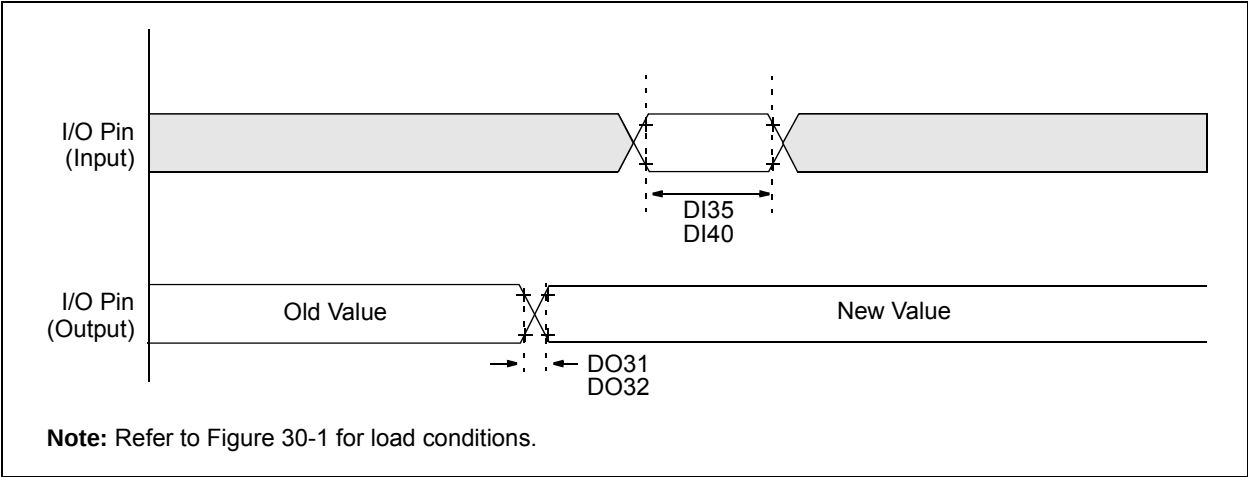
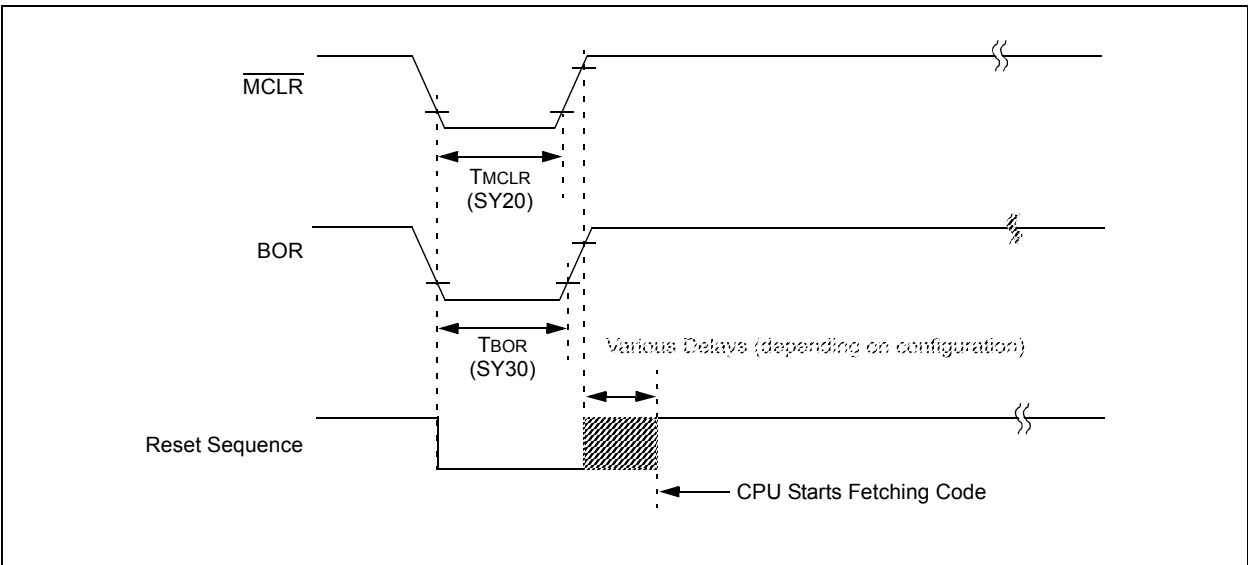


TABLE 30-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DO31	TioR	Port Output Rise Time	—	5	10	ns	
DO32	TioF	Port Output Fall Time	—	5	10	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	Tcy	

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS



**TABLE 30-46: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	Lesser of Fp or 11	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1} \downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1} \uparrow$ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	Tsch2ssH, TscL2ssH	$\overline{SS1} \uparrow$ after SCK1 Edge	1.5 Tcy + 40	—	—	ns	(Note 4)
SP60	TssL2doV	SDO1 Data Output Valid after $\overline{SS1}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 30-57: ADC MODULE SPECIFICATIONS

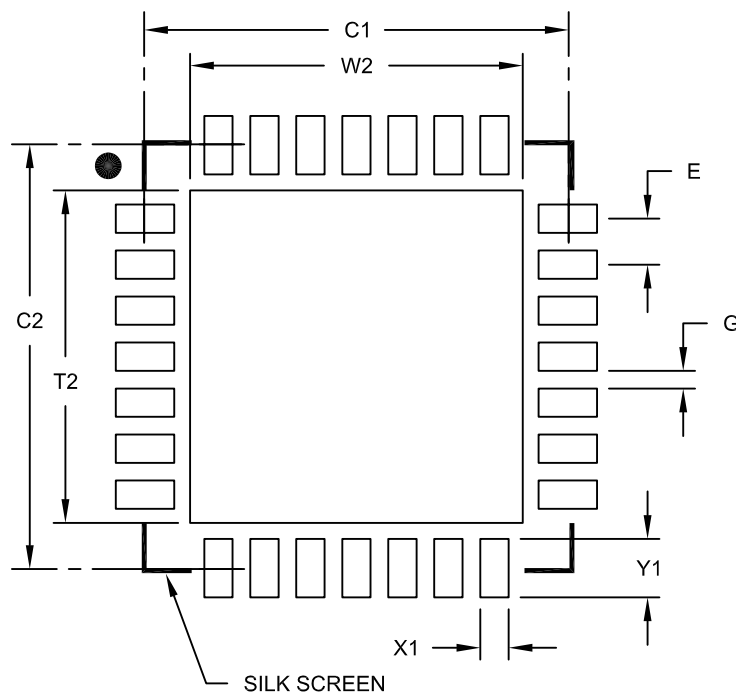
AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 3.0	—	Lesser of: VDD + 0.3 or 3.6	V	
AD02	AVSS	Module Vss Supply	Vss – 0.3	—	Vss + 0.3	V	
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVss + 2.5	—	AVDD	V	VREFH = VREF+ VREFL = VREF- (Note 1)
AD05a			3.0	—	3.6	V	VREFH = AVDD VREFL = AVSS = 0
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – 2.5	V	(Note 1)
AD06a			0	—	0	V	VREFH = AVDD VREFL = AVSS = 0
AD07	VREF	Absolute Reference Voltage	2.5	—	3.6	V	VREF = VREFH - VREFL
AD08	IREF	Current Drain	— —	— —	10 600	μA μA	ADC off ADC on
AD09	IAD	Operating Current ⁽²⁾	—	5	—	mA	ADC operating in 10-bit mode (Note 1)
			—	2	—	mA	ADC operating in 12-bit mode (Note 1)
Analog Input							
AD12	VINH	Input Voltage Range VINH	VINL	—	VREFH	V	This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input
AD13	VINL	Input Voltage Range VINL	VREFL	—	AVSS + 1V	V	This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	200	Ω	Impedance to achieve maximum performance of ADC

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

2: Parameter is characterized but not tested in manufacturing.

**28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S]
with 0.40 mm Contact Length**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (Y28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

TABLE A-5: MAJOR SECTION UPDATES (CONTINUED)

Section Name	Update Description
Section 30.0 “Electrical Characteristics”	• Throughout: qualifies all footnotes relating to the operation of analog modules below VDDMIN (replaces “will have” with “may have”) • Throughout: changes all references of SPI timing parameter symbol “TscP” to “FscP” • Table 30-1: changes VDD range to 3.0V to 3.6V • Table 30-4: removes Parameter DC12 (RAM Retention Voltage) • Table 30-7: updates Maximum values at 10 and 20 MIPS • Table 30-8: adds Maximum IPD values, and removes all ΔI_{WDT} entries • Adds new Table 30-9 (Watchdog Timer Delta Current) with consolidated values removed from Table 30-8. All subsequent tables are renumbered accordingly. • Table 30-10: adds footnote for all parameters for 1:2 Doze ratio • Table 30-11: - changes Minimum and Maximum values for D120 and D130 - adds Minimum and Maximum values for D131 - adds Minimum and Maximum values for D150 through D156, and removes Typical values • Table 30-12: - reformats table for readability - changes IOL conditions for DO10 • Table 30-14: adds footnote to D135 • Table 30-17: changes Minimum and Maximum values for OS30 • Table 30-19: - splits temperature range and adds new values for F20a - reduces temperature range for F20b to extended temperatures only • Table 30-20: - splits temperature range and adds new values for F21a - reduces temperature range for F20b to extended temperatures only • Table 30-53: - adds Maximum value to CM30 - adds footnote (“Parameter characterized...”) to multiple parameters • Table 30-55: adds Minimum and Maximum values for all CTMUI specifications, and removes Typical values • Table 30-57: adds new footnote to AD09 • Table 30-58: - removes all specifications for accuracy with external voltage references - removes Typical values for AD23a and AD24a - replaces Minimum and Maximum values for AD21a, AD22a, AD23a and AD24a with new values, split by Industrial and Extended temperatures - removes Maximum value of AD30 - removes Minimum values from AD31a and AD32a - adds or changes Typical values for AD30, AD31a, AD32a and AD33a • Table 30-59: - removes all specifications for accuracy with external voltage references - removes Maximum value of AD30 - removes Typical values for AD23b and AD24b - replaces Minimum and Maximum values for AD21b, AD22b, AD23b and AD24b with new values, split by Industrial and Extended temperatures - removes Minimum and Maximum values from AD31b, AD32b, AD33b and AD34b - adds or changes Typical values for AD30, AD31a, AD32a and AD33a • Table 30-61: Adds footnote to AD51
Section 32.0 “DC and AC Device Characteristics Graphs”	• Updates Figure 32-6 (Typical IDD @ 3.3V) with individual current vs. processor speed curves for the different program memory sizes
Section 33.0 “Packaging Information”	• Replaces drawing C04-149C (64-pin QFN, 7.15 x 7.15 exposed pad) with C04-154A (64-pin QFN, 5.4 x 5.4 exposed pad)