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Details

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Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64gp204t-e-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "CPU" (DS70359) in the "dsPIC33/PIC24 Family Reference Manual', which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can act as a data, address or address offset register. The 16th working register (W15) operates as a Software Stack Pointer for interrupts and calls.

3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The base Data Space can be addressed as 64 Kbytes (32K words).

The Data Space includes two ranges of memory, referred to as X and Y data memory. Each memory range is accessible through its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Spaces have memory locations that are device-specific, and are described further in the data memory maps in **Section 4.2 "Data Address Space"**.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 32-Kbyte aligned program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to the "**Data Memory**" (DS70595) and "**Program Memory**" (DS70613) sections in the "*dsPIC33/PIC24 Family Reference Manual*" for more details on EDS, PSV and table accesses.

On the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reversed Addressing.

3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- · Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5	IPL<2:0>: CPU Interrupt Priority Level Status bits ^(2,3) 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8)
bit 4	RA: REPEAT Loop Active bit 1 = REPEAT loop in progress 0 = REPEAT loop not in progress
bit 3	N: MCU ALU Negative bit 1 = Result was negative 0 = Result was non-negative (zero or positive)
bit 2	 OV: MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred
bit 1	 Z: MCU ALU Zero bit 1 = An operation that affects the Z bit has set it at some time in the past 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)
bit 0	C: MCU ALU Carry/Borrow bit 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred
Note 1: 2:	This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only. The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority

- Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
 3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- 4: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 2	SFA: Stack Frame Active Status bit
	1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and
	DSWPAG values
	0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space
hit 1	PND: Dounding Mode Select hit(1)

- bit 1 **RND:** Rounding Mode Select bit⁽¹⁾
 - 1 = Biased (conventional) rounding is enabled
 - 0 = Unbiased (convergent) rounding is enabled

bit 0 IF: Integer or Fractional Multiplier Mode Select bit⁽¹⁾ 1 = Integer mode is enabled for DSP multiply 0 = Fractional mode is enabled for DSP multiply

- Note 1: This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
 - **2:** This bit is always read as '0'.
 - 3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4-19: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0	>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI1CON1	0242	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI1BUF	0248							SPI1 Tra	ansmit and F	Receive Buf	fer Registe	r						0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	:	SPIBEC<2:0)>	SRMPT	SPIROV	SRXMPT		SISEL<2:0>		SPITBF	SPIRBF	0000
SPI2CON1	0262	_	—		DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN		SPRE<2:0>		PPRE	<1:0>	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	—	_	_	_	FRMDLY	SPIBEN	0000
SPI2BUF	0268	3 SPI2 Transmit and Receive Buffer Register						0000										

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—			RP57	R<5:0>		
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—			RP56	R<5:0>		
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplem			
-n = Value a	t POR	'1' = Bit is set	t	'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-14	Unimpleme	nted: Read as '	0'				
bit 13-8	RP57R<5:0> (see Table 1 [*]	 Peripheral Out 1-3 for peripheral 	utput Functior al function nu	n is Assigned to mbers)	RP57 Output	Pin bits	
bit 7-6	Unimpleme	nted: Read as '	0'				

REGISTER 11-24: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

(see Table	11-3 for peripheral function numbers)	

REGISTER 11-25: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			RP97	R<5:0>		
bit 15							bit 8

RP56R<5:0>: Peripheral Output Function is Assigned to RP56 Output Pin bits

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

bit 13-8 **RP97R<5:0>:** Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-0 Unimplemented: Read as '0'

bit 5-0



FIGURE 13-2: TYPE C TIMER BLOCK DIAGRAM (x = 3 AND 5)



FIGURE 13-1:TYPE B TIMER BLOCK DIAGRAM (x = 2 AND 4)

14.1 Input Capture Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

14.1.1 KEY RESOURCES

- "Input Capture" (DS70352) in the "dsPIC33/ PIC24 Family Reference Manual"
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 7-	6	DTC<1:0>: Dead-Time Control bits
		11 = Dead-Time Compensation mode
		10 = Dead-time function is disabled
		01 = Negative dead time is actively applied for Complementary Output mode
		00 = Positive dead time is actively applied for all output modes
bit 5		DTCP: Dead-Time Compensation Polarity bit ⁽³⁾
		When Set to '1':
		If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened.
		II DI CMPX = 1, PWWXH IS SNOTENED and PWWXL IS lengthened.
		When Set to 0.2. If DTCMPx = 0. PW/MxH is shortened and PW/MxL is lengthened
		If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.
bit 4		Unimplemented: Read as '0'
bit 3		MTBS: Master Time Base Select bit
		1 = PWM generator uses the secondary master time base for synchronization and as the clock source
		for the PWM generation logic (if secondary time base is available)
		0 = PWM generator uses the primary master time base for synchronization and as the clock source
		for the PWM generation logic
bit 2		CAM: Center-Aligned Mode Enable bit ^(2,4)
		1 = Center-Aligned mode is enabled
		0 = Edge-Aligned mode is enabled
bit 1		XPRES: External PWMx Reset Control bit ⁽⁵⁾
		 1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
		0 = External pins do not affect PWMx time base
bit 0		IUE: Immediate Update Enable bit ⁽²⁾
		1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate
		 Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary
Note	1:	Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
	2:	These bits should not be changed after the PWMx is enabled (PTEN = 1).
	3:	DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
	4:	The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.

5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 6	STREN: SCLx Clock Stretch Enable bit (when operating as I ² C slave) Used in conjunction with the SCLREL bit. 1 = Enables software or receives clock stretching 0 = Disables software or receives clock stretching
bit 5	ACKDT: Acknowledge Data bit (when operating as I ² C master, applicable during master receive)
	Value that is transmitted when the software initiates an Acknowledge sequence. 1 = Sends NACK during Acknowledge 0 = Sends ACK during Acknowledge
bit 4	ACKEN: Acknowledge Sequence Enable bit (when operating as I ² C master, applicable during master receive)
	 1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit. Hardware is clear at the end of the master Acknowledge sequence. 0 = Acknowledge sequence is not in progress
bit 3	RCEN: Receive Enable bit (when operating as I ² C master)
	 1 = Enables Receive mode for I²C. Hardware is clear at the end of the eighth bit of the master receive data byte. a Receive acquirement in program.
hit 2	0 = Receive sequence is not in progress
511 2	 1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of the master Stop sequence. a Stop condition is not in processor.
h :+ 4	0 = Stop condition is not in progress
DIT	RSEN: Repeated Start Condition Enable bit (when operating as I-C master)
	 Initiates Repeated Start condition on SDAx and SCLX pins. Hardware is clear at the end of the master Repeated Start sequence. 0 = Repeated Start condition is not in progress
bit 0	SEN: Start Condition Enable bit (when operating as l^2C master)
	 1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Start sequence. 0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

24.0 PERIPHERAL TRIGGER GENERATOR (PTG) MODULE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X. dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Peripheral Trigger Generator (PTG)" (DS70669) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

24.1 Module Introduction

The Peripheral Trigger Generator (PTG) provides a means to schedule complex high-speed peripheral operations that would be difficult to achieve using software. The PTG module uses 8-bit commands, called "Steps", that the user writes to the PTG Queue registers (PTGQUE0-PTGQUE7), which perform operations, such as wait for input signal, generate output trigger and wait for timer.

The PTG module has the following major features:

- Multiple clock sources
- Two 16-bit general purpose timers
- Two 16-bit general limit counters
- Configurable for rising or falling edge triggering
- Generates processor interrupts to include:
 - Four configurable processor interrupts
 - Interrupt on a Step event in Single-Step modeInterrupt on a PTG Watchdog Timer time-out
- Able to receive trigger signals from these peripherals:
 - ADC
 - PWM
 - Output Compare
 - Input Capture
 - Op Amp/Comparator
 - INT2
- Able to trigger or synchronize to these peripherals:
 - Watchdog Timer
 - Output Compare
 - Input Capture
 - ADC
 - PWM
- Op Amp/Comparator

REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)

bit 3 ABEN: AND Gate B Input Enable bit 1 = MBI is connected to AND gate 0 = MBI is not connected to AND gate bit 2 ABNEN: AND Gate B Input Inverted Enable bit 1 = Inverted MBI is connected to AND gate 0 = Inverted MBI is not connected to AND gate bit 1 AAEN: AND Gate A Input Enable bit 1 = MAI is connected to AND gate 0 = MAI is not connected to AND gate bit 0 AANEN: AND Gate A Input Inverted Enable bit 1 = Inverted MAI is connected to AND gate 0 = Inverted MAI is not connected to AND gate

NOTES:

Bit Field	Description
GCP	General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = Code protection is enabled for the entire program memory space
GWRP	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	 Two-Speed Oscillator Start-up Enable bit 1 = Start up device with FRC, then automatically switch to the user-selected oscillator source when ready 0 = Start up device with user-selected oscillator source
PWMLOCK ⁽¹⁾	PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence
FNOSC<2:0>	Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 (FRCDIV16) 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit 1 = Allow only one reconfiguration 0 = Allow multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	 Watchdog Timer Enable bit 1 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)
WINDIS	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled

TABLE 27-2: CONFIGURATION BITS DESCRIPTION

Note 1: This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

2: When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

DC CHARACTERISTICS			Standard Oper (unless otherw Operating temp	ating Conditions: 3.0V t rise stated) perature $-40^{\circ}C \le TA \le +8$ $-40^{\circ}C \le TA \le +7$	o 3.6V 35°C for Industrial 125°C for Extended
Parameter No.	Тур.	Max.	Units	Conditions	
DC61d	8		μΑ	-40°C	
DC61a	10	—	μA	+25°C	2.21/
DC61b	12	_	μA	+85°C	3.3V
DC61c	13		μA	+125°C	

TABLE 30-9: DC CHARACTERISTICS: WATCHDOG TIMER DELTA CURRENT (Δ Iwdt)⁽¹⁾

Note 1: The \triangle IwDT current is the additional current consumed when the module is enabled. This current should be added to the base IPD current. All parameters are characterized but not tested during manufacturing.

TABLE 30-10: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTERISTICS			Standard C (unless oth Operating to	perating erwise st emperatur	Condition ated) e -40°C -40°C	s: 3.0V to ≤ Ta ≤ +8 ≤ Ta ≤ +1	3.6V 5°C for Industrial 25°C for Extended
Parameter No.	Тур.	Max.	Doze Units Conditions			litions	
Doze Current (IDOZE) ⁽¹⁾							
DC73a ⁽²⁾	35	_	1:2	mA	40°C	3 3//	Ecco - 140 MHz
DC73g	20	30	1:128	mA	-40 C	3.3V	F03C - 140 MI12
DC70a ⁽²⁾	35	—	1:2	mA	+25%	2 21/	E000 - 140 MH7
DC70g	20	30	1:128	mA	720 C	3.3V	FUSC - 140 MITZ
DC71a ⁽²⁾	35	—	1:2	mA	+95°C	2 21/	E000 - 140 MHz
DC71g	20	30	1:128	mA	+05 C	3.3V	
DC72a ⁽²⁾	28	_	1:2	mA	±125°C	3 3//	Ecco - 120 MHz
DC72g	15	30	1:128	mA	+120 C	3.3V	

Note 1: IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing while(1) statement
- · JTAG is disabled
- 2: Parameter is characterized but not tested in manufacturing.

TABLE 30-37:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	ARACTERIS	TICS	Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industri $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				V to 3.6V +85°C for Industrial +125°C for Extended
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	-	—	Lesser of FP or 15	MHz	(Note 3)
SP72	TscF	SCK2 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK2 Input Rise Time	—	_	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO2 Data Output Rise Time	—	_	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	_	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	-	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.



FIGURE 30-21: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	Units	N	IILLIMETER	S
Dimension	Limits	MIN	NOM	MAX
Number of Pins	Ν		44	
Number of Pins per Side	ND		12	
Number of Pins per Side	NE		10	
Pitch	е	0.50 BSC		
Overall Height	Α	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	Е	6.00 BSC		
Exposed Pad Width	E2	4.40	4.55	4.70
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	4.40	4.55	4.70
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	К	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-157C Sheet 2 of 2

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