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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64gp204t-e-tl">https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64gp204t-e-tl</a>

## 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Program Memory**” (DS70613) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

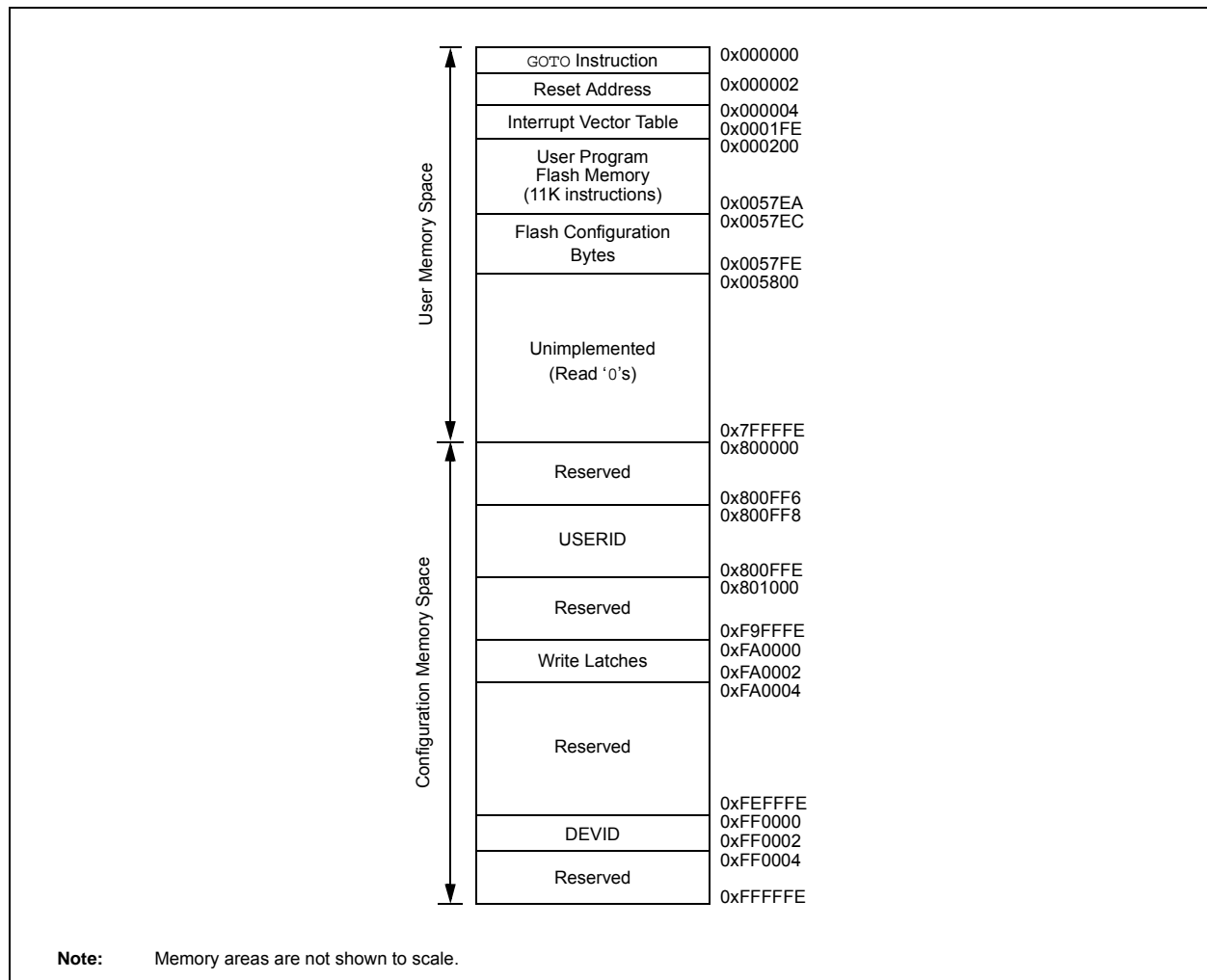
## 4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in **Section 4.8 “Interfacing Program and Data Memory Spaces”**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-5.

**FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X AND PIC24EP32GP/MC20X DEVICES**



## 4.2.5 X AND Y DATA SPACES

The dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X core has two Data Spaces, X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y Data Space is used in concert with the X Data Space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space. Modulo Addressing and Bit-Reversed Addressing are not present in PIC24EPXXXGP/MC20X devices.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

## 4.3 Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

<b>Note:</b>	In the event you are not able to access the product page using the link above, enter this URL in your browser: <a href="http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464">http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464</a>
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### 4.3.1 KEY RESOURCES

- “**Program Memory**” (DS70613) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

**TABLE 4-10: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 4 REGISTER MAP**

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0900	—	—	OCSIDL	OCTSEL<2:0>			—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC1RS	0904	Output Compare 1 Secondary Register																xxxx
OC1R	0906	Output Compare 1 Register																xxxx
OC1TMR	0908	Timer Value 1 Register																xxxx
OC2CON1	090A	—	—	OCSIDL	OCTSEL<2:0>			—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC2RS	090E	Output Compare 2 Secondary Register																xxxx
OC2R	0910	Output Compare 2 Register																xxxx
OC2TMR	0912	Timer Value 2 Register																xxxx
OC3CON1	0914	—	—	OCSIDL	OCTSEL<2:0>			—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC3RS	0918	Output Compare 3 Secondary Register																xxxx
OC3R	091A	Output Compare 3 Register																xxxx
OC3TMR	091C	Timer Value 3 Register																xxxx
OC4CON1	091E	—	—	OCSIDL	OCTSEL<2:0>			—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM<2:0>			0000
OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL<4:0>					000C
OC4RS	0922	Output Compare 4 Secondary Register																xxxx
OC4R	0924	Output Compare 4 Register																xxxx
OC4TMR	0926	Timer Value 4 Register																xxxx

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER**

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE2 <sup>(1)</sup>	DOZE1 <sup>(1)</sup>	DOZE0 <sup>(1)</sup>	DOZEN <sup>(2,3)</sup>	FRCDIV2	FRCDIV1	FRCDIV0
bit 15							bit 8

R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOST1	PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15            **ROI:** Recover on Interrupt bit  
1 = Interrupts will clear the DOZEN bit  
0 = Interrupts have no effect on the DOZEN bit
- bit 14-12       **DOZE<2:0>:** Processor Clock Reduction Select bits<sup>(1)</sup>  
111 = Fcy divided by 128  
110 = Fcy divided by 64  
101 = Fcy divided by 32  
100 = Fcy divided by 16  
011 = Fcy divided by 8 (default)  
010 = Fcy divided by 4  
001 = Fcy divided by 2  
000 = Fcy divided by 1
- bit 11            **DOZEN:** Doze Mode Enable bit<sup>(2,3)</sup>  
1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks  
0 = Processor clock and peripheral clock ratio is forced to 1:1
- bit 10-8        **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits  
111 = FRC divided by 256  
110 = FRC divided by 64  
101 = FRC divided by 32  
100 = FRC divided by 16  
011 = FRC divided by 8  
010 = FRC divided by 4  
001 = FRC divided by 2  
000 = FRC divided by 1 (default)
- bit 7-6         **PLLPOST<1:0>:** PLL VCO Output Divider Select bits (also denoted as 'N2', PLL postscaler)  
11 = Output divided by 8  
10 = Reserved  
01 = Output divided by 4 (default)  
00 = Output divided by 2
- bit 5            **Unimplemented:** Read as '0'

- Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
- 2:** This bit is cleared when the ROI bit is set and an interrupt occurs.
- 3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

**REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6**

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PWM3MD <sup>(1)</sup>	PWM2MD <sup>(1)</sup>	PWM1MD <sup>(1)</sup>
bit 15					bit 8		

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7					bit 0		

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **PWM3MD:** PWM3 Module Disable bit<sup>(1)</sup>

1 = PWM3 module is disabled

0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit<sup>(1)</sup>

1 = PWM2 module is disabled

0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit<sup>(1)</sup>

1 = PWM1 module is disabled

0 = PWM1 module is enabled

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** This bit is available on dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

**REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	OCFAR<6:0>							
bit 7								bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7

**Unimplemented:** Read as '0'

bit 6-0

**OCFAR<6:0>:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121

.

.

.

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

## 17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Quadrature Encoder Interface (QEI)**” (DS70601) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.



## 17.2 QEI Control Registers

REGISTER 17-1: QE1CON: QE1 CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QE1EN	—	QE1SIDL	PIMOD2 <sup>(1)</sup>	PIMOD1 <sup>(1)</sup>	PIMOD0 <sup>(1)</sup>	IMV1 <sup>(2)</sup>	IMV0 <sup>(2)</sup>
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INTDIV2 <sup>(3)</sup>	INTDIV1 <sup>(3)</sup>	INTDIV0 <sup>(3)</sup>	CNTPOL	GATEN	CCM1	CCM0
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15            **QE1EN:** Quadrature Encoder Interface Module Counter Enable bit  
1 = Module counters are enabled  
0 = Module counters are disabled, but SFRs can be read or written to
- bit 14            **Unimplemented:** Read as '0'
- bit 13            **QE1SIDL:** QE1 Stop in Idle Mode bit  
1 = Discontinues module operation when device enters Idle mode  
0 = Continues module operation in Idle mode
- bit 12-10        **PIMOD<2:0>:** Position Counter Initialization Mode Select bits<sup>(1)</sup>  
111 = Reserved  
110 = Modulo Count mode for position counter  
101 = Resets the position counter when the position counter equals QE1GEC register  
100 = Second index event after home event initializes position counter with contents of QE1IC register  
011 = First index event after home event initializes position counter with contents of QE1IC register  
010 = Next index input event initializes the position counter with contents of QE1IC register  
001 = Every index input event resets the position counter  
000 = Index input event does not affect position counter
- bit 9            **IMV1:** Index Match Value for Phase B bit<sup>(2)</sup>  
1 = Phase B match occurs when QEB = 1  
0 = Phase B match occurs when QEB = 0
- bit 8            **IMV0:** Index Match Value for Phase A bit<sup>(2)</sup>  
1 = Phase A match occurs when QEA = 1  
0 = Phase A match occurs when QEA = 0
- bit 7            **Unimplemented:** Read as '0'

- Note 1:** When CCM<1:0> = 10 or 11, all of the QE1 counters operate as timers and the PIMOD<2:0> bits are ignored.
- 2:** When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.
- 3:** The selected clock rate should be at least twice the expected maximum quadrature count rate.

**REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER**

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0
bit 15							bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **FBP<5:0>:** FIFO Buffer Pointer bits

011111 = RB31 buffer

011110 = RB30 buffer

•  
•  
•

000001 = TRB1 buffer

000000 = TRB0 buffer

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **FNRB<5:0>:** FIFO Next Read Buffer Pointer bits

011111 = RB31 buffer

011110 = RB30 buffer

•  
•  
•

000001 = TRB1 buffer

000000 = TRB0 buffer

**NOTES:**

**REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2**

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
VCFG2	VCFG1	VCFG0	—	—	CSCNA	CHPS1	CHPS0
bit 15						bit 8	

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7						bit 0	

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 15-13      **VCFG<2:0>:** Converter Voltage Reference Configuration bits

Value	VREFH	VREFL
000	AVDD	Avss
001	External VREF+	Avss
010	AVDD	External VREF-
011	External VREF+	External VREF-
1xx	AVDD	AVSS

bit 12-11      **Unimplemented:** Read as '0'

bit 10      **CSCNA:** Input Scan Select bit

1 = Scans inputs for CH0+ during Sample MUXA  
0 = Does not scan inputs

bit 9-8      **CHPS<1:0>:** Channel Select bits

In 12-bit mode (AD21B = 1), the CHPS<1:0> bits are Unimplemented and are Read as '0':

1x = Converts CH0, CH1, CH2 and CH3  
01 = Converts CH0 and CH1  
00 = Converts CH0

bit 7      **BUFS:** Buffer Fill Status bit (only valid when BUFM = 1)

1 = ADC is currently filling the second half of the buffer; the user application should access data in the first half of the buffer  
0 = ADC is currently filling the first half of the buffer; the user application should access data in the second half of the buffer

bit 6-2      **SMPI<4:0>:** Increment Rate bits

When ADDMAEN = 0:

x1111 = Generates interrupt after completion of every 16th sample/conversion operation

x1110 = Generates interrupt after completion of every 15th sample/conversion operation

•

•

•

x0001 = Generates interrupt after completion of every 2nd sample/conversion operation

x0000 = Generates interrupt after completion of every sample/conversion operation

When ADDMAEN = 1:

11111 = Increments the DMA address after completion of every 32nd sample/conversion operation

11110 = Increments the DMA address after completion of every 31st sample/conversion operation

•

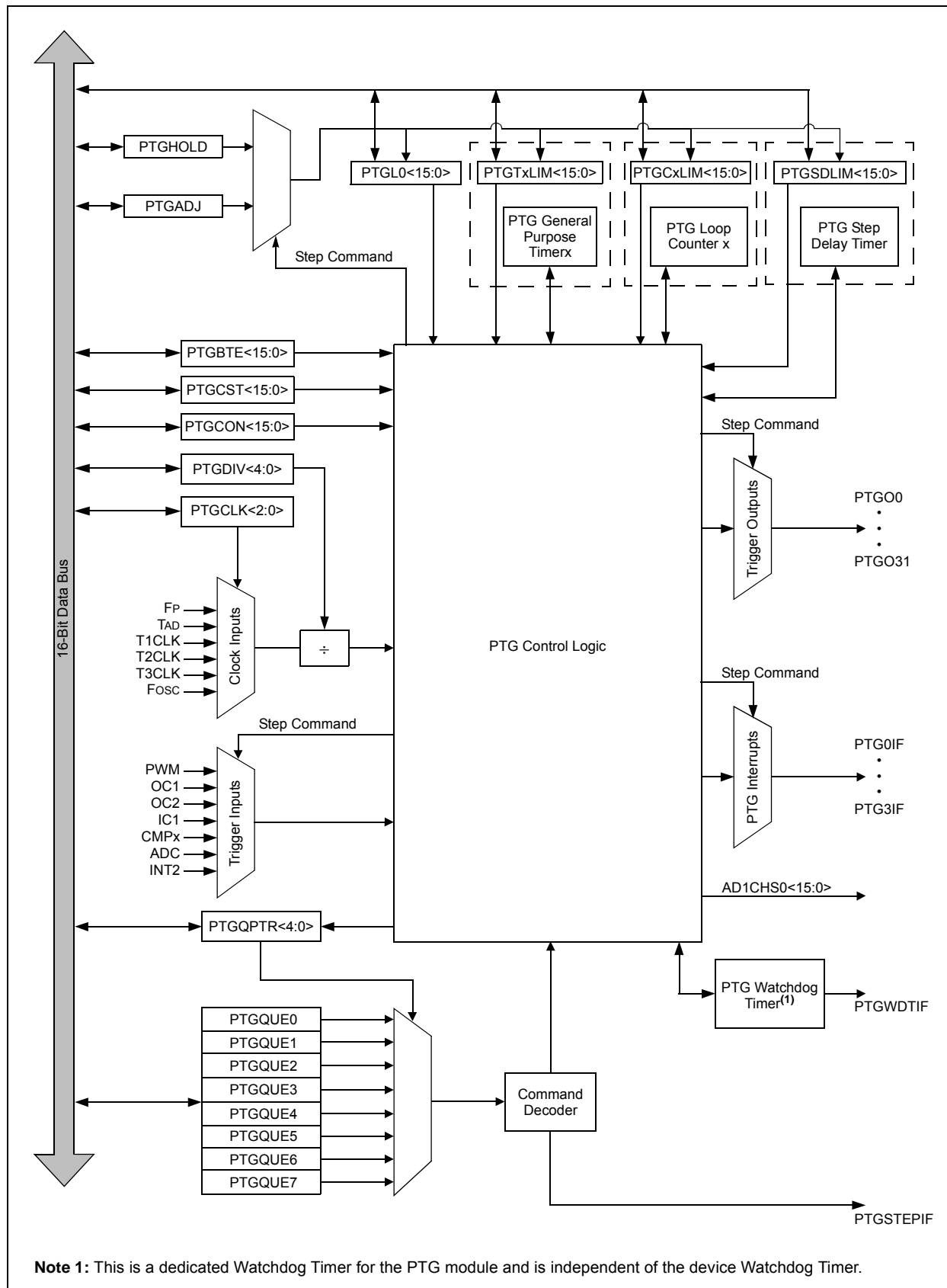
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•

00001 = Increments the DMA address after completion of every 2nd sample/conversion operation

00000 = Increments the DMA address after completion of every sample/conversion operation

FIGURE 24-1: PTF BLOCK DIAGRAM



**REGISTER 24-4: PTGT0LIM: PTG TIMER0 LIMIT REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PTGT0LIM<15:0>**: PTG Timer0 Limit Register bits

General Purpose Timer0 Limit register (effective only with a PTGT0 Step command).

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**REGISTER 24-5: PTGT1LIM: PTG TIMER1 LIMIT REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>**: PTG Timer1 Limit Register bits

General Purpose Timer1 Limit register (effective only with a PTGT1 Step command).

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGADJ<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGADJ<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **PTGADJ<15:0>**: PTG Adjust Register bits  
 This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGADD command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER<sup>(1)</sup>**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGL0<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGL0<7:0>							
bit 7				bit 0			

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 15-0      **PTGL0<15:0>**: PTG Literal 0 Register bits  
 This register holds the 16-bit value to be written to the AD1CHS0 register with the PTGCTRL Step command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions $\in \{W4 * W4, W5 * W5, W6 * W6, W7 * W7\}$
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions $\in \{W4 * W5, W4 * W6, W4 * W7, W5 * W6, W5 * W7, W6 * W7\}$
Wn	One of 16 working registers $\in \{W0...W15\}$
Wnd	One of 16 destination working registers $\in \{W0...W15\}$
Wns	One of 16 source working registers $\in \{W0...W15\}$
WREG	W0 (working register used in file register instructions)
Ws	Source W register $\in \{Ws, [Ws], [Ws++] , [Ws--], [++Ws], [--Ws] \}$
Wso	Source W register $\in \{Wns, [Wns], [Wns++] , [Wns--], [++Wns], [--Wns], [Wns+Wb] \}$
Wx	X Data Space Prefetch Address register for DSP instructions $\in \{[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], \text{none}\}$
Wxd	X Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$
Wy	Y Data Space Prefetch Address register for DSP instructions $\in \{[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], \text{none}\}$
Wyd	Y Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$



TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DI10 DI18 DI19	V <sub>IL</sub>	<b>Input Low Voltage</b>					
		Any I/O Pin and $\overline{\text{MCLR}}$	V <sub>SS</sub>	—	0.2 V <sub>DD</sub>	V	
		I/O Pins with SDAx, SCLx	V <sub>SS</sub>	—	0.3 V <sub>DD</sub>	V	SMBus disabled
		I/O Pins with SDAx, SCLx	V <sub>SS</sub>	—	0.8	V	SMBus enabled
DI20	V <sub>IH</sub>	<b>Input High Voltage</b>					
		I/O Pins Not 5V Tolerant	0.8 V <sub>DD</sub>	—	V <sub>DD</sub>	V	(Note 3)
		I/O Pins 5V Tolerant and $\overline{\text{MCLR}}$	0.8 V <sub>DD</sub>	—	5.5	V	(Note 3)
		I/O Pins with SDAx, SCLx	0.8 V <sub>DD</sub>	—	5.5	V	SMBus disabled
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled
DI30	ICNPU	<b>Change Notification Pull-up Current</b>	150	250	550	μA	V <sub>DD</sub> = 3.3V, V <sub>PIN</sub> = V <sub>SS</sub>
DI31	ICNPD	<b>Change Notification Pull-Down Current<sup>(4)</sup></b>	20	50	100	μA	V <sub>DD</sub> = 3.3V, V <sub>PIN</sub> = V <sub>DD</sub>

**Note 1:** The leakage current on the  $\overline{\text{MCLR}}$  pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

**2:** Negative current is defined as current sourced by the pin.

**3:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.

**4:** V<sub>IL</sub> source < (V<sub>SS</sub> – 0.3). Characterized but not tested.

**5:** Non-5V tolerant pins V<sub>IH</sub> source > (V<sub>DD</sub> + 0.3), 5V tolerant pins V<sub>IH</sub> source > 5.5V. Characterized but not tested.

**6:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.

**7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

**8:** Any number and/or combination of I/O pins not excluded under I<sub>ICL</sub> or I<sub>ICH</sub> conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

**FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)  
TIMING CHARACTERISTICS**

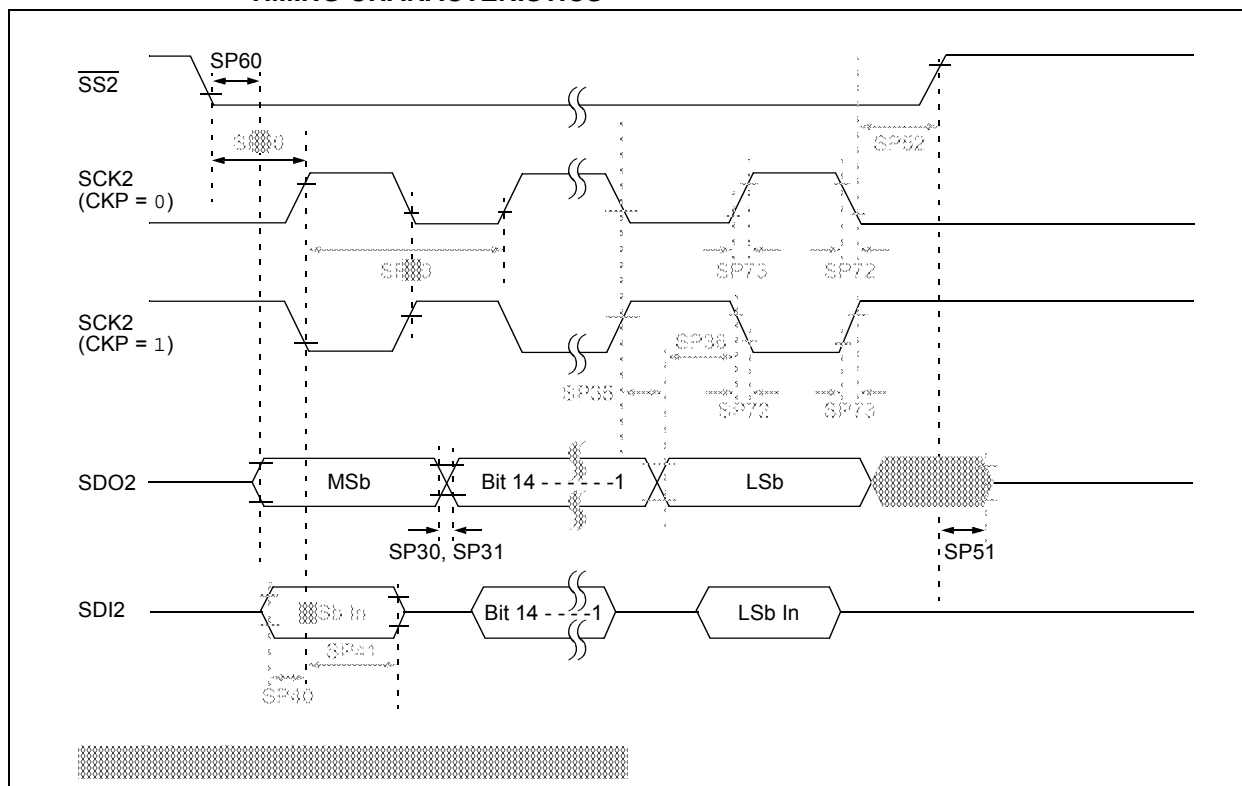


TABLE 30-59: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) <sup>(1)</sup> Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
ADC Accuracy (10-Bit Mode)							
AD20b	Nr	Resolution	10 Data Bits			bits	
AD21b	INL	Integral Nonlinearity	-0.625	—	0.625	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-1.5	—	1.5	LSb	+85°C < TA ≤ +125°C (Note 2)
AD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-0.25	—	0.25	LSb	+85°C < TA ≤ +125°C (Note 2)
AD23b	GERR	Gain Error	-2.5	—	2.5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-2.5	—	2.5	LSb	+85°C < TA ≤ +125°C (Note 2)
AD24b	EOFF	Offset Error	-1.25	—	1.25	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-1.25	—	1.25	LSb	+85°C < TA ≤ +125°C (Note 2)
AD25b	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance (10-Bit Mode)							
AD30b	THD	Total Harmonic Distortion <sup>(3)</sup>	—	64	—	dB	
AD31b	SINAD	Signal to Noise and Distortion <sup>(3)</sup>	—	57	—	dB	
AD32b	SFDR	Spurious Free Dynamic Range <sup>(3)</sup>	—	72	—	dB	
AD33b	FNYQ	Input Signal Bandwidth <sup>(3)</sup>	—	550	—	kHz	
AD34b	ENOB	Effective Number of Bits <sup>(3)</sup>	—	9.4	—	bits	

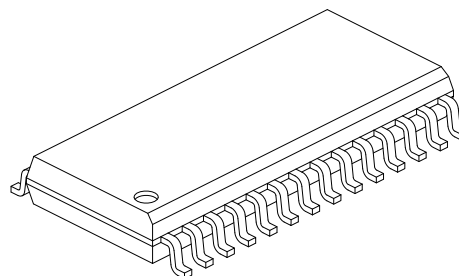
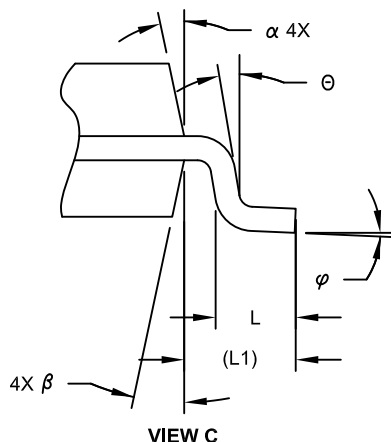
**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

**3:** Parameters are characterized but not tested in manufacturing.

**28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
  - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

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**TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)**

Section Name	Update Description
<b>Section 16.0 “High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)”</b>	Updated the High-Speed PWM Module Register Interconnection Diagram (see Figure 16-2). Added the TRGCONx and TRIGx registers (see Register 16-12 and Register 16-14, respectively).
<b>Section 21.0 “Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)”</b>	Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1).
<b>Section 22.0 “Charge Time Measurement Unit (CTMU)”</b>	Updated the IRNG<1:0> bit value definitions and added Note 2 in the CTMU Current Control Register (see Register 22-3).
<b>Section 25.0 “Op amp/Comparator Module”</b>	Updated the Op amp/Comparator I/O Operating Modes Diagram (see Figure 25-1). Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3). Updated the Digital Filter Interconnect Block Diagram (see Figure 25-4). Added <b>Section 25.1 “Op amp Application Considerations”</b> . Added Note 2 to the Comparator Control Register (see Register 25-2). Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-5).
<b>Section 27.0 “Special Features”</b>	Updated the FICD Configuration Register, updated Note 1, and added Note 3 in the Configuration Byte Register Map (see Table 27-1). Added <b>Section 27.2 “User ID Words”</b> .
<b>Section 30.0 “Electrical Characteristics”</b>	Updated the following Absolute Maximum Ratings: <ul style="list-style-type: none"> <li>Maximum current out of VSS pin</li> <li>Maximum current into VDD pin</li> </ul> Added Note 1 to the Operating MIPS vs. Voltage (see Table 30-1). Updated all Idle Current (IDLE) Typical and Maximum DC Characteristics values (see Table 30-7). Updated all Doze Current (IDOZE) Typical and Maximum DC Characteristics values (see Table 30-9). Added Note 2, removed Parameter CM24, updated the Typical values Parameters CM10, CM20, CM21, CM32, CM41, CM44, and CM45, and updated the Minimum values for CM40 and CM41, and the Maximum value for CM40 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14). Updated Note 2 and the Typical value for Parameter VR310 in the Op amp/Comparator Reference Voltage Settling Time Specifications (see Table 30-15). Added Note 1, removed Parameter VRD312, and added Parameter VRD314 to the Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16). Updated the Minimum, Typical, and Maximum values for Internal LPRC Accuracy (see Table 30-22). Updated the Minimum, Typical, and Maximum values for Parameter SY37 in the Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Timing Requirements (see Table 30-24). The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-35)