

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

⊡XFI

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64mc202t-e-mm

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the dsPIC33EP64MC506 product page of the Microchip web site (www.microchip.com) or select a family reference manual section from the following list.

> In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- "Introduction" (DS70573)
- "CPU" (DS70359)
- "Data Memory" (DS70595)
- "Program Memory" (DS70613)
- "Flash Programming" (DS70609)
- "Interrupts" (DS70600)
- "Oscillator" (DS70580)
- "Reset" (DS70602)
- "Watchdog Timer and Power-Saving Modes" (DS70615)
- "I/O Ports" (DS70598)
- "Timers" (DS70362)
- "Input Capture" (DS70352)
- "Output Compare" (DS70358)
- "High-Speed PWM" (DS70645)
- "Quadrature Encoder Interface (QEI)" (DS70601)
- "Analog-to-Digital Converter (ADC)" (DS70621)
- "UART" (DS70582)
- "Serial Peripheral Interface (SPI)" (DS70569)
- "Inter-Integrated Circuit (I²C[™])" (DS70330)
- "Enhanced Controller Area Network (ECAN™)" (DS70353)
- "Direct Memory Access (DMA)" (DS70348)
- "CodeGuard™ Security" (DS70634)
- "Programming and Diagnostics" (DS70608)
- "Op Amp/Comparator" (DS70357)
- "Programmable Cyclic Redundancy Check (CRC)" (DS70346)
- "Device Configuration" (DS70618)
- "Peripheral Trigger Generator (PTG)" (DS70669)
- "Charge Time Measurement Unit (CTMU)" (DS70661)

TABLE 4	-1:	CPU C	ORE RE	GISTE	R MAP F	OR dsF	PIC33EP	XXXMC	20X/50X	AND d	sPIC33I	EPXXX	GP50X	DEVICE	S ONL	(CON	TINUE	D)
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	Ν	OV	Z	С	0000
CORCON	0044	VAR	_	US<	1:0>	EDT		DL<2:0>		SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020
MODCON	0046	XMODEN	YMODEN	_	_		BWM	<3:0>			YWM<	:3:0>			XWM<	3:0>		0000
XMODSRT	0048							XMC	DSRT<15:0	>							_	0000
XMODEND	004A							XMC	DEND<15:0)>							_	0001
YMODSRT	004C							YMC	DSRT<15:0	>								0000
YMODEND	004E							YMC	DEND<15:0)>								0001
XBREV	0050	BREN							XBF	REV<14:0>								0000
DISICNT	0052	_	_							DISICNT<	13:0>							0000
TBLPAG	0054		_	_	_	_	_	_	_				TBLPA	G<7:0>				0000
MSTRPR	0058								MSTRPR<	:15:0>								0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

DS70000657H-page 64

TABLE 4-52: PORTG REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E60			—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6				—	—		03C0
PORTG	0E62	_	_	_	_	_	_	RG9	RG8	RG7	RG6	_	_	_	_	_	_	xxxx
LATG	0E64	_	_	_	_	_	_	LATG9	LATG8	LATG7	LATG6	_	_	_	_	_	_	xxxx
ODCG	0E66			—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6				—	—		0000
CNENG	0E68	_	_	_	_	_	_	CNIEG9	CNIEG8	CNIEG7	CNIEG6	_	_	_	_	_	_	0000
CNPUG	0E6A	_	_	_	_	_	_	CNPUG9	CNPUG8	CNPUG7	CNPUG6	_	_	_	_	_	_	0000
CNPDG	0E6C	_	_	_	_	_	_	CNPDG9	CNPDG8	CNPDG7	CNPDG6	_	_		—	—	_	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-56: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00			—			—		TRISA8				TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	011F
PORTA	0E02		-	—	-	-	—	-	RA8	_	_	-	RA4	RA3	RA2	RA1	RA0	0000
LATA	0E04	_	_	_	_	_	_	_	LATA8	_	_	_	LATA4	LATA3	LATA2	LA1TA1	LA0TA0	0000
ODCA	0E06	_	_	_	_	_	_	_	ODCA8	_	_	_	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
CNENA	0E08	_	_	_	_	_	_	_	CNIEA8	_	_	_	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
CNPUA	0E0A	_	_	_	_	_	_	_	CNPUA8	_	_	_	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
CNPDA	0E0C	_	_	_	_	_	_	_	CNPDA8	_	_	_	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
ANSELA	0E0E			—			—		_	_			ANSA4		-	ANSA1	ANSA0	0013

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-57: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	0E12	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	0E14	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
ODCB	0E16	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
CNENB	0E18	CNIEB15	CNIEB14	CNIEB13	CNIEB12	CNIEB11	CNIEB10	CNIEB9	CNIEB8	CNIEB7	CNIEB6	CNIEB5	CNIEB4	CNIEB3	CNIEB2	CNIEB1	CNIEB0	0000
CNPUB	0E1A	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
CNPDB	0E1C	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
ANSELB	0E1E	_	_	_	_	_	_	_	ANSB8	_	_	_	_	ANSB3	ANSB2	ANSB1	ANSB0	010F

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-58: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	_	—	_	—	—	—	TRISC8	_	—	—	—	—	—	TRISC1	TRISC0	0103
PORTC	0E22	—	_	—	_	_	_	_	RC8		—	_	_	_	_	RC1	RC0	xxxx
LATC	0E24	—	_	—	_	—	—	—	LATC8		_	—	—	—	_	LATC1	LATC0	xxxx
ODCC	0E26	—	_	—	_	—	—	—	ODCC8		_	—	—	—	_	ODCC1	ODCC0	0000
CNENC	0E28	—	_	—	_	—	—	—	CNIEC8		_	—	—	—	_	CNIEC1	CNIEC0	0000
CNPUC	0E2A	—	_	—	_	—	—	—	CNPUC8		_	—	—	—	_	CNPUC1	CNPUC0	0000
CNPDC	0E2C	—	_	—	_	—	—	—	CNPDC8		_	—	—	—	_	CNPDC1	CNPDC0	0000
ANSELC	0E2E	_	_	_	_	_	_	_	_	_	_	_	_	_		ANSC1	ANSC0	0003

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.6.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than, or greater than, the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note: The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed but the contents of the register remain unchanged.

4.7 Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.7.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when all these conditions are met:

- BWMx bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^{N}$ bytes, the last 'N' bits of the data buffer start address must be zeros.

XBREV<14:0> is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:	All bit-reversed EA calculations assume
	word-sized data (LSb of every EA is always
	clear). The XBREVx value is scaled
	accordingly to generate compatible (byte)
	addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XBREVx) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note: Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

REGISTER 5-2: NV	MADRH: NONVOLATILE MEMORY ADDRESS REGISTER HIGH
------------------	-------------------------------------------------

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	_
bit 15			•	•	•		bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMAD	R<23:16>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unki	nown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 **NVMADR<23:16>:** Nonvolatile Memory Write Address High bits Selects the upper 8 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

REGISTER 5-3: NVMADRL: NONVOLATILE MEMORY ADDRESS REGISTER LOW

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMA	DR<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	mented bit, rea	id as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 NVMADR<15:0>: Nonvolatile Memory Write Address Low bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
			NVMK	EY<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set	٤	'0' = Bit is cle	eared	x = Bit is unk	nown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 **NVMKEY<7:0>:** Key Register (write-only) bits

R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
GIE	DISI	SWTRAP		_	_	_	—
bit 15				·			bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
		_	_	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0
Legend:	L:1		L:1			(0)	
R = Readable	DIT	vv = vvritable	DIT		mented bit, read	as '0'	
-n = value at I	POR	"1" = Bit is set		$0^{\circ} = Bit is cle$	eared	x = Bit is unkr	nown
hit 15		ntorrunt Enable	, hit				
DIL 15		and associate	d IF hits are e	nahled			
	0 = Interrupts	are disabled,	but traps are s	still enabled			
bit 14	DISI: DISI Ir	nstruction Statu	s bit				
	1 = DISI ins	truction is activ	e				
	0 = DISI ins i	truction is not a	ictive				
bit 13	SWTRAP: So	oftware Trap St	atus bit				
	1 = Software	trap is enabled	4				
hit 12-3		ted: Read as '	 				
bit 2	INT2FP: Exte	ernal Interrupt 2	∘ PEdge Detect	Polarity Selec	et bit		
	1 = Interrupt	on negative ed	ae				
	0 = Interrupt	on positive edg	le				
bit 1	INT1EP: Exte	ernal Interrupt ?	Edge Detect	Polarity Selec	ct bit		
	1 = Interrupt	on negative ed	ge				
	0 = Interrupt	on positive edg	e				
bit 0	INTOEP: Exte	ernal Interrupt () Edge Detect	Polarity Selec	ct bit		
	\perp = interrupt	on negative ed	ye Ie				

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2



8.1 DMA Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

8.1.1 KEY RESOURCES

- Section 22. "Direct Memory Access (DMA)" (DS70348) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- · Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

8.2 DMAC Registers

Each DMAC Channel x (where x = 0 through 3) contains the following registers:

- 16-Bit DMA Channel Control register (DMAxCON)
- 16-Bit DMA Channel IRQ Select register (DMAxREQ)
- 32-Bit DMA RAM Primary Start Address register (DMAxSTA)
- 32-Bit DMA RAM Secondary Start Address register (DMAxSTB)
- 16-Bit DMA Peripheral Address register (DMAxPAD)
- 14-Bit DMA Transfer Count register (DMAxCNT)

Additional status registers (DMAPWC, DMARQC, DMAPPS, DMALCA and DSADR) are common to all DMAC channels. These status registers provide information on write and request collisions, as well as on last address and channel access information.

The interrupt flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding interrupt enable control bits (DMAxIE) are located in an IECx register in the interrupt controller, and the corresponding interrupt priority control bits (DMAxIP) are located in an IPCx register in the interrupt controller.

15.0 OUTPUT COMPARE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual" for OCxR and OCxRS register restrictions.





dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

REGISTER 17-7: VEL1CNT: VELOCITY COUNTER 1 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			VELC	NT<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			VELC	NT<7:0>			
bit 7							bit 0
Legend:							
R = Readable b	oit	W = Writable b	bit	U = Unimplem	nented bit, read	l as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown

bit 15-0 VELCNT<15:0>: Velocity Counter bits

REGISTER 17-8: INDX1CNTH: INDEX COUNTER 1 HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCN	T<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXCN	T<23:16>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 INDXCNT<31:16>: High Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits

REGISTER 17-9: INDX1CNTL: INDEX COUNTER 1 LOW WORD REGISTER

'1' = Bit is set

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXC	NT<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			INDXC	NT<7:0>			
bit 7							bit 0
Legend:							
R = Readable b	it	W = Writable bit	:	U = Unimpler	mented bit, read	l as '0'	

'0' = Bit is cleared

bit 15-0 INDXCNT<15:0>: Low Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits

-n = Value at POR

x = Bit is unknown

						D 444 A	
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
-	—	—	DISSCK	DISSDO	MODE16	SMP	CKE
bit 15							bit 8
				DAMA		DAM 0	
	2) R/VV-U	R/W-U		R/W-U	R/W-0		R/W-0
55EIN		MSTEN	SPRE2(*)	SPRET	SPREU	PPRET	PPREU
DIL 7							DILU
Legend:							
R = Read	able bit	W = Writable	bit	U = Unimpler	mented bit read	1 as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
			•	0 2.1.10 0.10			
bit 15-13	Unimplemer	nted: Read as '	0'				
bit 12	DISSCK: Dis	able SCKx Pin	bit (SPIx Mas	ter modes only	<i>'</i>)		
	1 = Internal S	SPIx clock is dis	sabled, pin fun	ctions as I/O			
	0 = Internal S	SPIx clock is er	abled				
bit 11	DISSDO: Dis	able SDOx Pir	ı bit				
	1 = SDOx pir	n is not used by	the module; p	oin functions as	s I/O		
bit 10		ord/Byte Com	y the moutle	oct bit			
	1 = Commun	ication is word	wide (16 bits)				
	0 = Commun	ication is byte-	wide (8 bits)				
bit 9	SMP: SPIx D	ata Input Sam	ole Phase bit				
	Master mode	<u>):</u>					
	1 = Input dat	a is sampled at	end of data of	utput time			
	0 – Input data Slave mode:	a is sampled at		a output time			
	SMP must be	e cleared when	SPIx is used i	n Slave mode.			
bit 8	CKE: SPIx C	lock Edge Sele	ect bit ⁽¹⁾				
	1 = Serial ou	tput data chang	ges on transitio	on from active	clock state to Id	lle clock state (i	refer to bit 6)
	0 = Serial ou	tput data chang	ges on transitio	on from Idle clo	ock state to activ	ve clock state (refer to bit 6)
bit 7	SSEN: Slave	Select Enable	bit (Slave mo	de) ⁽²⁾			
	$1 = \frac{SSx}{SSx}$ pin is	s used for Slav	e mode he module: nir	is controlled h	ov port function		
bit 6	CKP: Clock F	Polarity Select	hit		by port function		
bito	1 = Idle state	for clock is a h	iiah level: activ	ve state is a low	v level		
	0 = Idle state	for clock is a l	ow level; active	e state is a higl	h level		
bit 5	MSTEN: Mas	ster Mode Enat	ole bit				
	1 = Master m	node					
	0 = Slave mo	ode					
Note 1:	The CKE bit is not	used in Frame	d SPI modes. I	Program this bi	t to '0' for Fram	ed SPI modes (FRMEN = 1).
2:	This bit must be c	leared when FF	RMEN = 1.				

REGISTER 18-2: SPIXCON1: SPIX CONTROL REGISTER 1

- **3:** Do not set both primary and secondary prescalers to the value of 1:1.

20.3 UARTx Control Registers

REGISTER 20-1: UXMODE: UARTX MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0		
UARTEN ⁽	¹⁾ —	USIDL	IREN ⁽²⁾	RTSMD	—	UEN1	UEN0		
bit 15	bit 8						bit 8		
R/W-0, H	C R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL		
bit 7							bit 0		
Legend:		HC = Hardwa	re Clearable bi	t					
R = Reada	ıble bit	W = Writable	bit	U = Unimplem	ented bit, read	as '0'			
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown		
bit 15	UARTEN: UA 1 = UARTx is 0 = UARTx is minimal	RTx Enable bits enabled; all U disabled; all L	(1) ARTx pins are IARTx pins are	controlled by U controlled by F	ARTx as define ORT latches; L	ed by UEN<1:0 JARTx power c	> onsumption is		
bit 14	Unimplemen	ted: Read as ')'						
bit 13	USIDL: UART	Tx Stop in Idle I	Mode bit						
	1 = Discontin 0 = Continue	ues module op s module opera	eration when c ation in Idle mo	levice enters Id de	le mode				
bit 12	IREN: IrDA [®] I 1 = IrDA enc 0 = IrDA enc	Encoder and Do oder and decoo	ecoder Enable ler are enablec ler are disable	bit ⁽²⁾ 1 d					
bit 11	RTSMD: Mod 1 = $\overline{\text{UxRTS}}$ p 0 = $\overline{\text{UxRTS}}$ p	le Selection for in is in Simplex in is in Flow Co	UxRTS Pin bit mode ontrol mode						
bit 10	Unimplemen	ted: Read as ')'						
bit 9-8	UEN<1:0>: U	ARTx Pin Enat	ole bits						
	11 = UxTX, U 10 = UxTX, U 01 = UxTX, U 00 = UxTX an PORT la	JxRX and BCLF JxRX, UxCTS a JxRX and UxRT nd UxRX pins a atches	Xx pins are ena nd UxRTS pins S pins are ena are enabled ar	bled and used; s are enabled a bled and <u>used;</u> nd used; UxCTS	UxCTS pin is c nd used ⁽⁴⁾ UxCT <u>S pin is c</u> S and UxRTS/B	ontrolled by PC ontrolled by PC SCLKx pins are	DRT latches ⁽³⁾ DRT latches ⁽⁴⁾ controlled by		
bit 7	WAKE: Wake	e-up on Start bit	Detect During	Sleep Mode Er	nable bit				
	1 = UARTx c in hardwa 0 = No wake	ontinues to sar are on the follov -up is enabled	nple the UxRX wing rising edg	pin; interrupt is e	generated on t	he falling edge	; bit is cleared		
bit 6	LPBACK: UA	RTx Loopback	Mode Select b	bit					
	1 = Enables	Loopback mod	9						
	0 = Loopbacl	k mode is disat	led						
Note 1:	Refer to the "UAF enabling the UAR	RT " (DS70582) Tx module for r	section in the " eceive or transi	dsPIC33/PIC24 mit operation.	Family Referen	ce Manual" for i	nformation on		
2:	This feature is on	ly available for	the 16x BRG r	node (BRGH =	0).				
3:	This feature is on	ly available on	44-pin and 64-	s feature is only available on 44-pin and 64-pin devices.					

4: This feature is only available on 64-pin devices.





21.5 ECAN Message Buffers

ECAN Message Buffers are part of RAM memory. They are not ECAN Special Function Registers. The user application must directly write into the RAM area that is configured for ECAN Message Buffers. The location and size of the buffer area is defined by the user application.

BUFFER 21-1: ECAN™ MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	_	_	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE
bit 7							bit 0
[
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-13	Unimplemen	ted: Read as '	0'				
bit 12-2	SID<10:0>: S	tandard Identif	ier bits				
bit 1	SRR: Substitu	ute Remote Re	quest bit				
	When IDE = 0):					
	1 = Message	will request re	mote transmis	ssion			
	0 = Normal m	essage					
	When IDE = 1	<u>L:</u>					
	The SRR bit r	nust be set to '	1'.				
bit 0	IDE: Extende	d Identifier bit					
	1 = Message	will transmit Ex	ktended Ident	ifier			
	0 = Message will transmit Standard Identifier						

BUFFER 21-2: ECAN™ MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—		EID17	EID16	EID15	EID14
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID13	EID12	EID11	EID10	EID9	EID8	EID7	EID6
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimpler	mented bit, read	as '0'	
-n = Value at POR '1' = Bit is set '0'		'0' = Bit is cle	ared	x = Bit is unkr	nown		

bit 15-12 Unimplemented: Read as '0'

bit 11-0 EID<17:6>: Extended Identifier bits

TABLE 30-37:SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP70	FscP	Maximum SCK2 Input Frequency	-	—	Lesser of FP or 15	MHz	(Note 3)	
SP72	TscF	SCK2 Input Fall Time	—	_	_	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO2 Data Output Rise Time	_	—	—	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	_	—	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	_	_	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns		
SP51	TssH2doZ	SS2 ↑ to SDO2 Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH TscL2ssH	SS2 ↑ after SCK2 Edge	1.5 Tcy + 40	_	_	ns	(Note 4)	
SP60	TssL2doV	SDO2 Data Output Valid after SS2 Edge	-	—	50	ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.



FIGURE 30-28: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	Ν	IILLIMETER	S
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		44	
Pitch	е		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension. usually without tolerance. for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

Revision C (December 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see Section 20.1 "UART Helpful Tips" and Section 3.6 "CPU Resources". All occurrences of TLA were updated to VTLA throughout the document, with the exception of the pin diagrams (updated diagrams were not available at time of publication).

A new chapter, Section 31.0 "DC and AC Device Characteristics Graphs", was added.

All other major changes are referenced by their respective section in Table A-2.

Section Name	Update Description
"16-bit Microcontrollers and Digital Signal Controllers (up to 256-Kbyte Flash and 32-Kbyte SRAM) with High- Speed PWM, Op amps, and Advanced Analog"	The content on the first page of this section was extensively reworked to provide the reader with the key features and functionality of this device family in an "at-a-glance" format.
Section 1.0 "Device Overview"	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X Block Diagram (see Figure 1-1), which now contains a CPU block and a reference to the CPU diagram. Updated the description and Note references in the Pinout I/O Descriptions for these pins: C1IN2- C2IN2- C3IN2- OA1OUT OA2OUT and OA3OUT (see Table 1-1)
Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"	Updated the Recommended Minimum Connection diagram (see Figure 2-1).
Section 3.0 "CPU"	Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X CPU Block Diagram (see Figure 3-1). Updated the Status register definition in the Programmer's Model (see Figure 3-2).
Section 4.0 "Memory Organization"	Updated the Data Memory Maps (see Figure 4-6 and Figure 4-11). Removed the DCB<1:0> bits from the OC1CON2, OC2CON2, OC3CON2, and OC4CON2 registers in the Output Compare 1 Through Output Compare 4 Register Map (see Table 4-10). Added the TRIG1 and TRGCON1 registers to the PWM Generator 1 Register Map (see Table 4-13). Added the TRIG2 and TRGCON2 registers to the PWM Generator 2 Register Map (see Table 4-14). Added the TRIG3 and TRGCON3 registers to the PWM Generator 3 Register Map (see Table 4-15). Updated the second note in Section 4.7.1 "Bit-Reversed Addressing Implementation".
Section 8.0 "Direct Memory Access (DMA)"	Updated the DMA Controller diagram (see Figure 8-1).
Section 14.0 "Input Capture"	Updated the bit values for the ICx clock source of the ICTSEL<12:10> bits in the ICxCON1 register (see Register 14-1).
Section 15.0 "Output Compare"	Updated the bit values for the OCx clock source of the OCTSEL<2:0> bits in the OCxCON1 register (see Register 15-1). Removed the DCB<1:0> bits from the Output Compare x Control Register 2 (see Register 15-2).

TABLE A-2: MAJOR SECTION UPDATES

Revision E (April 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

TABLE A-4:	MAJOR SECTION UPDATES
------------	-----------------------

Section Name	Update Description
"16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High- Speed PWM, Op amps, and Advanced Analog"	The following 512-Kbyte devices were added to the General Purpose Families table (see Table 1): PIC24EP512GP202 PIC24EP512GP204 PIC24EP512GP206 dsPIC33EP512GP502 dsPIC33EP512GP506 The following 512-Kbyte devices were added to the Motor Control Families table (see Table 2): PIC24EP512MC202 PIC24EP512MC204 PIC24EP512MC206 dsPIC33EP512MC202 dsPIC33EP512MC202 dsPIC33EP512MC204 dsPIC33EP512MC204 dsPIC33EP512MC206 dsPIC33EP512MC206 dsPIC33EP512MC506
Section 4.0 "Memory Organization"	Added a Program Memory Map for the new 512-Kbyte devices (see Figure 4-4). Added a Data Memory Map for the new dsPIC 512-Kbyte devices (see Figure 4-11). Added a Data Memory Map for the new PIC24 512-Kbyte devices (see Figure 4-16).
Section 7.0 "Interrupt Controller"	Updated the VECNUM bits in the INTTREG register (see Register 7-7).
Section 11.0 "I/O Ports"	Added tip 6 to Section 11.5 "I/O Helpful Tips".
Section 27.0 "Special Features"	 The following modifications were made to the Configuration Byte Register Map (see Table 27-1): Added the column Device Memory Size (Kbytes) Removed Notes 1 through 4 Added addresses for the new 512-Kbyte devices
Section 30.0 "Electrical Characteristics"	Updated the Minimum value for Parameter DC10 (see Table 30-4). Added Power-Down Current (Ipd) parameters for the new 512-Kbyte devices (see Table 30-8). Updated the Minimum value for Parameter CM34 (see Table 30-53). Updated the Minimum and Maximum values and the Conditions for parameter SY12 (see Table 30-22).