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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64mc202t-e-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





#### TABLE 4-42: OP AMP/COMPARATOR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	PSIDL	—	—	—	C4EVT	C3EVT	C2EVT	C1EVT	—	-	—	—	C4OUT	C3OUT	C2OUT	C10UT	0000
CVRCON	0A82	—	CVR2OE	_	_	_	VREFSEL	_	—	CVREN	CVR10E	CVRR	CVRSS		CVR<	3:0>		0000
CM1CON	0A84	CON	COE	CPOL	—		OPMODE	CEVT	COUT	EVPO	_<1:0>	—	CREF		_	CCH	<1:0>	0000
CM1MSKSRC	0A86		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A		—		—		—		—		C	FSEL<2:0	>	CFLTREN	0	CFDIV<2:0	>	0000
CM2CON	0A8C	CON	COE	CPOL	—		OPMODE	CEVT	COUT	EVPO	_<1:0>	—	CREF		_	CCH	<1:0>	0000
CM2MSKSRC	0A8E		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92		—		—		—		—		C	FSEL<2:0	>	CFLTREN	0	CFDIV<2:0	>	0000
CM3CON <sup>(1)</sup>	0A94	CON	COE	CPOL	—		OPMODE	CEVT	COUT	EVPO	_<1:0>	—	CREF		_	CCH	<1:0>	0000
CM3MSKSRC(1)	0A96		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM3MSKCON <sup>(1)</sup>	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR <sup>(1)</sup>	0A9A	_	_	_	_	_	_	_	_	_	C	FSEL<2:0	>	CFLTREN	(	CFDIV<2:0	>	0000
CM4CON	0A9C	CON	COE	CPOL	_	_	_	CEVT	COUT	EVPO	_<1:0>	_	CREF	_	_	CCH	<1:0>	0000
CM4MSKSRC	0A9E		—		—		SELSR	CC<3:0>			SELSRC	B<3:0>			SELSRC	A<3:0>		0000
CM4MSKCON	0AA0	HLMS	_	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM4FLTR	0AA2	_	—	—	—	—	-	—	_	—	C	FSEL<2:0	>	CFLTREN	(	CFDIV<2:0	>	0000

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are unavailable on dsPIC33EPXXXGP502/MC502/MC502/MC202 and PIC24EP256GP/MC202 (28-pin) devices.

#### TABLE 4-43: CTMU REGISTER MAP

File	Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTML	JCON1	033A	CTMUEN	-	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	-	—			—	—	0000
CTML	JCON2	033C	EDG1MOD	EDG1POL		EDG1	SEL<3:0>		EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL		EDG2S	EL<3:0>		_		0000
CTML	JICON	033E			ITRIM<5	5:0>			IRNG	6<1:0>	—	_		_	_	_			0000

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

### TABLE 4-44: JTAG INTERFACE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
JDATAH	0FF0	—	_	—	—		JDATAH<27:16> x							xxxx				
JDATAL	0FF2					JDATAL<15:0> 00/							0000					

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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#### EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.

# 5.0 FLASH PROGRAM MEMORY

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXGP/MC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Flash Programming" (DS70609) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/ 50X and PIC24EPXXXGP/MC20X devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data a single program memory word, and erase program memory in blocks or 'pages' of 1024 instructions (3072 bytes) at a time.

# 5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

#### FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS

![](_page_4_Figure_16.jpeg)

#### REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

- bit 4-0 SYNCSEL<4:0>: Input Source Select for Synchronization and Trigger Operation bits<sup>(4)</sup>
  - 11111 = No Sync or Trigger source for ICx
  - 11110 = Reserved
  - 11101 = Reserved
  - 11100 = CTMU module synchronizes or triggers ICx
  - 11011 = ADC1 module synchronizes or triggers  $ICx^{(5)}$
  - 11010 = CMP3 module synchronizes or triggers  $ICx^{(5)}$
  - $11001 = CMP2 \text{ module synchronizes or triggers ICx}^{(5)}$
  - 11000 = CMP1 module synchronizes or triggers  $ICx^{(5)}$
  - 10111 = Reserved
  - 10110 = Reserved
  - 10101 = Reserved
  - 10100 = Reserved
  - 10011 = IC4 module synchronizes or triggers ICx
  - 10010 = IC3 module synchronizes or triggers ICx
  - 10001 = IC2 module synchronizes or triggers ICx
  - 10000 = IC1 module synchronizes or triggers ICx
  - 01111 = Timer5 synchronizes or triggers ICx
  - 01110 = Timer4 synchronizes or triggers ICx
  - 01101 = Timer3 synchronizes or triggers ICx (default)
  - 01100 = Timer2 synchronizes or triggers ICx
  - 01011 = Timer1 synchronizes or triggers ICx
  - 01010 = PTGOx module synchronizes or triggers  $ICx^{(6)}$
  - 01001 = Reserved
  - 01000 = Reserved
  - 00111 = Reserved
  - 00110 = Reserved
  - 00101 = Reserved
  - 00100 = OC4 module synchronizes or triggers ICx
  - 00011 = OC3 module synchronizes or triggers ICx
  - 00010 = OC2 module synchronizes or triggers ICx
  - 00001 = OC1 module synchronizes or triggers ICx
  - 00000 = No Sync or Trigger source for ICx
- **Note 1:** The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.
  - 2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
  - **3:** This bit is set by the selected input source (selected by SYNCSEL<4:0> bits). It can be read, set and cleared in software.
  - 4: Do not use the ICx module as its own Sync or Trigger source.
  - 5: This option should only be selected as a trigger source and not as a synchronization source.
  - Each Input Capture x (ICx) module has one PTG input source. See Section 24.0 "Peripheral Trigger Generator (PTG) Module" for more information.
     PTGO8 = IC1

PTGO9 = IC2 PTGO10 = IC3 PTGO11 = IC4

## REGISTER 17-1: QEI1CON: QEI1 CONTROL REGISTER (CONTINUED)

bit 6-4	<b>INTDIV&lt;2:0&gt;:</b> Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select) <sup>(3)</sup>
	<pre>111 = 1:128 prescale value 110 = 1:64 prescale value 101 = 1:32 prescale value 100 = 1:16 prescale value 011 = 1:8 prescale value 010 = 1:4 prescale value 001 = 1:2 prescale value 000 = 1:1 prescale value</pre>
bit 3	<b>CNTPOL:</b> Position and Index Counter/Timer Direction Select bit
	<ul> <li>0 = Counter direction is positive unless modified by external up/down signal</li> </ul>
bit 2	GATEN: External Count Gate Enable bit
	<ul> <li>1 = External gate signal controls position counter operation</li> <li>0 = External gate signal does not affect position counter/timer operation</li> </ul>
bit 1-0	CCM<1:0>: Counter Control Mode Selection bits
	<ul> <li>11 = Internal Timer mode with optional external count is selected</li> <li>10 = External clock count with optional external count is selected</li> <li>01 = External clock count with external up/down direction is selected</li> <li>00 = Quadrature Encoder Interface (x4 mode) Count mode is selected</li> </ul>
Note 1:	When CCM<1:0> = 10 or 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

- 2: When CCM<1:0> = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.
- 3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

![](_page_7_Figure_1.jpeg)

#### FIGURE 18-1: SPIX MODULE BLOCK DIAGRAM

# 19.1 I<sup>2</sup>C Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

### 19.1.1 KEY RESOURCES

- "Inter-Integrated Circuit (I<sup>2</sup>C)" (DS70330) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

#### 20.1 UART Helpful Tips

- 1. In multi-node, direct-connect UART networks, receive inputs UART react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
  - a) If URXINV = 0, use a pull-up resistor on the RX pin.
  - b) If URXINV = 1, use a pull-down resistor on the RX pin.
- 2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UARTx module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

#### 20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

#### 20.2.1 KEY RESOURCES

- "UART" (DS70582) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN <sup>(1)</sup>	UTXBF	TRMT
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7				-			bit 0
Legend:		HC = Hardwar	e Clearable bit	C = Clearable	e bit		
R = Readable	e bit	W = Writable b	bit	U = Unimpler	mented bit, read	d as '0'	

#### **REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER**

		0 – Onimplemented bit, rea	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: UARTx Transmit Polarity Inversion bit
  - If IREN = 0: 1 = UxTX Idle state is '0'
    - 0 = UxTX Idle state is '1'
    - If IREN = 1:
  - 1 = IrDA encoded, UxTX Idle state is '1'
  - 0 = IrDA encoded, UxTX Idle state is '0'
- bit 12 Unimplemented: Read as '0'
- bit 11 UTXBRK: UARTx Transmit Break bit
  - 1 = Sends Sync Break on next transmission Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
  - 0 = Sync Break transmission is disabled or completed
- **UTXEN:** UARTx Transmit Enable bit<sup>(1)</sup> bit 10 1 = Transmit is enabled, UxTX pin is controlled by UARTx
  - 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; UxTX pin is controlled by the PORT
- bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
  - 1 = Transmit buffer is full
  - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
  - 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
  - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
  - 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
  - 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
  - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters
- Note 1: Refer to the "UART" (DS70582) section in the "dsPIC33/PIC24 Family Reference Manual" for information on enabling the UARTx module for transmit operation.

### REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5	<ul> <li>ADDEN: Address Character Detect bit (bit 8 of received data = 1)</li> <li>1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect</li> <li>0 = Address Detect mode is disabled</li> </ul>
bit 4	RIDLE: Receiver Idle bit (read-only) 1 = Receiver is Idle 0 = Receiver is active
bit 3	<b>PERR:</b> Parity Error Status bit (read-only) 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected
bit 2	<pre>FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 0 = Framing error has not been detected</pre>
bit 1	<ul> <li>OERR: Receive Buffer Overrun Error Status bit (clear/read-only)</li> <li>1 = Receive buffer has overflowed</li> <li>0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the UxRSR to the empty state</li> </ul>
bit 0	<ul> <li>URXDA: UARTx Receive Buffer Data Available bit (read-only)</li> <li>1 = Receive buffer has data, at least one more character can be read</li> <li>0 = Receive buffer is empty</li> </ul>

**Note 1:** Refer to the **"UART"** (DS70582) section in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM	5 ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0
bit 15	·	·					bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—	—	—	—	_	_	—
bit 7							bit 0
Legend:							
R = Read	able bit	W = Writable b	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value	e at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	iown
bit 15-10	ITRIM<5:0>:	Current Source	Trim bits				
	011111 <b>= Ma</b>	aximum positive	change from	nominal curren	t + 62%		
	011110 <b>= Ma</b>	aximum positive	change from	nominal curren	t + 60%		
	•						
	•						
	•						
	000010 = Mii	nimum positive (	change from r	nominal current	+ 4% + 2%		
	000000 = No	minal current ou	utput specified	bv IRNG<1:0>	>		
	111111 = Mir	nimum negative	change from	nominal curren	nt – 2%		
	111110 <b>= Mi</b> i	nimum negative	change from	nominal curren	nt – 4%		
	•						
	•						
	•						
	100010 = Ma 100001 = Ma	aximum negative aximum negative	e change from e change from	nominal curre	nt – 60% nt – 62%		
bit 9-8	IRNG<1:0>: (	Current Source	Range Select	bits			
	11 = 100 × Ba	ase Current <sup>(2)</sup>					
	$10 = 10 \times Bas$	se Current <sup>(2)</sup>					
	$01 = Base CL00 = 1000 \times F$	Base Current(1,2	)				
bit 7-0	Unimplemen	ted: Read as '0	3				
Note 1:	This current range	e is not available	a to be used w	with the internal	temperature n	neasurement di	ode
						icasurement u	000.

#### REGISTER 22-3: CTMUICON: CTMU CURRENT CONTROL REGISTER

2: Refer to the CTMU Current Source Specifications (Table 30-56) in Section 30.0 "Electrical Characteristics" for the current range selection values.

![](_page_13_Figure_1.jpeg)

![](_page_13_Figure_2.jpeg)

#### REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNEL 1, 2, 3 SELECT REGISTER (CONTINUED)

bit 0

**CH123SA:** Channel 1, 2, 3 Positive Input Select for Sample MUXA bit In 12-bit mode (AD21B = 1), CH123SA is Unimplemented and is Read as '0':

Value	ADC Channel							
value	CH1	CH2	CH3					
1 <b>(2)</b>	OA1/AN3	OA2/AN0	OA3/AN6					
0 <b>(1,2)</b>	OA2/AN0	AN1	AN2					

**Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.

# REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGA	DJ<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGA	DJ<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		U = Unimpler	nented bit, rea	d as '0'			
-n = Value at POR '1' = Bit is set			'0' = Bit is cle	ared	x = Bit is unkr	nown	

bit 15-0 **PTGADJ<15:0>:** PTG Adjust Register bits This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the PTGADD command.

# REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGLC	<15:8>			
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGL	0<7:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 15-0 PTGL0<15:0>: PTG Literal 0 Register bits

This register holds the 16-bit value to be written to the AD1CHS0 register with the  ${\tt PTGCTRL}$  Step command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		—	DWIDTH4	DWIDTH3	DWIDTH2	DWIDTH1	DWIDTH0
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		—	PLEN4	PLEN3	PLEN2	PLEN1	PLEN0
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimpler	nented bit, read	as '0'		
-n = Value at F	-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown			nown
bit 15-13	Unimplemen	ted: Read as '	0'				
bit 12-8	bit 12-8 DWIDTH<4:0>: Data Width Select bits						
These bits set the width of the data word (DWIDTH<4:0> + 1).							
bit 7-5 Unimplemented: Read as '0'							

#### REGISTER 26-2: CRCCON2: CRC CONTROL REGISTER 2

bit 4-0 **PLEN<4:0>:** Polynomial Length Select bits

These bits set the length of the polynomial (Polynomial Length = PLEN<4:0> + 1).

#### 31.2 **AC Characteristics and Timing Parameters**

The information contained in this section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in Section 30.2 "AC Characteristics and Timing Parameters", with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in Section 30.2 "AC Characteristics and Timing Parameters" is the Industrial and Extended temperature equivalent of HOS53.

### TABLE 31-9: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

	Standard Operating Conditions: 3.0V to 3.6V
	(unless otherwise stated)
AC CHARACTERISTICS	Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$
	Operating voltage VDD range as described in Table 31-1.

#### **FIGURE 31-1:** LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

![](_page_17_Figure_7.jpeg)

#### TABLE 31-10: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$				
Param No.	Symbol	Characteristic	Min Typ Max Units Conditions				Conditions
HOS53	DCLK	CLKO Stability (Jitter) <sup>(1)</sup>	-5	0.5	5	%	Measured over 100 ms period

These parameters are characterized by similarity, but are not tested in manufacturing. This specification is Note 1: based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks use this formula:

$$Peripheral Clock Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Peripheral Bit Rate Clock}}}$$

For example: FOSC = 32 MHz, DCLK = 5%, SPIx bit rate clock (i.e., SCKx) is 2 MHz. Г

$$SPI SCK Jitter = \left\lfloor \frac{D_{CLK}}{\sqrt{\left(\frac{32 MHz}{2 MHz}\right)}} \right\rfloor = \left\lfloor \frac{5\%}{\sqrt{16}} \right\rfloor = \left\lfloor \frac{5\%}{4} \right\rfloor = 1.25\%$$

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## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![](_page_18_Figure_3.jpeg)

	N	<b>ILLIMETER</b>	S		
Dimension	Dimension Limits			MAX	
Contact Pitch	Contact Pitch E		0.65 BSC		
Optional Center Pad Width	W2			6.60	
Optional Center Pad Length	T2			6.60	
Contact Pad Spacing	C1		8.00		
Contact Pad Spacing	C2		8.00		
Contact Pad Width (X44)	X1			0.35	
Contact Pad Length (X44)	Y1			0.85	
Distance Between Pads	G	0.25			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B

# **Revision F (November 2012)**

Removed "Preliminary" from data sheet footer.

## **Revision G (March 2013)**

This revision includes the following global changes:

- changes "FLTx" pin function to "FLTx" on all occurrences
- adds Section 31.0 "High-Temperature Electrical Characteristics" for high-temperature (+150°C) data

This revision also includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-5.

Section Name	Update Description
Cover Section	<ul> <li>Changes internal oscillator specification to 1.0%</li> <li>Changes I/O sink/source values to 12 mA or 6 mA</li> <li>Corrects 44-pin VTLA pin diagram (pin 32 now shows as 5V tolerant)</li> </ul>
Section 4.0 "Memory Organization"	<ul> <li>Deletes references to Configuration Shadow registers</li> <li>Corrects the spelling of the JTAGIP and PTGWDTIP bits throughout</li> <li>Corrects the Reset value of all IOCON registers as C000h</li> <li>Adds footnote to Table 4-42 to indicate the absence of Comparator 3 in 28-pin devices</li> </ul>
Section 6.0 "Resets"	<ul> <li>Removes references to cold and warm Resets, and clarifies the initial configuration of the device clock source on all Resets</li> </ul>
Section 7.0 "Interrupt Controller"	Corrects the definition of GIE as "Global Interrupt Enable" (not "General")
Section 9.0 "Oscillator Configuration"	<ul> <li>Clarifies the behavior of the CF bit when cleared in software</li> <li>Removes POR behavior footnotes from all control registers</li> <li>Corrects the tuning range of the TUN&lt;5:0&gt; bits in Register 9-4 to an overall range ±1.5%</li> </ul>
Section 13.0 "Timer2/3 and Timer4/5"	Clarifies the presence of the ADC Trigger in 16-bit Timer3 and Timer5, as well as the 32-bit timers
Section 15.0 "Output Compare"	Corrects the first trigger source for SYNCSEL<4:0> (OCxCON2<4:0>) as OCxRS match
Section 16.0 "High-Speed PWM Module"	<ul> <li>Clarifies the source of the PWM interrupts in Figure 16-1</li> <li>Corrects the Reset states of IOCONx&lt;15:14&gt; in Register 16-13 as '11'</li> </ul>
Section 17.0 "Quadrature Encoder Interface (QEI) Module"	<ul> <li>Clarifies the operation of the IMV&lt;1:0&gt; bits (QEICON&lt;9:8&gt;) with updated text and additional notes</li> <li>Corrects the first prescaler value for QFVDIV&lt;2:0&gt; (QEI10C&lt;13:11&gt;), now 1:128</li> </ul>
Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)"	<ul> <li>Adds note to Figure 23-1 that Op Amp 3 is not available in 28-pin devices</li> <li>Changes "sample clock" to "sample trigger" in AD1CON1 (Register 23-1)</li> <li>Clarifies footnotes on op amp usage in Registers 23-5 and 23-6</li> </ul>
Section 25.0 "Op Amp/ Comparator Module"	<ul> <li>Adds Note text to indicate that Comparator 3 is unavailable in 28-pin devices</li> <li>Splits Figure 25-1 into two figures for clearer presentation (Figure 25-1 for Op amp/ Comparators 1 through 3, Figure 25-2 for Comparator 4). Subsequent figures are renumbered accordingly.</li> <li>Corrects reference description in xxxxx (now (AVDD+AVss)/2)</li> <li>Changes CMSTAT&lt;15&gt; in Register 25-1 to "PSIDL"</li> </ul>
Section 27.0 "Special Features"	Corrects the addresses of all Configuration bytes for 512 Kbyte devices

#### TABLE A-5: MAJOR SECTION UPDATES

Section Name	Update Description
Section 30.0 "Electrical Characteristics"	<ul> <li>Throughout: qualifies all footnotes relating to the operation of analog modules below VDDMIN (replaces "will have" with "may have")</li> </ul>
	<ul> <li>Throughout: changes all references of SPI timing parameter symbol "TscP" to "FscP"</li> <li>Table 30-1: changes VDD range to 3.0V to 3.6V</li> </ul>
	Table 30-4: removes Parameter DC12 (RAM Retention Voltage)
	<ul> <li>Table 30-7: updates Maximum values at 10 and 20 MIPS</li> </ul>
	<ul> <li>Table 30-8: adds Maximum IPD values, and removes all ∆IWDT entries</li> </ul>
	<ul> <li>Adds new Table 30-9 (Watchdog Timer Delta Current) with consolidated values removed from Table 30-8. All subsequent tables are renumbered accordingly.</li> </ul>
	Table 30-10: adds footnote for all parameters for 1:2 Doze ratio     Table 30-11:
	- changes Minimum and Maximum values for D120 and D130
	<ul> <li>adds Minimum and Maximum values for D131</li> </ul>
	<ul> <li>adds Minimum and Maximum values for D150 through D156, and removes Typical values</li> </ul>
	• Table 30-12:
	- reformats table for readability
	- changes IOL conditions for DO10
	Iable 30-14: adds footnote to D135     Table 30-17: abangaa Minimum and Maximum values for OS20
	Table 30-17: changes minimum and maximum values for OS30     Table 30-19:
	- splits temperature range and adds new values for E20a
	<ul> <li>reduces temperature range for F20b to extended temperatures only</li> </ul>
	• Table 30-20:
	<ul> <li>splits temperature range and adds new values for F21a</li> </ul>
	- reduces temperature range for F20b to extended temperatures only
	Table 30-53:
	- adds footpote ("Parameter characterized") to multiple parameters
	<ul> <li>Table 30-55: adds Minimum and Maximum values for all CTMUI specifications, and removes Typical values</li> </ul>
	<ul> <li>Table 30-57: adds new footnote to AD09</li> <li>Table 30-58:</li> </ul>
	<ul> <li>removes all specifications for accuracy with external voltage references</li> <li>removes Typical values for AD23a and AD24a</li> </ul>
	<ul> <li>replaces Minimum and Maximum values for AD21a, AD22a, AD23a and AD24a with new values, split by Industrial and Extended temperatures</li> </ul>
	- removes Maximum value of AD30
	- removes Minimum values from AD31a and AD32a
	- adds of changes Typical values for AD30, AD31a, AD32a and AD33a
	- removes all specifications for accuracy with external voltage references
	<ul> <li>removes Maximum value of AD30</li> </ul>
	<ul> <li>removes Typical values for AD23b and AD24b</li> </ul>
	- replaces Minimum and Maximum values for AD21b, AD22b, AD23b and AD24b
	with new values, split by Industrial and Extended temperatures
	<ul> <li>removes withintum and waximum values from AD310, AD320, AD330 and AD340</li> <li>adds or changes Typical values for AD30, AD31a, AD32a and AD33a</li> </ul>
	Table 30-61: Adds footnote to AD51
Section 32.0 "DC and AC	Updates Figure 32-6 (Typical IDD @ 3.3V) with individual current vs. processor speed
Device Characteristics	curves for the different program memory sizes
Graphs"	
Section 33.0 "Packaging	Replaces drawing C04-149C (64-pin QFN, 7.15 x 7.15 exposed pad) with C04-154A
Information"	(64-pin QFN, 5.4 x 5.4 exposed pad)

## TABLE A-5: MAJOR SECTION UPDATES (CONTINUED)