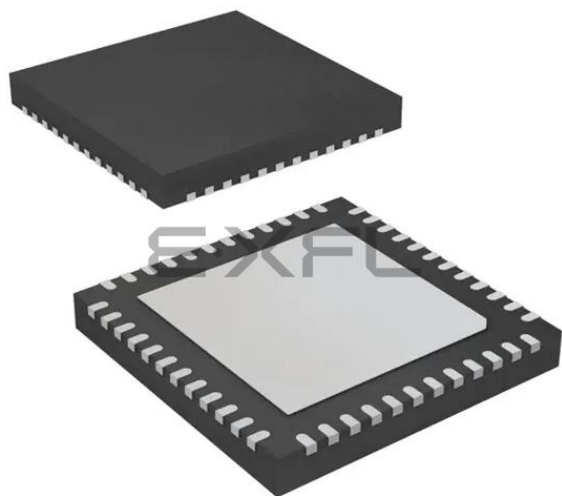




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Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64mc204-e-mv

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

- bit 2 **SFA:** Stack Frame Active Status bit
1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space
- bit 1 **RND:** Rounding Mode Select bit⁽¹⁾
1 = Biased (conventional) rounding is enabled
0 = Unbiased (convergent) rounding is enabled
- bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit⁽¹⁾
1 = Integer mode is enabled for DSP multiply
0 = Fractional mode is enabled for DSP multiply

- Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
2: This bit is always read as '0'.
3: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

4.4 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXMC20X/50X AND dsPIC33EPXXG50X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
W0	0000	W0 (WREG)																xxxx	
W1	0002	W1																xxxx	
W2	0004	W2																xxxx	
W3	0006	W3																xxxx	
W4	0008	W4																xxxx	
W5	000A	W5																xxxx	
W6	000C	W6																xxxx	
W7	000E	W7																xxxx	
W8	0010	W8																xxxx	
W9	0012	W9																xxxx	
W10	0014	W10																xxxx	
W11	0016	W11																xxxx	
W12	0018	W12																xxxx	
W13	001A	W13																xxxx	
W14	001C	W14																xxxx	
W15	001E	W15																xxxx	
SPLIM	0020	SPLIM																0000	
ACCAL	0022	ACCAL																0000	
ACCAH	0024	ACCAH																0000	
ACCAU	0026	Sign Extension of ACCA<39>									ACCAU							0000	
ACCBL	0028	ACCBL																0000	
ACCBH	002A	ACCBH																0000	
ACCBU	002C	Sign Extension of ACCB<39>									ACCBU							0000	
PCL	002E	PCL<15:0>																—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH<6:0>							0000	
DSRPAG	0032	—	—	—	—	—	—	DSRPAG<9:0>										0001	
DSWPAG	0034	—	—	—	—	—	—	—	DSWPAG<8:0>										0001
RCOUNT	0036	RCOUNT<15:0>																0000	
DCOUNT	0038	DCOUNT<15:0>																0000	
DOSTARTL	003A	DOSTARTL<15:1>																—	0000
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>						0000	
DOENDL	003E	DOENDL<15:1>																—	0000
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH<5:0>						0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-2: CPU CORE REGISTER MAP FOR PIC24EPXXXGP/MC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
W0	0000	W0 (WREG)																XXXX	
W1	0002	W1																XXXX	
W2	0004	W2																XXXX	
W3	0006	W3																XXXX	
W4	0008	W4																XXXX	
W5	000A	W5																XXXX	
W6	000C	W6																XXXX	
W7	000E	W7																XXXX	
W8	0010	W8																XXXX	
W9	0012	W9																XXXX	
W10	0014	W10																XXXX	
W11	0016	W11																XXXX	
W12	0018	W12																XXXX	
W13	001A	W13																XXXX	
W14	001C	W14																XXXX	
W15	001E	W15																XXXX	
SPLIM	0020	SPLIM<15:0>																0000	
PCL	002E	PCL<15:1>																—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	PCH<6:0>							0000	
DSRPAG	0032	—	—	—	—	—	—	DSRPAG<9:0>										0001	
DSWPAG	0034	—	—	—	—	—	—	—	DSWPAG<8:0>										0001
RCOUNT	0036	RCOUNT<15:0>																0000	
SR	0042	—	—	—	—	—	—	—	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000	
CORCON	0044	VAR	—	—	—	—	—	—	—	—	—	—	—	IPL3	SFA	—	—	0020	
DISICNT	0052	—	—	DISICNT<13:0>														0000	
TBLPAG	0054	—	—	—	—	—	—	—	—	TBLPAG<7:0>									0000
MSTRPR	0058	MSTRPR<15:0>																0000	

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC23	086E	—	PWM2IP<2:0>			—	PWM1IP<2:0>			—	—	—	—	—	—	—	—	4400
IPC24	0870	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IP<2:0>			0004
IPC35	0886	—	JTAGIP<2:0>			—	ICDIP<2:0>			—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP<2:0>			—	PTGWDTIP<2:0>			—	PTGSTEPIP<2:0>			—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP<2:0>			—	PTG2IP<2:0>			—	PTG1IP<2:0>			0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVATE	OVATE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFail	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
INTTREG	08C8	—	—	—	—	ILR<3:0>				VECNUM<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-33: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		
RPINR0	06A0	—	INT1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>								0000	
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>								0000	
RPINR7	06AE	—	IC2R<6:0>								—	IC1R<6:0>								0000
RPINR8	06B0	—	IC4R<6:0>								—	IC3R<6:0>								0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>								0000	
RPINR12	06B8	—	FLT2R<6:0>								—	FLT1R<6:0>								0000
RPINR14	06BC	—	QEB1R<6:0>								—	QEA1R<6:0>								0000
RPINR15	06BE	—	HOME1R<6:0>								—	INDX1R<6:0>								0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>								0000	
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>								0000	
RPINR22	06CC	—	SCK2INR<6:0>								—	SDI2R<6:0>								0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>								0000	
RPINR37	06EA	—	SYNC1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR38	06EC	—	DTCMP1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR39	06EE	—	DTCMP3R<6:0>								—	DTCMP2R<6:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 3	SLEEP: Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode
bit 2	IDLE: Wake-up from Idle Flag bit 1 = Device was in Idle mode 0 = Device was not in Idle mode
bit 1	BOR: Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

- Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 4	Unimplemented: Read as '0'
bit 3	CF: Clock Fail Detect bit ⁽³⁾ 1 = FSCM has detected clock failure 0 = FSCM has not detected clock failure
bit 2-1	Unimplemented: Read as '0'
bit 0	OSWEN: Oscillator Switch Enable bit 1 = Requests oscillator switch to selection specified by the NOSC<2:0> bits 0 = Oscillator switch is complete

- Note 1:** Writes to this register require an unlock sequence. Refer to “**Oscillator**” (DS70580) in the “*dsPIC33/PIC24 Family Reference Manual*” (available from the Microchip web site) for details.
- 2:** Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.
- 3:** This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

NOTES:

REGISTER 16-14: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **TRGCMP<15:0>**: Trigger Control Value bits

When the primary PWMx functions in local time base, this register contains the compare values that can trigger the ADC module.

REGISTER 16-18: AUXCONx: PWMx AUXILIARY CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0
bit 15				bit 8			

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLLEN
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'bit 11-8 **BLANKSEL<3:0>:** PWMx State Blank Source Select bits

The selected state blank signal will block the current-limit and/or Fault input signals (if enabled via the BCH and BCL bits in the LEBCONx register).

1001 = Reserved

•
•
•

0100 = Reserved

0011 = PWM3H selected as state blank source

0010 = PWM2H selected as state blank source

0001 = PWM1H selected as state blank source

0000 = No state blanking

bit 7-6 **Unimplemented:** Read as '0'bit 5-2 **CHOPSEL<3:0>:** PWMx Chop Clock Source Select bits

The selected signal will enable and disable (CHOP) the selected PWMx outputs.

1001 = Reserved

•
•
•

0100 = Reserved

0011 = PWM3H selected as CHOP clock source

0010 = PWM2H selected as CHOP clock source

0001 = PWM1H selected as CHOP clock source

0000 = Chop clock generator selected as CHOP clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit

1 = PWMxH chopping function is enabled

0 = PWMxH chopping function is disabled

bit 0 **CHOPLLEN:** PWMxL Output Chopping Enable bit

1 = PWMxL chopping function is enabled

0 = PWMxL chopping function is disabled

REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	—	CH0SB4 ⁽¹⁾	CH0SB3 ⁽¹⁾	CH0SB2 ⁽¹⁾	CH0SB1 ⁽¹⁾	CH0SB0 ⁽¹⁾
bit 15							bit 8

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	—	CH0SA4 ⁽¹⁾	CH0SA3 ⁽¹⁾	CH0SA2 ⁽¹⁾	CH0SA1 ⁽¹⁾	CH0SA0 ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample MUXB bit
 1 = Channel 0 negative input is AN1⁽¹⁾
 0 = Channel 0 negative input is VREFL
- bit 14-13 **Unimplemented:** Read as '0'
- bit 12-8 **CH0SB<4:0>:** Channel 0 Positive Input Select for Sample MUXB bits⁽¹⁾
 11111 = Open; use this selection with CTMU capacitive and time measurement
 11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
 11101 = Reserved
 11100 = Reserved
 11011 = Reserved
 11010 = Channel 0 positive input is the output of OA3/AN6^(2,3)
 11001 = Channel 0 positive input is the output of OA2/AN0⁽²⁾
 11000 = Channel 0 positive input is the output of OA1/AN3⁽²⁾
 10111 = Reserved
 .
 .
 .
 10000 = Reserved
 01111 = Channel 0 positive input is AN15⁽³⁾
 01110 = Channel 0 positive input is AN14⁽³⁾
 01101 = Channel 0 positive input is AN13⁽³⁾
 .
 .
 .
 00010 = Channel 0 positive input is AN2⁽³⁾
 00001 = Channel 0 positive input is AN1⁽³⁾
 00000 = Channel 0 positive input is AN0⁽³⁾
- bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample MUXA bit
 1 = Channel 0 negative input is AN1⁽¹⁾
 0 = Channel 0 negative input is VREFL
- bit 6-5 **Unimplemented:** Read as '0'

- Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
- 2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON<10>) = 1); otherwise, the ANx input is used.
- 3:** See the “Pin Diagrams” section for the available analog channels for each device.

REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCTS4	ADCTS3	ADCTS2	ADCTS1	IC4TSS	IC3TSS	IC2TSS	IC1TSS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC4CS	OC3CS	OC2CS	OC1CS	OC4TSS	OC3TSS	OC2TSS	OC1TSS
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **ADCTS4:** Sample Trigger PTGO15 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed
- bit 14 **ADCTS3:** Sample Trigger PTGO14 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed
- bit 13 **ADCTS2:** Sample Trigger PTGO13 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed
- bit 12 **ADCTS1:** Sample Trigger PTGO12 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed
- bit 11 **IC4TSS:** Trigger/Synchronization Source for IC4 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed
- bit 10 **IC3TSS:** Trigger/Synchronization Source for IC3 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed
- bit 9 **IC2TSS:** Trigger/Synchronization Source for IC2 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed
- bit 8 **IC1TSS:** Trigger/Synchronization Source for IC1 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed
- bit 7 **OC4CS:** Clock Source for OC4 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed
- bit 6 **OC3CS:** Clock Source for OC3 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed
- bit 5 **OC2CS:** Clock Source for OC2 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: This register is only used with the PTGCTRL OPTION = 1111 Step command.

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3)

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CON	COE ⁽²⁾	CPOL	—	—	OPMODE	CEVT	COUT
bit 15						bit 8	

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1	EVPOL0	—	CREF ⁽¹⁾	—	—	CCH1 ⁽¹⁾	CCH0 ⁽¹⁾
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CON:** Op Amp/Comparator Enable bit
1 = Op amp/comparator is enabled
0 = Op amp/comparator is disabled
- bit 14 **COE:** Comparator Output Enable bit⁽²⁾
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only
- bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted
- bit 12-11 **Unimplemented:** Read as '0'
- bit 10 **OPMODE:** Op Amp/Comparator Operation Mode Select bit
1 = Circuit operates as an op amp
0 = Circuit operates as a comparator
- bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to the EVPOL<1:0> settings occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur
- bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1 (inverted polarity):
1 = VIN+ < VIN-
0 = VIN+ > VIN-

Note 1: Inputs that are selected and not available will be tied to Vss. See the “Pin Diagrams” section for available inputs for each package.

2: This output is not available when OPMODE (CMxCON<10>) = 1.

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions $\in \{W4 * W4, W5 * W5, W6 * W6, W7 * W7\}$
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions $\in \{W4 * W5, W4 * W6, W4 * W7, W5 * W6, W5 * W7, W6 * W7\}$
Wn	One of 16 working registers $\in \{W0...W15\}$
Wnd	One of 16 destination working registers $\in \{W0...W15\}$
Wns	One of 16 source working registers $\in \{W0...W15\}$
WREG	W0 (working register used in file register instructions)
Ws	Source W register $\in \{Ws, [Ws], [Ws++] , [Ws--], [++Ws], [--Ws] \}$
Wso	Source W register $\in \{Wns, [Wns], [Wns++] , [Wns--], [++Wns], [--Wns], [Wns+Wb] \}$
Wx	X Data Space Prefetch Address register for DSP instructions $\in \{[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], \text{none}\}$
Wxd	X Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$
Wy	Y Data Space Prefetch Address register for DSP instructions $\in \{[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], \text{none}\}$
Wyd	Y Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$

FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS

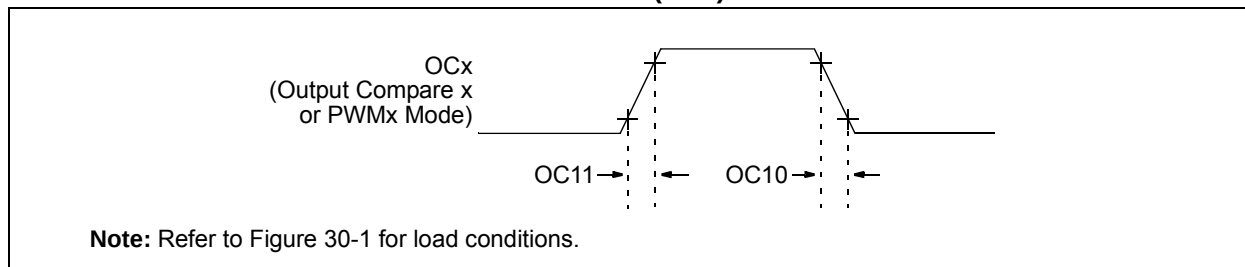


TABLE 30-27: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS

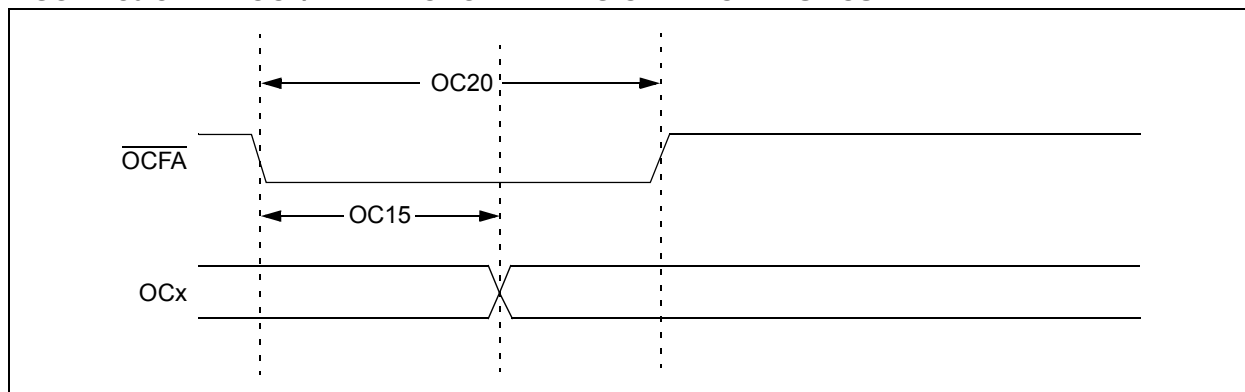


TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC15	TFD	Fault Input to PWMx I/O Change	—	—	$T_{CY} + 20$	ns	
OC20	TFLT	Fault Input Pulse Width	$T_{CY} + 20$	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-33: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	CKP	SMP
15 MHz	Table 30-33	—	—	0,1	0,1	0,1
9 MHz	—	Table 30-34	—	1	0,1	1
9 MHz	—	Table 30-35	—	0	0,1	1
15 MHz	—	—	Table 30-36	1	0	0
11 MHz	—	—	Table 30-37	1	1	0
15 MHz	—	—	Table 30-38	0	1	0
11 MHz	—	—	Table 30-39	0	0	0

FIGURE 30-14: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKP = 0)
TIMING CHARACTERISTICS

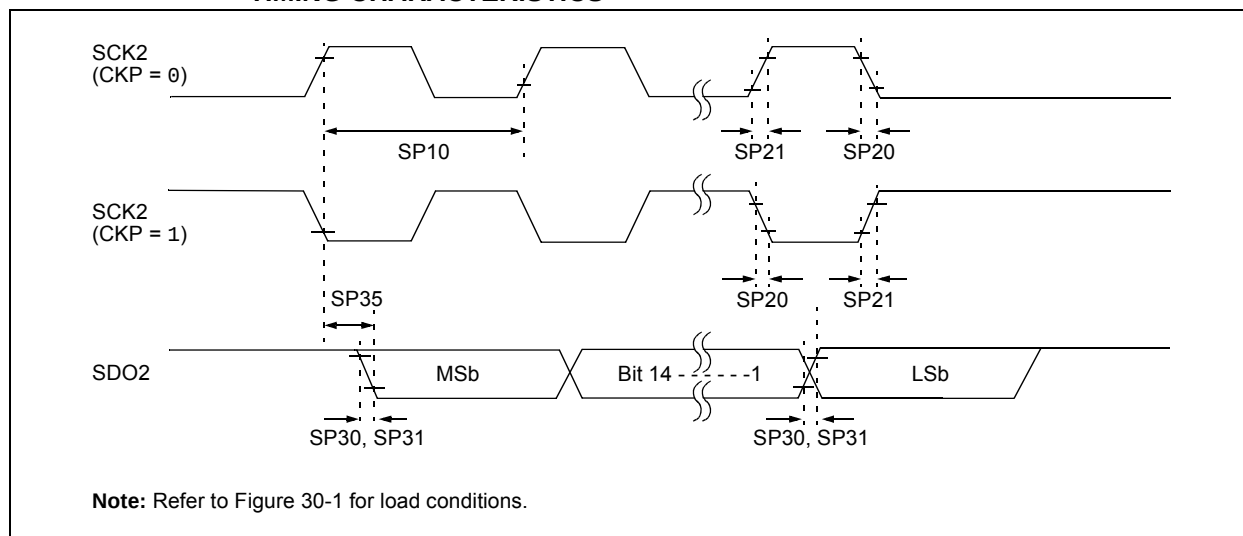
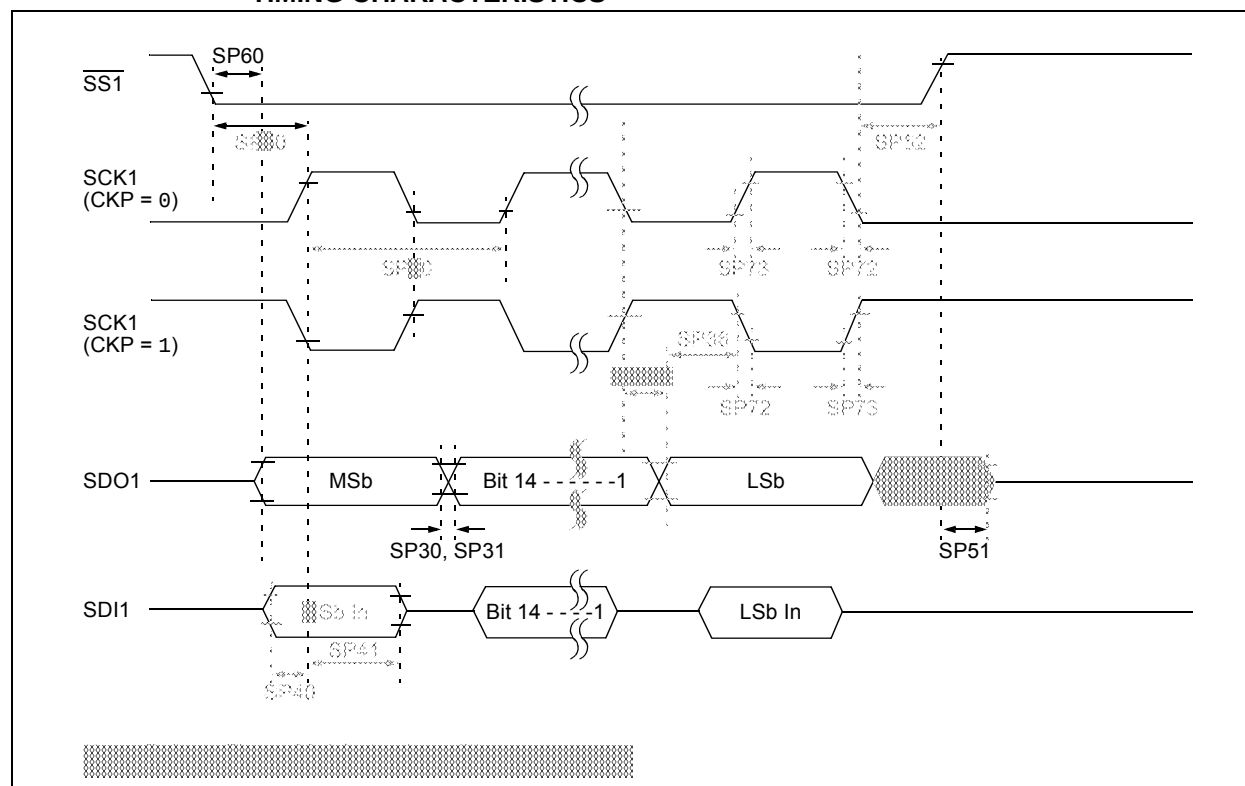


FIGURE 30-26: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)
TIMING CHARACTERISTICS



31.1 High-Temperature DC Characteristics

TABLE 31-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Max MIPS
			dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X
HDC5	3.0 to 3.6V ⁽¹⁾	-40°C to +150°C	40

Note 1: Device is functional at $V_{BORMIN} < V_{DD} < V_{DDMIN}$. Analog modules, such as the ADC, may have degraded performance. Device functionality is tested but not characterized.

TABLE 31-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
High-Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+155	°C
Operating Ambient Temperature Range	TA	-40	—	+150	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \sum I_{OH})$ I/O Pin Power Dissipation: $I/O = \sum (\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum (V_{OL} \times I_{OL})$	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	$(T_J - T_A)/\theta_{JA}$			W

TABLE 31-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^\circ\text{C} \leq T_A \leq +150^\circ\text{C}$				
Parameter No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Operating Voltage							
HDC10	Supply Voltage						
	VDD	—	3.0	3.3	3.6	V	-40°C to +150°C

TABLE 31-12: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (12-Bit Mode) ⁽¹⁾							
HAD20a	Nr	Resolution ⁽³⁾	12 Data Bits			bits	
HAD21a	INL	Integral Nonlinearity	-5.5	—	5.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD23a	GERR	Gain Error	-10	—	10	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD24a	EOFF	Offset Error	-5	—	5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
Dynamic Performance (12-Bit Mode) ⁽²⁾							
HAD33a	FNYQ	Input Signal Bandwidth	—	—	200	kHz	

Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

TABLE 31-13: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
ADC Accuracy (10-Bit Mode) ⁽¹⁾							
HAD20b	Nr	Resolution ⁽³⁾	10 Data Bits			bits	
HAD21b	INL	Integral Nonlinearity	-1.5	—	1.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD23b	GERR	Gain Error	-2.5	—	2.5	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
HAD24b	EOFF	Offset Error	-1.25	—	1.25	LSb	V _{INL} = AV _{SS} = V _{REFL} = 0V, AV _{DD} = V _{REFH} = 3.6V
Dynamic Performance (10-Bit Mode) ⁽²⁾							
HAD33b	FNYQ	Input Signal Bandwidth	—	—	400	kHz	

Note 1: These parameters are characterized, but are tested at 20 ksp/s only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents $> |0|$ can affect the ADC results by approximately 4-6 counts.

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