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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24ep64mc204-i-mv

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TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES (CONTINUED)

s)		s)	-	Remappable Peripherals												1					
Device	Page Erase Size (Instructions)	Program Flash Memory (Kbyte	RAM (Kbytes)	16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM ⁽⁴⁾ (Channels)	Quadrature Encoder Interface	UART	SPI ⁽²⁾	ECAN™ Technology	External Interrupts ⁽³⁾	I ² C TM	CRC Generator	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	I/O Pins	Pins	Packages
dsPIC33EP32MC504	512	32	4																		
dsPIC33EP64MC504	1024	64	8																		VTLA ⁽⁵⁾ ,
dsPIC33EP128MC504	1024	128	16	5	4	4	6	1	2	2	1	3	2	1	9	3/4	Yes	Yes	35	44/ 48	TQFP, OEN
dsPIC33EP256MC504	1024	256	32																	40	UQFN
dsPIC33EP512MC504	1024	512	48																		
dsPIC33EP64MC506	1024	64	8																		
dsPIC33EP128MC506	1024	128	16	5	4	4	6	1	2	2	1	2	2	1	16	2/4	Vaa	Voo	52	64	TQFP,
dsPIC33EP256MC506	1024	256	32	э	4	4	0	1	2	2	1	3	2		10	3/4	res	res	53	04	QFN
dsPIC33EP512MC506	1024	512	48																		

 Note 1:
 On 28-pin devices, Comparator 4 does not have external connections. Refer to Section 25.0 "Op Amp/Comparator Module" for details.

 2:
 Only SPI2 is remappable.

3: INT0 is not remappable.

4: Only the PWM Faults are remappable.

5: The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.



FIGURE 4-9: DATA MEMORY MAP FOR dsPIC33EP128MC20X/50X AND dsPIC33EP128GP50X DEVICES

TABLE 4	-1:	CPU C	ORE RE	GISTE	R MAP F	OR dsF	PIC33EP	XXXMC	20X/50X	AND d	sPIC33I	EPXXX	GP50X	DEVICE	S ONL	(CON	TINUE	D)
File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	С	0000
CORCON	0044	VAR	_	US<	1:0>	EDT		DL<2:0>		SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020
MODCON	0046	XMODEN	DEN YMODEN — — BWM<3:0> XWM<3:0>											0000				
XMODSRT	0048		XMODSRT<15:0>000											0000				
XMODEND	004A		XMODEND<15:0> —											0001				
YMODSRT	004C							YMC	DSRT<15:0	>								0000
YMODEND	004E							YMC	DEND<15:0)>								0001
XBREV	0050	BREN							XBF	REV<14:0>								0000
DISICNT	0052	_	_							DISICNT<	13:0>							0000
TBLPAG	0054		TBLPAG<7:0> 0000											0000				
MSTRPR	0058		MSTRPR<15:0> 0000												0000			

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY (CONTINUED)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC35	0886	—		JTAGIP<2:0)>	—		ICDIP<2:0	>	—	_	—	—	_	_	—	-	4400
IPC36	0888	_		PTG0IP<2:0)>	_	PT	GWDTIP<	2:0>	_	PT	GSTEPIP<2	::0>	_	_	_	_	4440
IPC37	088A	_	_	_	_	_	F	PTG3IP<2:	0>	_		PTG2IP<2:0	>	_	I	PTG1IP<2:0>		0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	_	_	_	_	_	_	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	_	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	_	—	_	—	—	_	INT2EP	INT1EP	INT0EP	8000
INTCON3	08C4	—	—	—	_	_	_	—	_	—	_	DAE	DOOVR	—	—	—		0000
INTCON4	08C6	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	SGHT	0000
INTTREG	08C8	_	_	_	_		ILR<	3:0>					VECN	IUM<7:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

	Vector	IRQ		Inte	errupt Bit L	ocation			
Interrupt Source	#	#	IVI Address	Flag	Enable	Priority			
QEI1 – QEI1 Position Counter Compare ⁽²⁾	66	58	0x000088	IFS3<10>	IEC3<10>	IPC14<10:8>			
Reserved	67-72	59-64	0x00008A-0x000094	_	_	—			
U1E – UART1 Error Interrupt	73	65	0x000096	IFS4<1>	IEC4<1>	IPC16<6:4>			
U2E – UART2 Error Interrupt	74	66	0x000098	IFS4<2>	IEC4<2>	IPC16<10:8>			
CRC – CRC Generator Interrupt	75	67	0x00009A	IFS4<3>	IEC4<3>	IPC16<14:12>			
Reserved	76-77	68-69	0x00009C-0x00009E	_	_	—			
C1TX – CAN1 TX Data Request ⁽¹⁾	78	70	0x000A0	IFS4<6>	IEC4<6>	IPC17<10:8>			
Reserved	79-84	71-76	0x0000A2-0x0000AC	_	_	—			
CTMU – CTMU Interrupt	85	77	0x0000AE	IFS4<13>	IEC4<13>	IPC19<6:4>			
Reserved	86-101	78-93	0x0000B0-0x0000CE	_	_	—			
PWM1 – PWM Generator 1 ⁽²⁾	102	94	0x0000D0	IFS5<14>	IEC5<14>	IPC23<10:8>			
PWM2 – PWM Generator 2 ⁽²⁾	103	95	0x0000D2	IFS5<15>	IEC5<15>	IPC23<14:12>			
PWM3 – PWM Generator 3 ⁽²⁾	104	96	0x0000D4	IFS6<0>	IEC6<0>	IPC24<2:0>			
Reserved	105-149	97-141	0x0001D6-0x00012E	—	—	—			
ICD – ICD Application	150	142	0x000142	IFS8<14>	IEC8<14>	IPC35<10:8>			
JTAG – JTAG Programming	151	143	0x000130	IFS8<15>	IEC8<15>	IPC35<14:12>			
Reserved	152	144	0x000134	—	—	—			
PTGSTEP – PTG Step	153	145	0x000136	IFS9<1>	IEC9<1>	IPC36<6:4>			
PTGWDT – PTG Watchdog Time-out	154	146	0x000138	IFS9<2>	IEC9<2>	IPC36<10:8>			
PTG0 – PTG Interrupt 0	155	147	0x00013A	IFS9<3>	IEC9<3>	IPC36<14:12>			
PTG1 – PTG Interrupt 1	156	148	0x00013C	IFS9<4>	IEC9<4>	IPC37<2:0>			
PTG2 – PTG Interrupt 2	157	149	0x00013E	IFS9<5>	IEC9<5>	IPC37<6:4>			
PTG3 – PTG Interrupt 3	158	150	0x000140	IFS9<6>	IEC9<6>	IPC37<10:8>			
Reserved	159-245	151-245	0x000142-0x0001FE	_	_	_			
Lowest Natural Order Priority									

TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Note 1: This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

2: This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode

- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU interrupt after half or full block transfer complete
- Byte or word transfers
- · Fixed priority channel arbitration
- Manual (software) or automatic (peripheral DMA requests) transfer initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer is complete)
- DMA request for each channel can be selected from any supported interrupt source
- Debug support features

The peripherals that can utilize DMA are listed in Table 8-1.

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	00000000	—	—
IC1 – Input Capture 1	0000001	0x0144 (IC1BUF)	—
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	_
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—
OC1 – Output Compare 1	00000010	_	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	_	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	_	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	_	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	—	—
TMR3 – Timer3	00001000	-	—
TMR4 – Timer4	00011011	_	—
TMR5 – Timer5	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)
ECAN1 – RX Data Ready	00100010	0x0440 (C1RXD)	
ECAN1 – TX Data Request	01000110	—	0x0442 (C1TXD)
ADC1 – ADC1 Convert Done	00001101	0x0300 (ADC1BUF0)	_

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0					
CHEN	SIZE	DIR	HALF	NULLW	_	—	—					
bit 15							bit 8					
U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0					
		AMODE1	AMODE0			MODE1	MODE0					
bit 7							bit 0					
Legend:			,			(0)						
R = Readable	bit	W = Writable	bit		mented bit, read	as '0'						
-n = Value at F	POR	'1' = Bit is set		0^{\prime} = Bit is cle	eared	x = Bit is unkn	IOWN					
bit 15		Channel Enabl	o hit									
bit 15	1 = Channel	is enabled										
	0 = Channel	is disabled										
bit 14	SIZE: DMA D	ata Transfer Si	ze bit									
	1 = Byte											
	0 = Word											
bit 13 DIR: DMA Transfer Direction bit (source/destination bus select)												
	1 = Reads from 0 = Reads from 1	om RAM addre	ddress. writes to p	s to RAM addr	ess ess							
bit 12	HALF: DMA	Block Transfer	Interrupt Sele	ct bit								
	1 = Initiates i	nterrupt when I	nalf of the dat	a has been mo	oved							
	0 = Initiates i	nterrupt when a	all of the data	has been mov	ved							
bit 11	NULLW: Null	Data Periphera	al Write Mode	Select bit								
	1 = Null data	write to periph	eral in additio	n to RAM write	e (DIR bit must a	also be clear)						
bit 10-6	Unimplemen	ted: Read as '	ר'									
bit 5-4	AMODE<1:0	: DMA Channe	el Addressina	Mode Select	bits							
	11 = Reserve	ed										
	10 = Peripher	ral Indirect Add	ressing mode									
	01 = Register	Indirect withou	ut Post-Increm	nent mode								
hit 3 2		tod: Pood as '	ost-incremen	tmode								
bit 1_0		DMA Channel	Operating Mc	nda Salact hits								
bit 1-0	11 = One-Sh	ot. Pina-Pona r	nodes are en	abled (one blo	ck transfer from	/to each DMA b	ouffer)					
	10 = Continue	ous, Ping-Pong	modes are e	nabled								
	01 = One-Sho	ot, Ping-Pong r	nodes are dis	abled								
		ous, Ping-Pong	modes are d	ISADIEO								

REGISTER 8-1: DMAXCON: DMA CHANNEL X CONTROL REGISTER

REGISTER 8-7: DMAXPAD: DMA CHANNEL X PERIPHERAL ADDRESS REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PAD	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PAD)<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 PAD<15:0>: Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-8: DMAXCNT: DMA CHANNEL X TRANSFER COUNT REGISTER⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	_			CNT<	13:8> (2)		
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CNT≪	<7:0> (2)			
bit 7							bit 0
Legend:							
R = Readable b	oit	W = Writable b	oit	U = Unimpler	nented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-14 Unimplemented: Read as '0'

bit 13-0 CNT<13:0>: DMA Transfer Count Register bits⁽²⁾

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: The number of DMA transfers = CNT<13:0> + 1.

12.2 Timer1 Control Register

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0						
TON ⁽¹⁾	—	TSIDL	—	_	—	—	—						
bit 15							bit 8						
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0						
	TGATE	TCKPS1	TCKPS0	_	TSYNC ⁽¹⁾	TCS ⁽¹⁾	—						
bit 7							bit 0						
Legend:													
R = Readab	ole bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'							
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own						
		(1)											
bit 15	TON: Timer1	On bit ⁽¹⁾											
	1 = Starts 16-	bit Limer1 bit Timer1											
bit 1/	Unimplement	ted: Pead as '	ı'										
bit 13		1 Stop in Idle N	/ode hit										
DIC 15	1 = Discontinues module operation when device enters Idle mode												
	 Discontinues module operation when device enters rale mode Continues module operation in Idle mode 												
bit 12-7	Unimplement	Unimplemented: Read as '0'											
bit 6	TGATE: Time	TGATE: Timer1 Gated Time Accumulation Enable bit											
	When TCS =	<u>1:</u> prod											
	When TCS =	0. 0.											
	1 = Gated tim	<u>e</u> accumulatior	n is enabled										
	0 = Gated tim	e accumulatior	n is disabled										
bit 5-4	TCKPS<1:0>	: Timer1 Input	Clock Prescal	e Select bits									
	11 = 1:256												
	10 = 1:64 01 = 1:8												
	01 = 1.0 00 = 1.1												
bit 3	Unimplement	ted: Read as ')'										
bit 2	TSYNC: Time	er1 External Clo	ock Input Sync	chronization Se	elect bit ⁽¹⁾								
	When TCS =	1:											
	1 = Synchroni	izes external cl	ock input										
	0 = Does not	synchronize ex	ternal clock in	nput									
	This bit is jand	<u>ored</u> .											
bit 1	TCS: Timer1 (Clock Source S	Select bit ⁽¹⁾										
	1 = External c	lock is from pir	n, T1CK (on th	ne rising edge)									
	0 = Internal cl	ock (FP)		5 5-7									
bit 0	Unimplement	ted: Read as ')'										
Note 1: \	When Timer1 is en attempts by user so	abled in Exterr oftware to write	al Synchrono to the TMR1	us Counter mo register are ig	ode (TCS = 1, T nored.	SYNC = 1, TO	N = 1), any						

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

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15.0 OUTPUT COMPARE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See "Output Compare" (DS70358) in the "dsPIC33/PIC24 Family Reference Manual" for OCxR and OCxRS register restrictions.





dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	_			DTR)	<13:8>		
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			DTR	2x<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

REGISTER 16-10: DTRx: PWMx DEAD-TIME REGISTER

bit 15-14 Unimplemented: Read as '0'

bit 13-0 DTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 16-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			ALTDT	Rx<13:8>		
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			ALTDT	Rx<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	d as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-14 Unimplemented: Read as '0'

bit 13-0 ALTDTRx<13:0>: Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	EC<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	EC<23:16>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'			
-n = Value at POR		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	

REGISTER 17-15: QEI1GECH: QEI1 GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER

bit 15-0 QEIGEC<31:16>: High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

REGISTER 17-16: QEI1GECL: QEI1 GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIGE	C<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			QEIG	EC<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bi		bit	U = Unimplei	mented bit, rea	id as '0'		
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown

bit 15-0 QEIGEC<15:0>: Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

18.1 SPI Helpful Tips

- 1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on SSx.
 - b) If FRMPOL = 0, use a pull-up resistor on $\frac{1}{SSx}$.

Note:	This	insures	that	the	first	fra	ame
	transn	nission	after	initializ	ation	is	not
	shifted	d or corru	upted.				

- 2. In Non-Framed 3-Wire mode, (i.e., not using SSx from a master):
 - a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on SSx.
 - b) If CKP = 0, always place a pull-down resistor on SSx.
 - **Note:** This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data.
- FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the SSx pin, which indicates the start of a data frame.
 - Note: Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in Section 30.0 "Electrical Characteristics" for details.
- In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the
	product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en555464

18.2.1 KEY RESOURCES

- "Serial Peripheral Interface (SPI)" (DS70569) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 18-2: SPIXCON1: SPIX CONTROL REGISTER 1 (CONTINUED)

- SPRE<2:0>: Secondary Prescale bits (Master mode)⁽³⁾ bit 4-2 111 = Secondary prescale 1:1 110 = Secondary prescale 2:1 000 = Secondary prescale 8:1 bit 1-0 PPRE<1:0>: Primary Prescale bits (Master mode)⁽³⁾ 11 = Primary prescale 1:1
 - 10 = Primary prescale 4:1
 - 01 = Primary prescale 16:1
 - 00 = Primary prescale 64:1
- Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
 - 2: This bit must be cleared when FRMEN = 1.
 - 3: Do not set both primary and secondary prescalers to the value of 1:1.

21.4 ECAN Control Registers

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
		CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0
bit 15				·			bit 8
R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE2	OPMODE1	OPMODE0		CANCAP	—	—	WIN
bit 7							bit 0
		'1' = Bit is set	JIL	$0^{\circ} = \text{Bit is closed}$	ared	v = Bitis unkr	
	UK	I - DILIS SEL			aleu		IOWIT
bit 15-14	Unimplemen	ted: Read as '()'				
bit 13	CSIDL: ECAN	Nx Stop in Idle I	Mode bit				
	1 = Discontin	ues module ope	eration when	device enters I	dle mode		
	0 = Continues	s module opera	tion in Idle m	ode			
bit 12	ABAT: Abort	All Pending Tra	nsmissions b	it			
	1 = Signals al	I transmit buffe	rs to abort tra when all tran	ansmission smissions are a	aborted		
bit 11		CANx Module C	lock (ECAN) S	Source Select b	bit		
2	1 = FCAN is e	qual to 2 * FP					
	0 = FCAN is e	qual to FP					
bit 10-8	REQOP<2:0>	Request Ope	ration Mode	bits			
	111 = Set Lis	ten All Messag	es mode				
	101 = Reserv	red					
	100 = Set Co	nfiguration mod	le				
	011 = Set Lis	ten Only mode					
	001 = Set Dis	able mode					
	000 = Set No	rmal Operation	mode				
bit 7-5	OPMODE<2:	0> : Operation N	/lode bits				
	111 = Module	e is in Listen All	Messages m	node			
	110 = Reserv 101 = Reserv	red red					
	100 = Module	e is in Configura	ation mode				
	011 = Module	e is in Listen Or	ly mode				
	010 = Module	e is in Loopback e is in Disable n	node				
	000 = Module	e is in Normal C	peration mod	de			
bit 4	Unimplemen	ted: Read as 'o)'				
bit 3	CANCAP: CAN Message Receive Timer Capture Event Enable bit						
	1 = Enables in 0 = Disables (nput capture ba CAN capture	ised on CAN	message recei	ve		
bit 2-1	Unimplemen	ted: Read as '()'				
bit 0	WIN: SFR Ma	ap Window Sele	ect bit				
	1 = Uses filter	r window					
	0 = Uses buff	er window					

NOTES:

24.3 PTG Control Registers

REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT ⁽²⁾	PTGSSEN ⁽³⁾	PTGIVIS
bit 15							bit 8
R/W-0	HS-0	U-0	U-0	U-0	U-0	R/V	V-0
PTGSTRT	PTGWDTO	_	_	_	_	PTGITM1 ⁽¹⁾	PTGITM0 ⁽¹⁾

h	it	7
υ	π.	1

Legend:	HS = Hardware Settable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15		PTGEN: Module Enable bit
		1 = PTG module is enabled
		0 = PTG module is disabled
bit 14		Unimplemented: Read as '0'
bit 13		PTGSIDL: PTG Stop in Idle Mode bit
		 1 = Discontinues module operation when device enters Idle mode 0 = Continues module operation in Idle mode
bit 12		PTGTOGL: PTG TRIG Output Toggle Mode bit
		 1 = Toggle state of the PTGOx for each execution of the PTGTRIG command 0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits
bit 11		Unimplemented: Read as '0'
bit 10		PTGSWT: PTG Software Trigger bit ⁽²⁾
		1 = Triggers the PTG module
		0 = No action (clearing this bit will have no effect)
bit 9		PTGSSEN: PTG Enable Single-Step bit ⁽³⁾
		1 = Enables Single-Step mode
		0 = Disables Single-Step mode
bit 8		PTGIVIS: PTG Counter/Timer Visibility Control bit
		1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)
		 Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers
bit 7		PTGSTRT: PTG Start Sequencer bit
		1 = Starts to sequentially execute commands (Continuous mode)0 = Stops executing commands
bit 6		PTGWDTO: PTG Watchdog Timer Time-out Status bit
		1 = PTG Watchdog Timer has timed out
		0 = PTG watchdog Timer has not timed out.
bit 5-2		Unimplemented: Read as '0'
Note	1: Th	nese bits apply to the PTGWHI and PTGWLO commands only.
	2: Th	is bit is only used with the PTGCTRL step command software trigger option.

3: Use of the PTG Single-Step mode is reserved for debugging tools only.

bit 0

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/ MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss ⁽³⁾	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 3.0V^{(3)}$	0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $VDD < 3.0V^{(3)}$	-0.3V to +3.6V
Maximum current out of Vss pin	
Maximum current into VDD pin ⁽²⁾	
Maximum current sunk/sourced by any 4x I/O pin	
Maximum current sunk/sourced by any 8x I/O pin	25 mA
Maximum current sunk by all ports ^(2,4)	200 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).
 - 3: See the "Pin Diagrams" section for the 5V tolerant pins.
 - 4: Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

TABLE 30-48:SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS

АС СНА	AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions	
SP70	FscP	Maximum SCK1 Input Frequency		_	11	MHz	(Note 3)	
SP72	TscF	SCK1 Input Fall Time	_		—	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDO1 Data Output Fall Time			_	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDO1 Data Output Rise Time	—	_	_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	30	_	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	30	_	_	ns		
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	Ι	—	ns		
SP51	TssH2doZ	SS1 ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH, TscL2ssH	SS1 ↑ after SCK1 Edge	1.5 Tcy + 40	—	_	ns	(Note 4)	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A

	Units	N	MILLIMETERS	
Dimension	Limits	MIN	NOM	MAX
Number of Pins	Ν	36		
Number of Pins per Side	ND	10		
Number of Pins per Side	NE	8		
Pitch	е	0.50 BSC		
Overall Height	А	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	3.60	3.75	3.90
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.60	3.75	3.90
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2