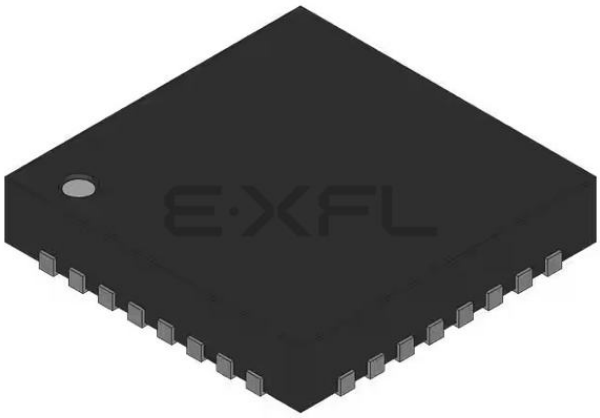

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	-
Interface	-
Clock Rate	-
Non-Volatile Memory	-
On-Chip RAM	-
Voltage - I/O	-
Voltage - Core	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1461wbcpz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Mute Attenuation	PGA muted				
	LDMUTE, RDMUTE = 0		−76	−73	dB
	RDBOOST[1:0], LDBOOST[1:0] = 00		−87	−82	dB
Interchannel Gain Mismatch		−0.6	−0.073	+0.6	dB
Offset Error		−6	0	+6	mV
Gain Error		−24	−14	−3	%
Interchannel Isolation			83		dB
Common-Mode Rejection Ratio	100 mV rms, 1 kHz		−58		dB
	100 mV rms, 20 kHz	−52	−48	−44	dB
FULL DIFFERENTIAL PGA INPUT	Differential PGA inputs				
Full-Scale Input Voltage (0 dB)			1.0 (2.83)		V rms (V p-p)
Dynamic Range	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)		94	98		dB
No Filter (RMS)		91	95		dB
Total Harmonic Distortion + Noise	−1 dBFS		−78	−74	dB
Signal-to-Noise Ratio					
With A-Weighted Filter (RMS)			98		dB
No Filter (RMS)			95		dB
PGA Boost Gain Error	20 dB gain setting (RDBOOST[1:0], LDBOOST[1:0] = 10)	−8	−0.15	+8	dB
Mute Attenuation	PGA muted				
	LDMUTE, RDMUTE = 0		−76	−73	dB
	RDBOOST[1:0], LDBOOST[1:0] = 00		−87	−82	dB
Interchannel Gain Mismatch		−0.3	−0.0005	+0.3	dB
Offset Error		−6	0	+6	mV
Gain Error		−17	−14	−9	%
Interchannel Isolation			83		dB
Common-Mode Rejection Ratio	100 mV rms, 1 kHz		−58		dB
	100 mV rms, 20 kHz	−52	−48	−44	dB
MICROPHONE BIAS	MBIEN = 1				
Bias Voltage					
0.65 × AVDD	MBI = 1, MPERF = 0	2.00	2.145	2.19	V
	MBI = 1, MPERF = 1	2.04	2.13	2.21	V
0.90 × AVDD	MBI = 0, MPERF = 0	2.89	2.97	3.04	V
	MBI = 0, MPERF = 1	2.89	2.99	3.11	V
Bias Current Source	MBI = 0, MPERF = 1			3	mA
Noise in the Signal Bandwidth	1 kHz to 20 kHz				
	MBI = 0, MPERF = 0		42		nV/√Hz
	MBI = 0, MPERF = 1		85		nV/√Hz
	MBI = 1, MPERF = 0		25		nV/√Hz
	MBI = 1, MPERF = 1	13	22	36	nV/√Hz
DIGITAL-TO-ANALOG CONVERTERS	DAC performance excludes mixers and headphone amplifier				
DAC Resolution	All DACs		24		Bits
Digital Attenuation Step			0.375		dB
Digital Attenuation Range			95		dB
DAC TO LINE OUTPUT					
Full-Scale Output Voltage (0 dB)			0.92 (2.60)		V rms (V p-p)
Dynamic Range	20 Hz to 20 kHz, −60 dBFS input, line output mode				
With A-Weighted Filter (RMS)		95	101		dB
No Filter (RMS)		93.5	98		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Total Harmonic Distortion + Noise	0 dBFS, 10 kΩ load				
Line Output Mode			−92	−77	dB
Headphone Output Mode			−89	−79	dB
Signal-to-Noise Ratio	Line output mode				
With A-Weighted Filter (RMS)			101		dB
No Filter (RMS)			98		dB
Mute Attenuation					
Mixer 3 and Mixer 4 Muted	MX3RM, MX3LM, MX4RM, MX4LM = 0, MX3AUXG[3:0], MX4AUXG[3:0] = 0000, MX3G1[3:0], MX3G2[3:0] = 0000, MX4G1[3:0], MX4G2[3:0] = 0000		−85	−78	dB
Mixer 5, Mixer 6, and Mixer 7 Muted	MX5G3[1:0], MX5G4[1:0], MX6G3[1:0], MX6G4[1:0], MX7[1:0] = 00		−89	−80	dB
All Volume Controls Muted	LOUTM, ROUTM = 0		−82	−74	dB
	MONOM, LHPM, RHPM = 0		−74	−69	dB
Interchannel Gain Mismatch		−0.3	−0.005	+0.3	dB
Offset Error		−22	0	+22	mV
Gain Error		−10	+3	+10	%
Interchannel Isolation	1 kHz, 0 dBFS input signal		100		dB
Power Supply Rejection Ratio	CM capacitor = 20 µF, 100 mV p-p @ 1 kHz		70		dB
DAC TO HEADPHONE/EARPIECE OUTPUT	LOUTx, ROUTx, LHP, RHP in headphone output mode; P_O = output power per channel				
Full-Scale Output Voltage (0 dB)	Scales linearly with AVDD		0.92 (2.60)		V rms (V p-p)
Total Harmonic Distortion + Noise	−4 dBFS, 16 Ω load, P_O = 21.1 mW		−82		dB
	−4 dBFS, 32 Ω load, P_O = 10.6 mW		−82		dB
Capless Headphone Mode	−2 dBFS, 16 Ω load		−78	−71	dB
	−2 dBFS, 32 Ω load		−75	−65	dB
Headphone Output Mode	0 dBFS, 10 kΩ load		−86	−77	dB
Interchannel Isolation	1 kHz, 0 dBFS input signal, 32 Ω load				
	Referred to GND		73		dB
	Referred to CM (capless headphone mode)		50		dB
Power Supply Rejection Ratio	CM capacitor = 20 µF, 100 mV p-p @ 1 kHz		67		dB
REFERENCE					
Common-Mode Reference Output	CM pin	1.62	1.65	1.67	V

ANALOG PERFORMANCE SPECIFICATIONS, −40°C < T_A < +105°C

IOVDD = 3.3 V ± 10%.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SINGLE-ENDED LINE INPUT					
Dynamic Range	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)		74			dB
No Filter (RMS)		71			dB
Total Harmonic Distortion + Noise	−1 dBFS			−67	dB
Input Mixer Gain per Step	−12 dB to +6 dB range	2.88		3.09	dB
Mute Attenuation	LINPG[2:0], LINNG[2:0] = 000, RINPG[2:0], RINNG[2:0] = 000, MX1AUXG[2:0], MX2AUXG[2:0] = 000			−77	dB
Interchannel Gain Mismatch		−0.5		+0.5	dB
Offset Error		−5		+5	mV
Gain Error		−22		−6	%

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PSEUDO-DIFFERENTIAL PGA INPUT					
Dynamic Range	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)		94			dB
No Filter (RMS)		91			dB
Total Harmonic Distortion + Noise	−1 dBFS			−75	dB
PGA Boost Gain Error	20 dB gain setting (RDBOOST[1:0], LDBOOST[1:0] = 10)	−11		−7	dB
Mute Attenuation	PGA muted				
	LDMUTE, RDMUTE = 0			−73	dB
	RDBOOST[1:0], LDBOOST[1:0] = 00			−82	dB
Interchannel Gain Mismatch		−0.6		+0.6	dB
Offset Error		−6		+6	mV
Gain Error		−24		−3	%
Common-Mode Rejection Ratio	100 mV rms, 1 kHz	−64		−38	dB
	100 mV rms, 20 kHz	−53		−43	dB
FULL DIFFERENTIAL PGA INPUT	Differential PGA inputs				
Dynamic Range	20 Hz to 20 kHz, −60 dB input				
With A-Weighted Filter (RMS)		89			dB
No Filter (RMS)		86			dB
Total Harmonic Distortion + Noise	−1 dBFS			−70	dB
PGA Boost Gain Error	20 dB gain setting (RDBOOST[1:0], LDBOOST[1:0] = 10)	−11		−7	dB
Mute Attenuation	PGA muted				
	LDMUTE, RDMUTE = 0			−73	dB
	RDBOOST[1:0], LDBOOST[1:0] = 00			−82	dB
Interchannel Gain Mismatch		−0.4		+0.4	dB
Offset Error		−6		+6	mV
Gain Error		−21		−7	%
Common-Mode Rejection Ratio	100 mV rms, 1 kHz	−64		−38	dB
	100 mV rms, 20 kHz	−53		−43	dB
MICROPHONE BIAS	MBIEN = 1				
Bias Voltage					
0.65 × AVDD	MBI = 1, MPERF = 0	1.85		2.45	V
	MBI = 1, MPERF = 1	1.87		2.45	V
0.90 × AVDD	MBI = 0, MPERF = 0	2.65		3.40	V
	MBI = 0, MPERF = 1	2.65		3.40	V
Noise in the Signal Bandwidth	1 kHz to 20 kHz	11		36	nV/√Hz
DAC TO LINE OUTPUT					
Dynamic Range	20 Hz to 20 kHz, −60 dB input, line output mode				
With A-Weighted Filter (RMS)		85			dB
No Filter (RMS)		78			dB
Total Harmonic Distortion + Noise	0 dBFS, 10 kΩ load				
Line Output Mode				−76	dB
Headphone Output Mode				−78	dB
Mute Attenuation					
Mixer 3 and Mixer 4 Muted	MX3RM, MX3LM, MX4RM, MX4LM = 0, MX3AUXG[3:0], MX4AUXG[3:0] = 0000, MX3G1[3:0], MX3G2[3:0] = 0000, MX4G1[3:0], MX4G2[3:0] = 0000			−77	dB
Mixer 5, Mixer 6, and Mixer 7 Muted	MX5G3[1:0], MX5G4[1:0], MX6G3[1:0], MX6G4[1:0], MX7[1:0] = 00			−77	dB
All Volume Controls Muted	LOUTM, ROUTM = 0			−74	dB
	MONOM, LHPM, RHPM = 0			−69	dB

DIGITAL TIMING SPECIFICATIONS

−40°C < T_A < +105°C, IOVDD = 3.3 V ± 10%.

Table 6. Digital Timing

	Limit			
Parameter	**t_{MIN}**	**t_{MAX}**	**Unit**	**Description**
MASTER CLOCK				
t_{MP}	74	488	ns	MCLK period, 256 × f_S mode.
t_{MP}	37	244	ns	MCLK period, 512 × f_S mode.
t_{MP}	24.7	162.7	ns	MCLK period, 768 × f_S mode.
t_{MP}	18.5	122	ns	MCLK period, 1024 × f_S mode.
SERIAL PORT				
t_{BIL}	5		ns	BCLK pulse width low.
t_{BIH}	5		ns	BCLK pulse width high.
t_{LIS}	5		ns	LRCLK setup. Time to BCLK rising.
t_{LIH}	5		ns	LRCLK hold. Time from BCLK rising.
t_{SIS}	5		ns	DAC_SDATA setup. Time to BCLK rising.
t_{SIH}	5		ns	DAC_SDATA hold. Time from BCLK rising.
t_{SODM}		50	ns	ADC_SDATA delay. Time from BCLK falling in master mode.
SPI PORT				
f_{CCLK}		10	MHz	CCLK frequency.
t_{CCPL}	10		ns	CCLK pulse width low.
t_{CCPH}	10		ns	CCLK pulse width high.
t_{CLS}	5		ns	$\overline{\text{CLATCH}}$ setup. Time to CCLK rising.
t_{CLH}	10		ns	$\overline{\text{CLATCH}}$ hold. Time from CCLK rising.
t_{CLPH}	10		ns	$\overline{\text{CLATCH}}$ pulse width high.
t_{CDS}	5		ns	CDATA setup. Time to CCLK rising.
t_{CDH}	5		ns	CDATA hold. Time from CCLK rising.
t_{COD}		50	ns	COUT three-stated. Time from $\overline{\text{CLATCH}}$ rising.
I²C PORT				
f_{SCL}		400	kHz	SCL frequency.
t_{SCLH}	0.6		µs	SCL high.
t_{SCLL}	1.3		µs	SCL low.
t_{SCS}	0.6		µs	Setup time; relevant for repeated start condition.
t_{SCH}	0.6		µs	Hold time. After this period, the first clock is generated.
t_{DS}	100		ns	Data setup time.
t_{SCR}		300	ns	SCL rise time.
t_{SCF}		300	ns	SCL fall time.
t_{SDR}		300	ns	SDA rise time.
t_{SDF}		300	ns	SDA fall time.
t_{BFT}	0.6		µs	Bus-free time. Time between stop and start.
DIGITAL MICROPHONE				R_{LOAD} = 1 MΩ, C_{LOAD} = 14 pF.
t_{DCF}		10	ns	Digital microphone clock fall time.
t_{DCR}		10	ns	Digital microphone clock rise time.
t_{DDV}	22	30	ns	Digital microphone delay time for valid data.
t_{DDH}	0	12	ns	Digital microphone delay time for data three-stated.

Pin No.	Mnemonic	Type[1]	Description
19	RHP	A_OUT	Right Headphone Output. Biased at AVDD/2.
20	LHP	A_OUT	Left Headphone Output. Biased at AVDD/2.
21	MONOOUT	A_OUT	Mono Output or Virtual Ground for Capless Headphone. Biased at AVDD/2 when set as mono output.
22	AGND	PWR	Analog Ground. The AGND and DGND pins can be tied together on a common ground plane. AGND should be decoupled locally to AVDD with a 100 nF capacitor.
23	AVDD	PWR	3.3 V Analog Supply for ADC, Output Driver, and Input to Digital Supply Regulator. This pin should be decoupled locally to AGND with a 100 nF capacitor.
24	DVDDOUT	PWR	Digital Core Supply Decoupling Point. The digital supply is generated from an on-board regulator and does not require an external supply. DVDDOUT should be decoupled to DGND with a 100 nF capacitor and a 10 µF capacitor.
25	DGND	PWR	Digital Ground. The AGND and DGND pins can be tied together on a common ground plane. DGND should be decoupled to DVDDOUT and to IOVDD with 100 nF capacitors and 10 µF capacitors.
26	ADC_SDATA/GPIO1	D_IO	ADC Serial Output Data (ADC_SDATA). General-Purpose Input/Output 1 (GPIO1).
27	DAC_SDATA/GPIO0	D_IO	DAC Serial Input Data (DAC_SDATA). General-Purpose Input/Output 0 (GPIO0).
28	BCLK/GPIO2	D_IO	Serial Data Port Bit Clock (BCLK). General-Purpose Input/Output 2 (GPIO2).
29	LRCLK/GPIO3	D_IO	Serial Data Port Frame Clock (LRCLK). General-Purpose Input/Output 3 (GPIO3).
30	ADDR1/CDATA	D_IN	I²C Address Bit 1 (ADDR1). SPI Data Input (CDATA).
31	SDA/COUT	D_IO	I²C Data (SDA). This pin is a bidirectional open-collector input/output. The line connected to this pin should have a 2 kΩ pull-up resistor. SPI Data Output (COUT). This pin is used for reading back registers and memory locations. It is three-state when an SPI read is not active.
32	SCL/CCLK	D_IN	I²C Clock (SCL). This pin is always an open-collector input when in I²C control mode. The line connected to this pin should have a 2 kΩ pull-up resistor. SPI Clock (CCLK). This pin can run continuously or be gated off between SPI transactions.
EP	Exposed Pad		Exposed Pad. The exposed pad is connected internally to the ADAU1461 grounds. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the ground plane. See the Exposed Pad PCB Design section for more information.

[1] A_IN = analog input, A_OUT = analog output, D_IN = digital input, D_IO = digital input/output, PWR = power.

TYPICAL PERFORMANCE CHARACTERISTICS

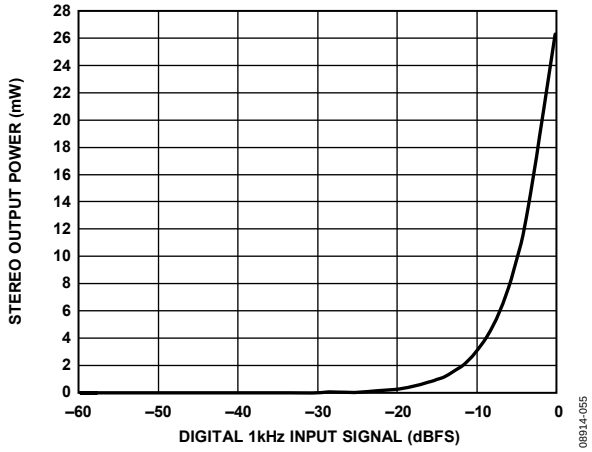

Figure 8. Headphone Amplifier Power vs. Input Level, 16 Ω Load

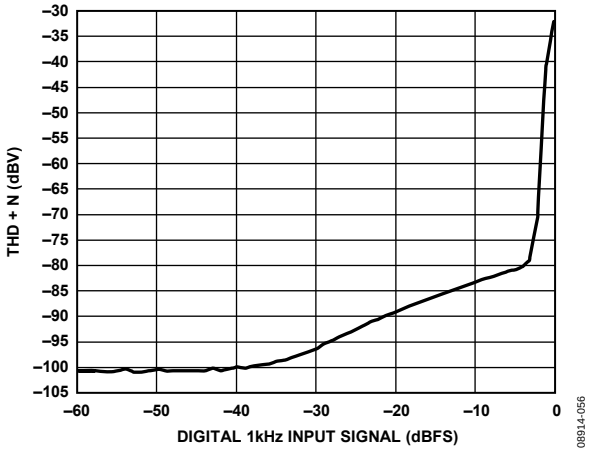

Figure 11. Headphone Amplifier THD + N vs. Input Level, 16 Ω Load

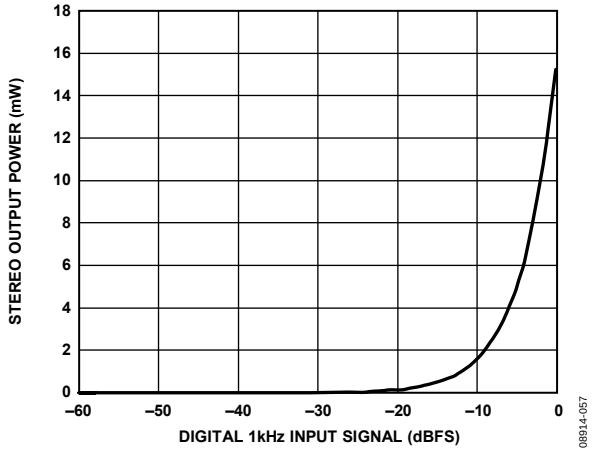

Figure 9. Headphone Amplifier Power vs. Input Level, 32 Ω Load

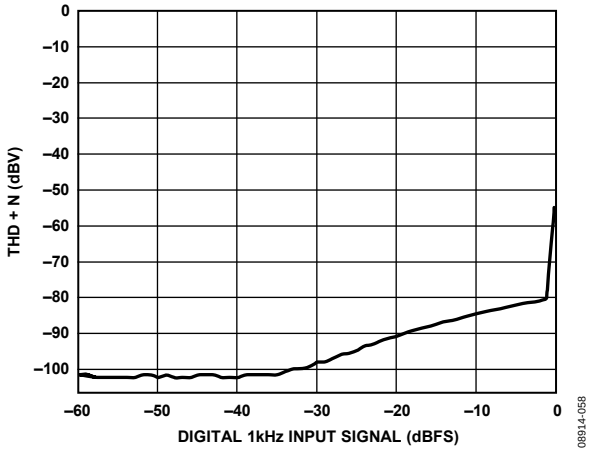

Figure 12. Headphone Amplifier THD + N vs. Input Level, 32 Ω Load

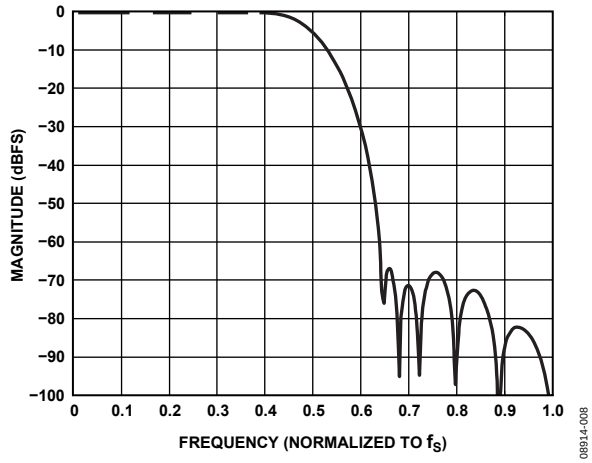

Figure 10. ADC Decimation Filter, 64× Oversampling, Normalized to f_S

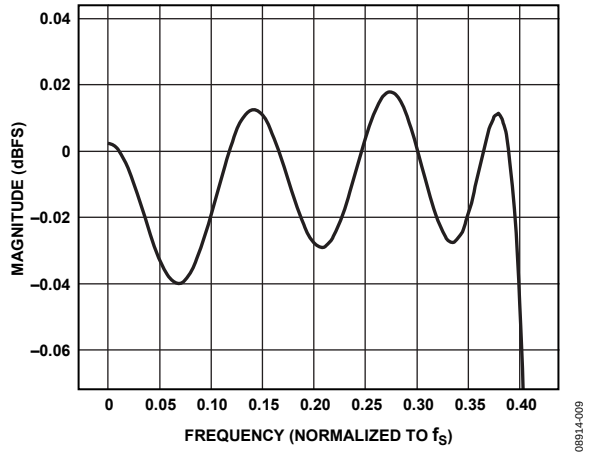

Figure 13. ADC Decimation Filter Pass-Band Ripple, 64× Oversampling, Normalized to f_S

RECORD SIGNAL PATH

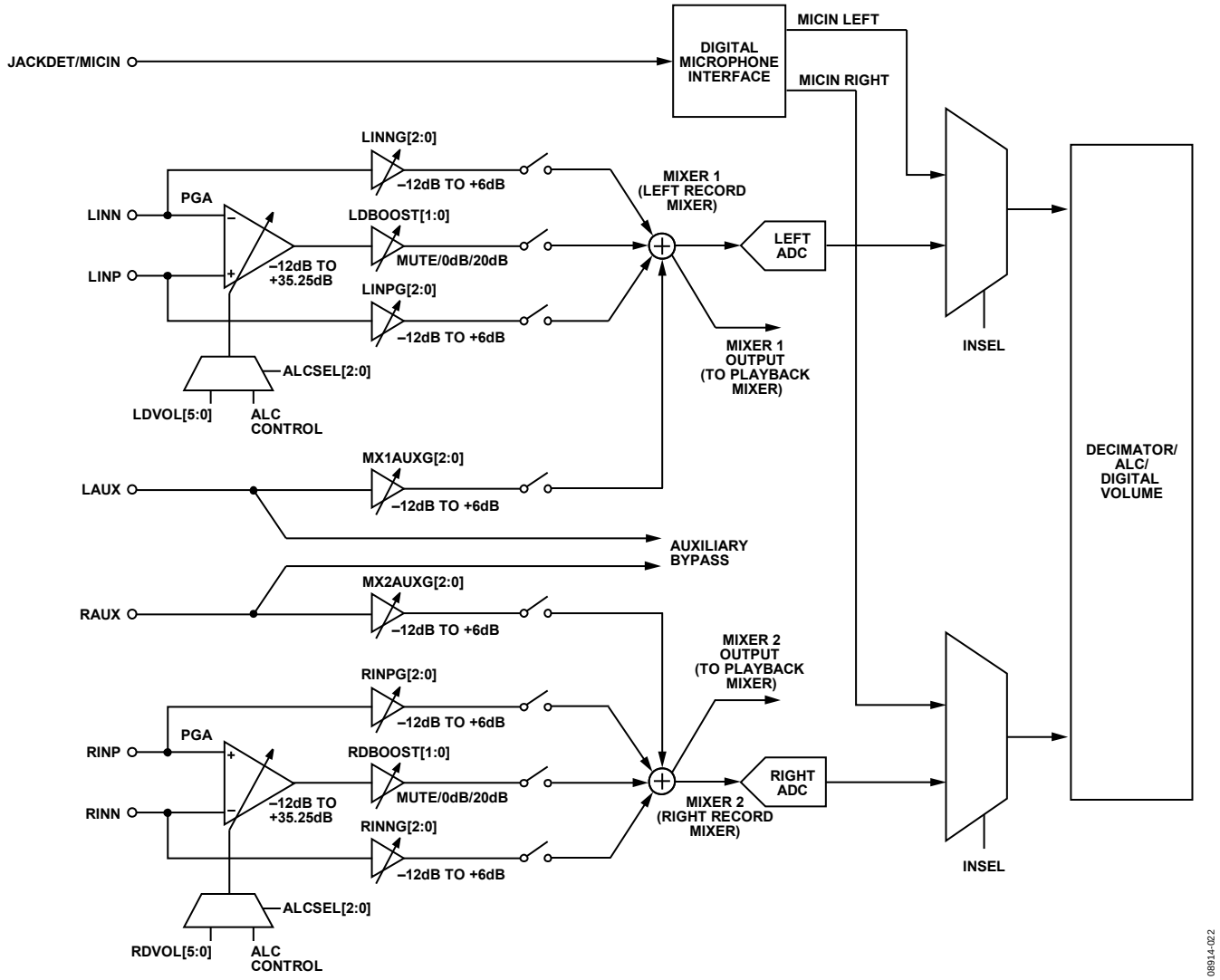

Figure 32. Record Signal Path

INPUT SIGNAL PATHS

The ADAU1461 can accept both line level and microphone inputs. The analog inputs can be configured in a single-ended or differential configuration. There is also an input for a digital microphone. The analog inputs are biased at AVDD/2. Unused input pins should be connected to CM.

Each of the six analog inputs has individual gain controls (boost or cut). The input signals are mixed and routed to an ADC. The mixed input signals can also bypass the ADCs and be routed directly to the playback mixers. Left channel inputs are mixed before the left ADC; however, it is possible to route the mixed analog signal around the ADC and output it into a left or right output channel. The same capabilities apply to the right channel and the right ADC.

Signals are inverted through the PGAs and the mixers. The result of this inversion is that differential signals input through the PGA are output from the ADCs at the same polarity as they are input. Single-ended inputs that pass through the mixer but not through the PGA are inverted. The ADCs are noninverting.

The input impedance of the analog inputs varies with the gain of the PGA. This impedance ranges from 1.7 kΩ at the 35.25 dB gain setting to 80.4 kΩ at the −12 dB setting. This range is shown in Figure 25.

Digital Microphone Input

When using a digital microphone connected to the JACKDET/MICIN pin, the JDFUNC[1:0] bits in Register R2 (Address 0x4008) must be set to 10 to enable the microphone input and disable the jack detection function. The ADAU1461 must operate in master mode and source BCLK to the input clock of the digital microphone. The DSPRUN bit must also be asserted in Register R62 (DSP run register, Address 0x40F6) for digital microphone operation.

The digital microphone signal bypasses record path mixers and ADCs and is routed directly into the decimation filters. The digital microphone and ADCs share decimation filters and, therefore, both cannot be used simultaneously. The digital microphone input select bit, INSEL, can be set in Register R19 (ADC control register, Address 0x4019). Figure 36 depicts the digital microphone interface and signal routing.

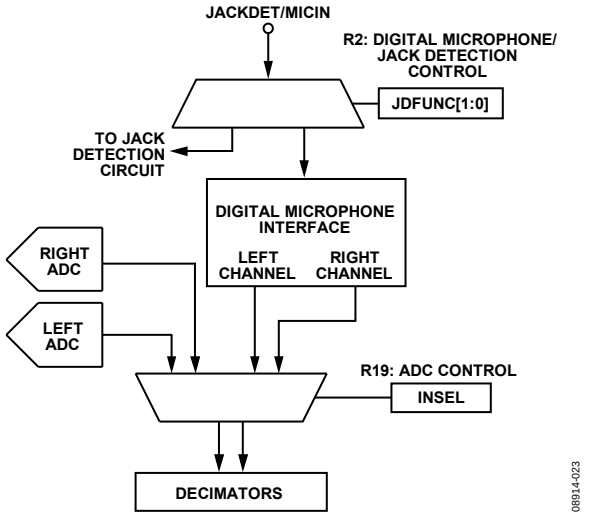

Figure 36. Digital Microphone Interface Block Diagram

Microphone Bias

The MICBIAS pin provides a voltage reference for electret analog microphones. The MICBIAS voltage is set in Register R10 (record microphone bias control register, Address 0x4010). In this register, the MICBIAS output can be enabled or disabled. Additional options include high performance operation and a gain boost. The gain boost provides two different voltage biases: 0.65 × AVDD or 0.90 × AVDD. When enabled, the high performance bit increases supply current to the microphone bias circuit to decrease rms input noise.

The MICBIAS pin can also be used to cleanly supply voltage to digital microphones or analog microphones with separate power supply pins.

ANALOG-TO-DIGITAL CONVERTERS

The ADAU1461 uses two 24-bit Σ-Δ analog-to-digital converters (ADCs) with selectable oversampling ratios of 64× or 128× (selected by Bit 3 in Register R17, Address 0x4017).

ADC Full-Scale Level

The full-scale input to the ADCs (0 dBFS) is 1.0 V rms with AVDD = 3.3 V. This full-scale analog input will output a digital signal at −1.38 dBFS. This gain offset is built into the ADAU1461 to prevent clipping. The full-scale input level scales linearly with the level of AVDD.

For single-ended and pseudo-differential signals, the full-scale value corresponds to the signal level at the pins, 0 dBFS.

The full differential full-scale input level is measured after the differential amplifier, which corresponds to −6 dBFS at each pin.

Signal levels above the full-scale value cause the ADCs to clip.

Digital ADC Volume Control

The digital ADC volume can be attenuated before DSP processing using Register R20 (left input digital volume register, Address 0x401A) and Register R21 (right input digital volume register, Address 0x401B).

High-Pass Filter

By default, a high-pass filter is used in the ADC path to remove dc offsets; this filter can be enabled or disabled in Register R19 (ADC control register, Address 0x4019). At f_S = 48 kHz, the corner frequency of this high-pass filter is 2 Hz.

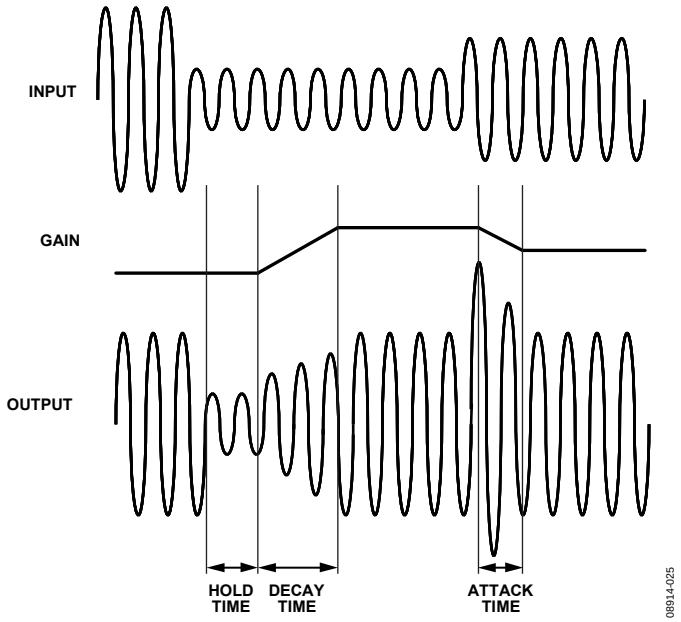

Figure 38. Basic ALC Operation

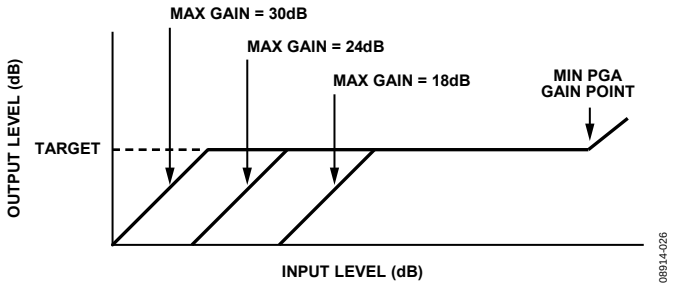

Figure 39. Effect of Varying the Maximum Gain Parameter

NOISE GATE FUNCTION

When using the ALC, one potential problem is that for small input signals, the PGA gain can become very large. A side effect of this is that the noise is amplified along with the signal of interest. To avoid this situation, the ADAU1461 noise gate can be used. The noise gate cuts off the ADC output when its signal level is below a set threshold. The noise gate is controlled using the following parameters in the ALC Control 3 register (Address 0x4014):

- NGTYP[1:0]: The noise gate type is set to one of four modes by writing to the NGTYP[1:0] bits.
- NGEN: The noise gate function is enabled by writing to the NGEN bit.
- NGTHR[4:0]: The threshold for muting the output is set by writing to the NGTHR[4:0] bits.

One common problem with noise gate functions is chatter, where a small signal that is close to the noise gate threshold varies in amplitude, causing the noise gate function to open and close rapidly. This causes an unpleasant sound.

To reduce this effect, the noise gate in the ADAU1461 uses a combination of a timeout period and hysteresis. The timeout period is set to 250 ms, so the signal must consistently be below the threshold for 250 ms before the noise gate operates. Hysteresis is used so that the threshold for coming out of the mute state is 6 dB higher than the threshold for going into the mute state. There are four operating modes for the noise gate.

Noise Gate Mode 0 (see Figure 40) is selected by setting the NGTYP[1:0] bits to 00. In this mode, the current state of the PGA gain is held at its current state when the noise gate logic is activated. This prevents a large increase in background noise during periods of silence. When using this mode, it is advisable to use a relatively slow decay time. This is because the noise gate takes at least 250 ms to activate, and if the PGA gain has already increased to a large value during this time, the value at which the gain is held will be large.

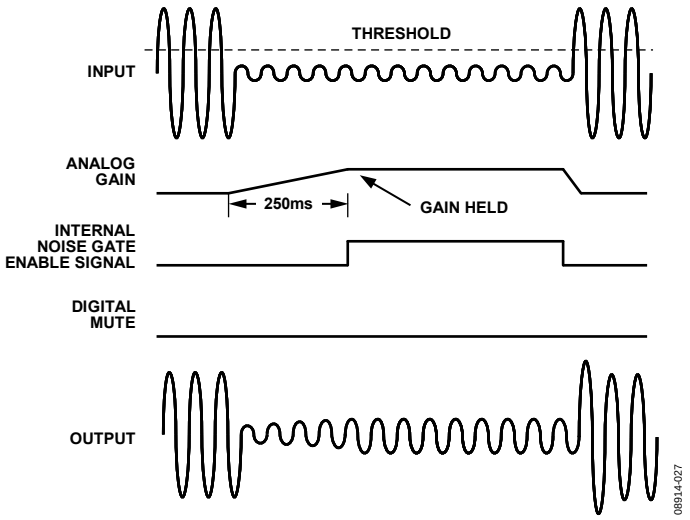

Figure 40. Noise Gate Mode 0 (PGA Gain Hold)

Noise Gate Mode 1 (see Figure 41) is selected by setting the NGTYP[1:0] bits to 01. In this mode, the ADAU1461 does a simple digital mute of the ADC output. Although this mode completely eliminates any background noise, the effect of an abrupt mute may not be pleasant to the ear.

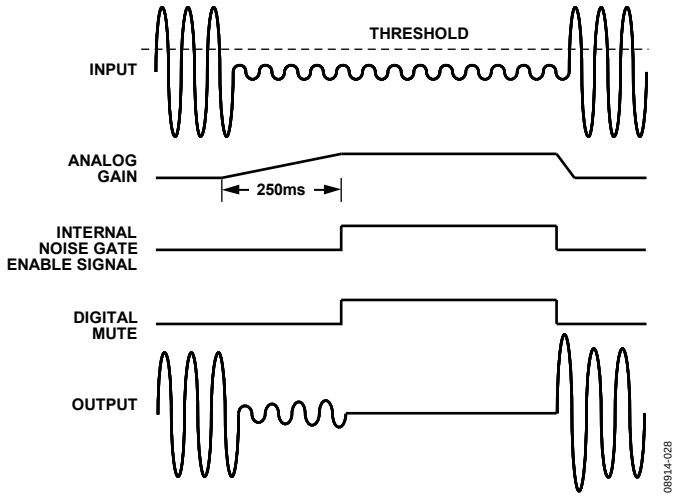

Figure 41. Noise Gate Mode 1 (Digital Mute)

Noise Gate Mode 2 (see Figure 42) is selected by setting the NGTYP[1:0] bits to 10. In this mode, the ADAU1461 improves the sound of the noise gate operation by first fading the PGA gain over a period of about 100 ms to the minimum PGA gain value. The ADAU1461 does not do a hard mute after the fade is complete, so some small background noise will still exist.

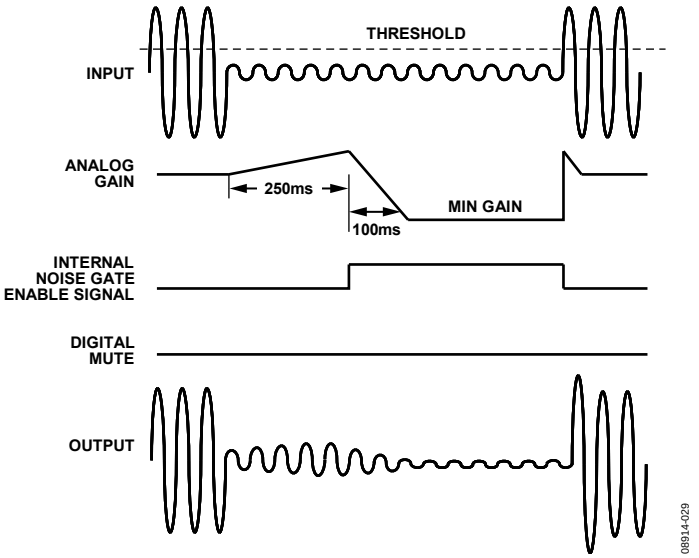

Figure 42. Noise Gate Mode 2 (Analog Fade)

Noise Gate Mode 3 (see Figure 43) is selected by setting the NGTYP[1:0] bits to 11. This mode is the same as Mode 2 except that at the end of the PGA fade gain interval, a digital mute is performed. In general, this mode is the best-sounding mode, because the audible effect of the digital hard mute is reduced by the fact that the gain has already faded to a low level before the mute occurs.

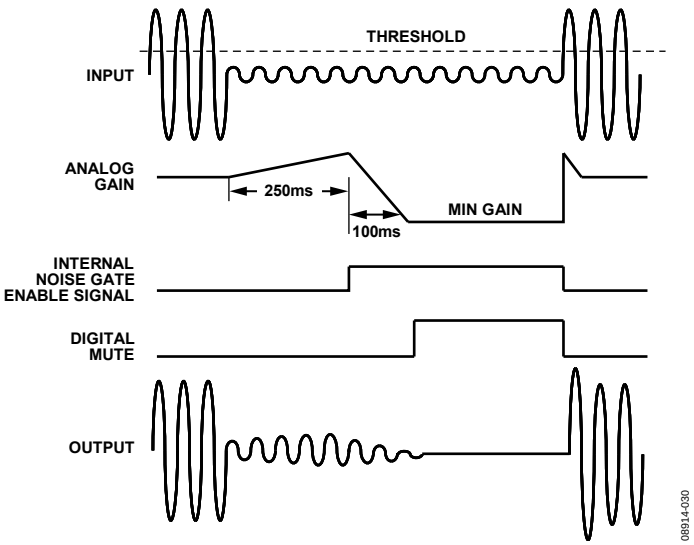

Figure 43. Noise Gate Mode 3 (Analog Fade/Digital Mute)

SPI PORT

By default, the ADAU1461 is in I²C mode, but it can be put into SPI control mode by pulling $\overline{\text{CLATCH}}$ low three times. This is done by performing three dummy writes to the SPI port (the ADAU1461 does not acknowledge these three writes). Beginning with the fourth SPI write, data can be written to or read from the IC. The ADAU1461 can be taken out of SPI mode only by a full reset initiated by power-cycling the IC.

The SPI port uses a 4-wire interface, consisting of the $\overline{\text{CLATCH}}$, CCLK, CDATA, and COUT signals, and it is always a slave port. The $\overline{\text{CLATCH}}$ signal should go low at the beginning of a transaction and high at the end of a transaction. The CCLK signal latches CDATA on a low-to-high transition. COUT data is shifted out of the ADAU1461 on the falling edge of CCLK and should be clocked into a receiving device, such as a microcontroller, on the CCLK rising edge. The CDATA signal carries the serial input data, and the COUT signal carries the serial output data. The COUT signal remains three-state until a read operation is requested. This allows other SPI-compatible peripherals to share the same readback line. All SPI transactions have the same basic format shown in Table 22. A timing diagram is shown in Figure 4. All data should be written MSB first.

Chip Address R/$\overline{W}$

The LSB of the first byte of an SPI transaction is a R/$\overline{\text{W}}$ bit. This bit determines whether the communication is a read (Logic Level 1) or a write (Logic Level 0). This format is shown in Table 21.

Table 21. ADAU1461 SPI Address and Read/$\overline{\text{Write}}$ Byte Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	0	0	0	0	0	0	R/$\overline{\text{W}}$

Subaddress

The 16-bit subaddress word is decoded into a location in one of the registers. This subaddress is the location of the appropriate register. The MSBs of the subaddress are zero-padded to bring the word to a full 2-byte length.

Data Bytes

The number of data bytes varies according to the register being accessed. During a burst mode write, an initial subaddress is written followed by a continuous sequence of data for consecutive register locations.

A sample timing diagram for a single-word SPI write operation to a register is shown in Figure 55. A sample timing diagram of a single-word SPI read operation is shown in Figure 56. The COUT pin goes from being three-state to being driven at the beginning of Byte 3. In this example, Byte 0 to Byte 2 contain the addresses and R/$\overline{\text{W}}$ bit, and subsequent bytes carry the data.

Table 22. Generic Control Word Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4[1]
chip_adr[6:0], R/$\overline{\text{W}}$	subaddr[15:8]	subaddr[7:0]	data	data

[1] Continues to end of data.

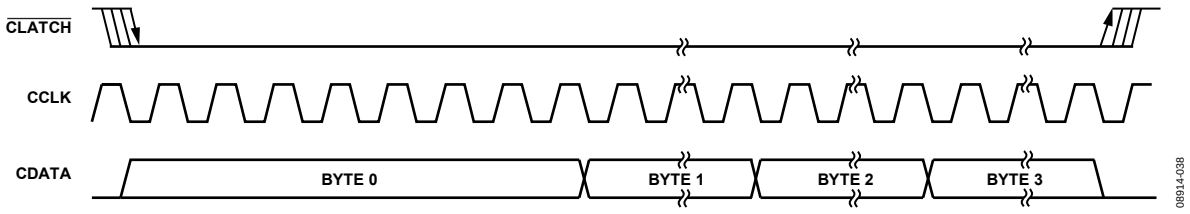

Figure 55. SPI Write to ADAU1461 Clocking (Single-Word Write Mode)

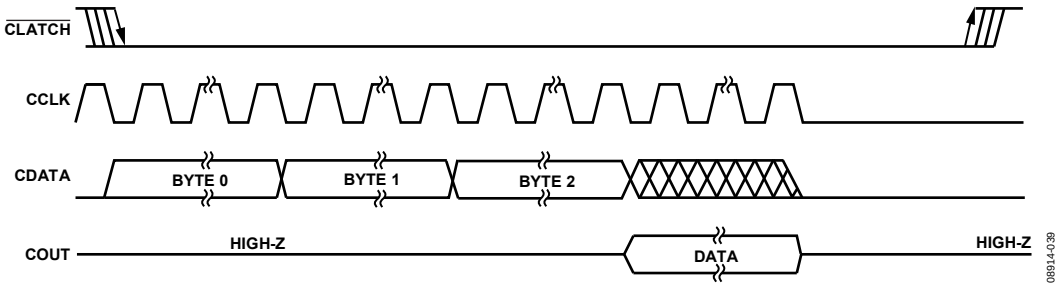

Figure 56. SPI Read from ADAU1461 Clocking (Single-Word Read Mode)

NUMERIC FORMATS

DSP systems commonly use a standard numeric format. Fractional numeric systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The ADAU1461 uses numeric format 5.23 for both the parameter and data values.

Numeric Format 5.23

Linear range: −16.0 to (+16.0 − 1 LSB)

Examples:
1000 0000 0000 0000 0000 0000 0000 = −16.0
1110 0000 0000 0000 0000 0000 0000 = −4.0
1111 1000 0000 0000 0000 0000 0000 = −1.0
1111 1110 0000 0000 0000 0000 0000 = −0.25
1111 1111 0011 0011 0011 0011 0011 = −0.1
1111 1111 1111 1111 1111 1111 1111 = (1 LSB below 0)
0000 0000 0000 0000 0000 0000 0000 = 0
0000 0000 1100 1100 1100 1100 1101 = 0.1
0000 0010 0000 0000 0000 0000 0000 = 0.25
0000 1000 0000 0000 0000 0000 0000 = 1.0
0010 0000 0000 0000 0000 0000 0000 = 4.0
0111 1111 1111 1111 1111 1111 1111 = (16.0 − 1 LSB)

The serial port accepts up to 24 bits on the input and is sign-extended to the full 28 bits of the DSP core. This allows internal gains of up to 24 dB without internal clipping.

A digital clipper circuit is used between the output of the DSP core and the DACs or serial port outputs (see Figure 68). This circuit clips the top four bits of the signal to produce a 24-bit output with a range of 1.0 (minus 1 LSB) to −1.0. Figure 68 shows the maximum signal levels at each point in the data flow in both binary and decibel levels.

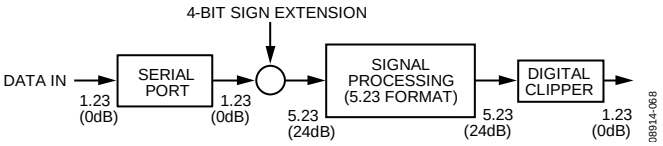

Figure 68. Numeric Precision and Clipping Structure

PROGRAMMING

On power-up, the ADAU1461 must be configured with a clocking scheme and then loaded with register settings. After the codec signal path is set up, the DSP core can be programmed. There are 1024 instruction cycles per audio sample, resulting in an internal clock rate of 49.152 MHz when f_S = 48 kHz.

The part can be programmed easily using SigmaStudio, a graphical tool provided by Analog Devices (see Figure 69). No knowledge of writing line-level DSP code is required. More information about SigmaStudio can be found at www.analog.com.

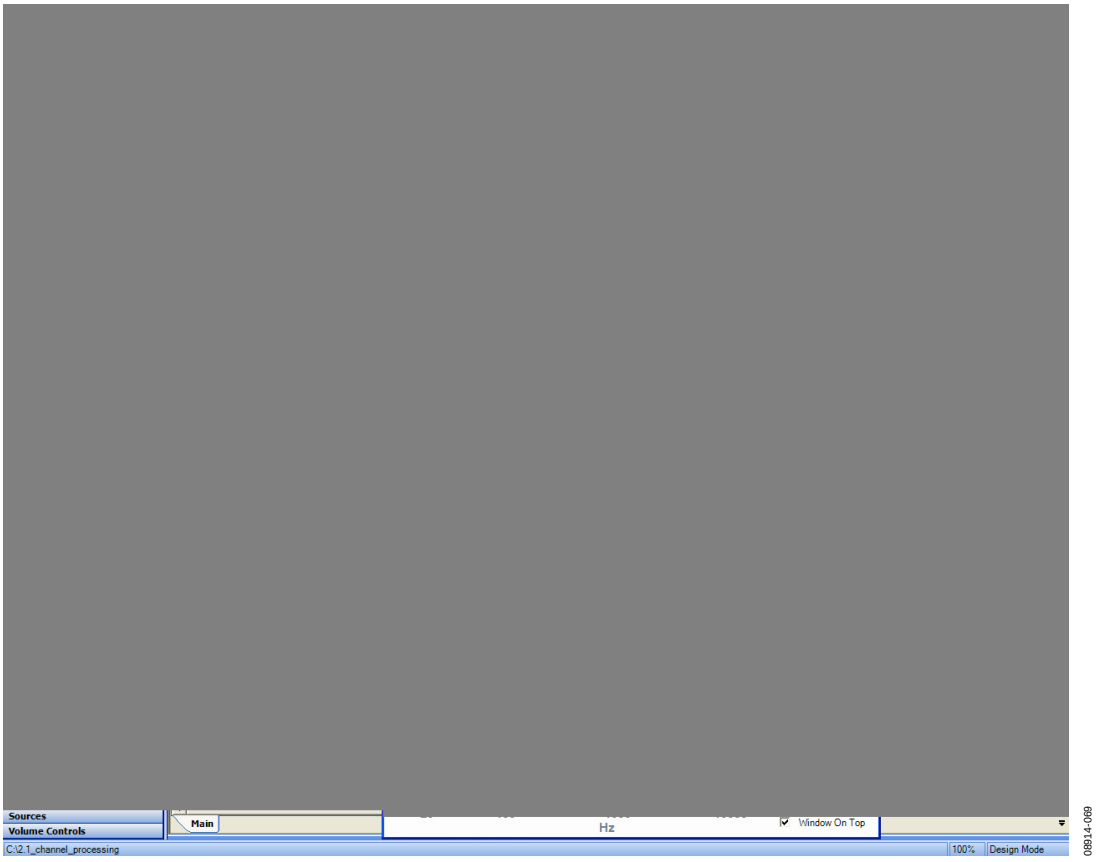

Figure 69. SigmaStudio Screen Shot

PROGRAM RAM, PARAMETER RAM, AND DATA RAM

Table 25. RAM Map and Read/Write Modes

Memory	Size	Address Range	Read	Write	Write Modes
Parameter RAM	1024 × 32	0 to 1023 (0x0000 to 0x03FF)	Yes	Yes	Direct, safeload
Program RAM	1024 × 40	2048 to 3071 (0x0800 to 0x0BFF)	Yes	Yes	Direct

Table 25 shows the RAM map (the ADAU1461 register map is provided in the Control Registers section). The address space encompasses a set of registers and three RAMs: program, parameter, and data. The program RAM and parameter RAM are not initialized on power-up and are in an unknown state until written to.

PROGRAM RAM

The program RAM contains the 40-bit operation codes that are executed by the core. The SigmaStudio compiler calculates maximum instructions per frame for a project and generates an error when the value exceeds the maximum allowable instructions per frame based on the sample rate of the signals in the core.

Because the end of a program contains a jump-to-start command, the unused program RAM space does not need to be filled with no-operation (NOP) commands.

PARAMETER RAM

The parameter RAM is 32 bits wide and occupies Address 0 to Address 1023. Each parameter is padded with four 0s before the MSB to extend the 28-bit word to a full 4-byte width. The data format of the parameter RAM is twos complement, 5.23. This means that the coefficients can range from +16.0 (minus 1 LSB) to −16.0, with 1.0 represented by the binary word 0000 1000 0000 0000 0000 0000 0000 or by the hexadecimal word 0x00 0x80 0x00 0x00.

The parameter RAM can be written to directly or with a safeload write. The direct write mode of operation is typically used during a complete new loading of the RAM using burst mode addressing to avoid any clicks or pops in the outputs. Note that this mode can be used during live program execution, but because there is no handshaking between the core and the control port, the parameter RAM is unavailable to the DSP core during control writes, resulting in pops and clicks in the audio stream.

SigmaStudio automatically assigns the first eight positions to safeload parameters; therefore, project-specific parameters start at Address 0x0008.

The parameter RAM should not be written to until the DSPEN bit has been set in Register R61 (Address 0x40F5).

DATA RAM

The ADAU1461 data RAM is used to store audio data-words for processing, as well as certain run-time parameters. SigmaStudio provides the data and address information for writing to and reading from the data RAM.

When implementing blocks, such as delays, that require large amounts of data RAM space, data RAM utilization should be taken into account. The SigmaDSP core processes delay times in one-sample increments; therefore, the total pool of delay available to the user equals 4096 multiplied by the sample period. For a $f_{S,DSP}$ of 48 kHz, the pool of available delay is a maximum of about 86 ms, where $f_{S,DSP}$ is the DSP core sampling rate. In practice, this much data memory is not available to the user because every block in a design uses a few data memory locations for its processing. In most DSP programs, this does not significantly affect the total delay time. The SigmaStudio compiler manages the data RAM and indicates whether the number of addresses needed in the design exceeds the maximum number available.

READ/WRITE DATA FORMATS

The read/write formats of the control port are designed to be byte oriented to allow for easy programming of common microcontroller chips. To fit into a byte-oriented format, 0s are added to the data fields before the MSB to extend the data-word to eight bits. For example, 28-bit words written to the parameter RAM are preceded by four leading 0s to equal 32 bits (four bytes); 40-bit words written to the program RAM are not preceded by 0s because they are already a full five bytes. These zero-padded data fields are appended to a 3-byte field consisting of a 7-bit chip address, a read/write bit, and a 16-bit RAM/register address. The control port knows how many data bytes to expect based on the address given in the first three bytes.

The total number of bytes for a single-location write command can vary from one byte (for a control register write) to five bytes (for a program RAM write). Burst mode can be used to fill contiguous register or RAM locations. A burst mode write begins by writing the address and data of the first RAM or register location to be written. Rather than ending the control port transaction (by issuing a stop command in I²C mode or by bringing the CLATCH signal high in SPI mode after the data-word), as would be done in a single-address write, the next data-word can be written immediately without specifying its address. The ADAU1461 control port autoincrements the address of each write even across the boundaries of the different RAMs and registers. Table 27 and Table 29 show examples of burst mode writes.

R6: Record Mixer Right (Mixer 2) Control 0, 16,396 (0x400C)

This register controls the gain of single-ended inputs for the right channel record path. The right channel record mixer is referred to as Mixer 2.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	RINPG[2:0]			RINNG[2:0]			MX2EN

Table 38. Record Mixer Right (Mixer 2) Control 0 Register

Bits	Bit Name	Description	
[6:4]	RINPG[2:0]	Gain for a right channel single-ended input from the RINP pin, input to Mixer 2.	
		Setting	**Gain**
		000	Mute (default)
		001	−12 dB
		010	−9 dB
		011	−6 dB
		100	−3 dB
		101	0 dB
		110	3 dB
		111	6 dB
[3:1]	RINNG[2:0]	Gain for a right channel single-ended input from the RINN pin, input to Mixer 2.	
		Setting	**Gain**
		000	Mute (default)
		001	−12 dB
		010	−9 dB
		011	−6 dB
		100	−3 dB
		101	0 dB
		110	3 dB
		111	6 dB
0	MX2EN	Right channel mixer enable in the record path. Referred to as Mixer 2. 0 = mixer disabled (default). 1 = mixer enabled.	

R11: ALC Control 0, 16,401 (0x4011)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PGASLEW[1:0]		ALCMAX[2:0]			ALCSEL[2:0]		

Table 43. ALC Control 0 Register

Bits	Bit Name	Description	
[7:6]	PGASLEW[1:0]	PGA volume slew time when the ALC is off. The slew time is the period of time that a volume increase or decrease takes to ramp up or ramp down to the target volume set in Register R8 (left differential input volume control) and Register R9 (right differential input volume control).	
		Setting	**Slew Time**
		00	24 ms (default)
		01	48 ms
		10	96 ms
		11	Off
[5:3]	ALCMAX[2:0]	The maximum ALC gain sets a limit to the amount of gain that the ALC can provide to the input signal. This protects small signals from excessive amplification.	
		Setting	**Maximum ALC Gain**
		000	−12 dB (default)
		001	−6 dB
		010	0 dB
		011	6 dB
		100	12 dB
		101	18 dB
		110	24 dB
		111	30 dB
[2:0]	ALCSEL[2:0]	ALC select. These bits set the channels that are controlled by the ALC. When set to right only, the ALC responds only to the right channel input and controls the gain of the right PGA amplifier only. When set to left only, the ALC responds only to the left channel input and controls the gain of the left PGA amplifier only. When set to stereo, the ALC responds to the greater of the left or right channel and controls the gain of both the left and right PGA amplifiers. DSP control allows the PGA gain to be set within the DSP or from external GPIO inputs. These bits must be off if manual control of the volume is desired.	
		Setting	**Channels**
		000	Off (default)
		001	Right only
		010	Left only
		011	Stereo
		100	DSP control
		101	Reserved
		110	Reserved
		111	Reserved

R27: Playback L/R Mixer Right (Mixer 6) Line Output Control, 16,417 (0x4021)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			MX6G4[1:0]		MX6G3[1:0]		MX6EN

Table 59. Playback L/R Mixer Right (Mixer 6) Line Output Control Register

Bits	Bit Name	Description	
[4:3]	MX6G4[1:0]	Mixer input gain boost. The signal from the right channel playback mixer (Mixer 4) can be enabled and boosted in the playback L/R mixer right (Mixer 6).	
		Setting	**Gain Boost**
		00	Mute (default)
		01	0 dB output (−6 dB gain on each of the two inputs)
		10	6 dB output (0 dB gain on each of the two inputs)
		11	Reserved
[2:1]	MX6G3[1:0]	Mixer input gain boost. The signal from the left channel playback mixer (Mixer 3) can be enabled and boosted in the playback L/R mixer right (Mixer 6).	
		Setting	**Gain Boost**
		00	Mute (default)
		01	0 dB output (−6 dB gain on each of the two inputs)
		10	6 dB output (0 dB gain on each of the two inputs)
		11	Reserved
0	MX6EN	Mixer 6 enable. 0 = disabled (default). 1 = enabled.	

R28: Playback L/R Mixer Mono Output (Mixer 7) Control, 16,418 (0x4022)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					MX7[1:0]		MX7EN

Table 60. Playback L/R Mixer Mono Output (Mixer 7) Control Register

Bits	Bit Name	Description	
[2:1]	MX7[1:0]	L/R mono playback mixer (Mixer 7). Mixes the left and right playback mixers (Mixer 3 and Mixer 4) with either a 0 dB or 6 dB gain boost. Additionally, this mixer can operate as a common-mode output, which is used as the virtual ground in a capless headphone configuration.	
		Setting	**Gain Boost**
		00	Common-mode output (default)
		01	0 dB output (−6 dB gain on each of the two inputs)
		10	6 dB output (0 dB gain on each of the two inputs)
		11	Reserved
0	MX7EN	Mixer 7 enable. 0 = disabled (default). 1 = enabled.	

R33: Playback Mono Output Control, 16,423 (0x4027)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MONOVOL[5:0]						MONOM	MOMODE

Table 65. Playback Mono Output Control Register

Bits	Bit Name	Description	
[7:2]	MONOVOL[5:0]	Mono output volume control. Each 1-bit step corresponds to a 1 dB increase in volume. If MX7[1:0] in Register R28 is set for common-mode output, volume control is disabled. See Table 93 for a complete list of the volume settings.	
		Setting	**Volume**
		000000	−57 dB (default)
		…	…
		111001	0 dB
		…	…
		111111	6 dB
1	MONOM	Mono output mute (active low). 0 = mute. 1 = unmute (default).	
0	MOMODE	Headphone mode enable. If MX7[1:0] in Register R28 is set for common-mode output for a capless headphone configuration, this bit should be set to 1 (headphone output). 0 = line output (default). 1 = headphone output.	

R34: Playback Pop/Click Suppression, 16,424 (0x4028)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved							

R38: DAC Control 2, 16,428 (0x402C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDAVOL[7:0]							

Table 70. DAC Control 2 Register

Bits	Bit Name	Description	
[7:0]	RDAVOL[7:0]	Controls the digital volume attenuation for right channel inputs from the right DAC. Each bit corresponds to a 0.375 dB step with slewing between settings. See Table 92 for a complete list of the volume settings.	
		Setting	**Volume Attenuation**
		00000000	0 dB (default)
		00000001	−0.375 dB
		00000010	−0.75 dB
		…	…
		11111110	−95.25 dB
		11111111	−95.625 dB

R39: Serial Port Pad Control, 16,429 (0x402D)

The optional pull-up/pull-down resistors are nominally 250 kΩ. When enabled, these pull-up/pull-down resistors set the serial port signals to a defined state when the signal source becomes three-state.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCSDP[1:0]		DACSDP[1:0]		LRCLKP[1:0]		BCLKP[1:0]	

Table 71. Serial Port Pad Control Register

Bits	Bit Name	Description	
[7:6]	ADCSDP[1:0]	ADC_SDATA pad pull-up/pull-down configuration.	
		Setting	**Configuration**
		00	Pull-up
		01	Reserved
		10	None (default)
		11	Pull-down
[5:4]	DACSDP[1:0]	DAC_SDATA pad pull-up/pull-down configuration.	
		Setting	**Configuration**
		00	Pull-up
		01	Reserved
		10	None (default)
		11	Pull-down
[3:2]	LRCLKP[1:0]	LRCLK pad pull-up/pull-down configuration.	
		Setting	**Configuration**
		00	Pull-up
		01	Reserved
		10	None (default)
		11	Pull-down
[1:0]	BCLKP[1:0]	BCLK pad pull-up/pull-down configuration.	
		Setting	**Configuration**
		00	Pull-up
		01	Reserved
		10	None (default)
		11	Pull-down

R42: Jack Detect Pin Control, 16,433 (0x4031)

With IOVDD set to 3.3 V, the low and high drive strengths of the JACKDET/MICIN pin are approximately 2.0 mA and 4.0 mA, respectively. The optional pull-up/pull-down resistors are nominally 250 kΩ. When enabled, these pull-up/pull-down resistors set the input si