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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30280fathp-u3

Table 1.2 Performance Overview of M16C/28 Group (64-Pin Package)

Item		Performance
CPU	Number of basic instructions	91 instructions
	Shortest instruction excution time	50 ns (f(BCLK)= 20MHz, VCC= 3.0 to 5.5V) (T-ver.) 50 ns (f(BCLK)= 20MHz, VCC= 4.2 to 5.5V, -40 to 105°C) (V-ver.) 62.5 ns (f(BCLK)= 16MHz, VCC= 4.2 to 5.5V, -40 to 125°C) (V-ver.)
	Operation mode	Single chip mode
	Address space	1 Mbytes
	Memory capacity	ROM/RAM : See **Table 1.3** and **Table 1.4**
Peripheral Function	port	Input/Output : 55 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous serial I/O, I^2C bus, or IEbus(1)) 1 channel (Clock synchronous serial I/O) 1 channel (Multi-Master I^2C bus)
	A/D converter	10 bits x 16 channels
	DMAC	2 channels
	CRC calculation circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	24 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock, • Sub-clock (These circuits contain a built-in feedback resistor) • On-chip oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer
	Oscillation Stop Detect Function	Main clock oscillation stop, re-oscillation detect function
	Voltage detection circuit	Not available
Electrical Characteristics	Power supply voltage	VCC=3.0 to 5.5V (T-ver.) VCC=4.2 to 5.5V (V-ver.)
	Power consumption	18mA (VCC=5V, f(BCLK)=20MHz) 25 µA (VCC=5V, f(BCLK)=f(XCIN)=32kHz on RAM) 3 µA (VCC=5V, f(BCLK)=f(XCIN)=32kHz, in wait mode) 0.8 µA (VCC=5V, in stop mode)
Flash Memory	Program/erase voltage	3.0V to 5.5V (T-ver.) 4.2V to 5.5V (V-ver.)
	Number of program/erase	100 times (all space) or 1,000 times (blocks 0 to 4)/ 10,000 times (blocks A and B(2))
Operating Ambient Temperature		-40 to 85°C (T-ver.), -40 to 125°C (V-ver.)
Package		64-pin plastic mold LQFP

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. Refer to **Table 1.5** and **Table 1.6** for number of program/erase endurance and ambient temperature.

Table 4.6 SFR Information(6)(1)

Address	Register	Symbol	After Reset
0380₁₆	Count start flag	TABSR	00₁₆
0381₁₆	Clock prescaler reset flag	CPSRF	0XXXXXXX₂
0382₁₆	One-shot start flag	ONSF	00₁₆
0383₁₆	Trigger select register	TRGSR	00₁₆
0384₁₆	Up-dowm flag	UDF	00₁₆
0385₁₆			
0386₁₆ 0387₁₆	Timer A0 register	TA0	XX₁₆ XX₁₆
0388₁₆ 0389₁₆	Timer A1 register	TA1	XX₁₆ XX₁₆
038A₁₆ 038B₁₆	Timer A2 register	TA2	XX₁₆ XX₁₆
038C₁₆ 038D₁₆	Timer A3 register	TA3	XX₁₆ XX₁₆
038E₁₆ 038F₁₆	Timer A4 register	TA4	XX₁₆ XX₁₆
0390₁₆ 0391₁₆	Timer B0 register	TB0	XX₁₆ XX₁₆
0392₁₆ 0393₁₆	Timer B1 register	TB1	XX₁₆ XX₁₆
0394₁₆ 0395₁₆	Timer B2 register	TB2	XX₁₆ XX₁₆
0396₁₆	Timer A0 mode register	TA0MR	00₁₆
0397₁₆	Timer A1 mode register	TA1MR	00₁₆
0398₁₆	Timer A2 mode register	TA2MR	00₁₆
0399₁₆	Timer A3 mode register	TA3MR	00₁₆
039A₁₆	Timer A4 mode register	TA4MR	00₁₆
039B₁₆	Timer B0 mode register	TB0MR	00XX0000₂
039C₁₆	Timer B1 mode register	TB1MR	00XX0000₂
039D₁₆	Timer B2 mode register	TB2MR	00XX0000₂
039E₁₆	Timer B2 special mode register	TB2SC	X0000000₂
039F₁₆			
03A0₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
03A1₁₆	UART0 bit rate register	U0BRG	XX₁₆
03A2₁₆ 03A3₁₆	UART0 transmit buffer register	U0TB	XX₁₆ XX₁₆
03A4₁₆	UART0 transmit/receive control register 0	U0C0	00001000₂
03A5₁₆	UART0 transmit/receive control register 1	U0C1	00000010₂
03A6₁₆ 03A7₁₆	UART0 receive buffer register	U0RB	XX₁₆ XX₁₆
03A8₁₆	UART1 transmit/receive mode register	U1MR	00₁₆
03A9₁₆	UART1 bit rate register	U1BRG	XX₁₆
03AA₁₆ 03AB₁₆	UART1 transmit buffer register	U1TB	XX₁₆ XX₁₆
03AC₁₆	UART1 transmit/receive control register 0	U1C0	00001000₂
03AD₁₆	UART1 transmit/receive control register 1	U1C1	00000010₂
03AE₁₆ 03AF₁₆	UART1 receive buffer register	U1RB	XX₁₆ XX₁₆
03B0₁₆	UART transmit/receive control register 2	UCON	X0000000₂
03B1₁₆			
03B2₁₆			
03B3₁₆			
03B4₁₆ 03B5₁₆	SFR snoop address register	CRCSAR	XX₁₆ 00XXXXXX₂
03B6₁₆	CRC mode register	CRCMR	0XXXXXX0₂
03B7₁₆			
03B8₁₆	DMA0 request cause select register	DM0SL	00₁₆
03B9₁₆			
03BA₁₆	DMA1 request cause select register	DM1SL	00₁₆
03BB₁₆			
03BC₁₆ 03BD₁₆	CRC data register	CRCD	XX₁₆ XX₁₆
03BE₁₆	CRC input register	CRCIN	XX₁₆
03BF₁₆			

NOTE:
1. The blank areas are reserved and cannot be used by users.

X : Undefined

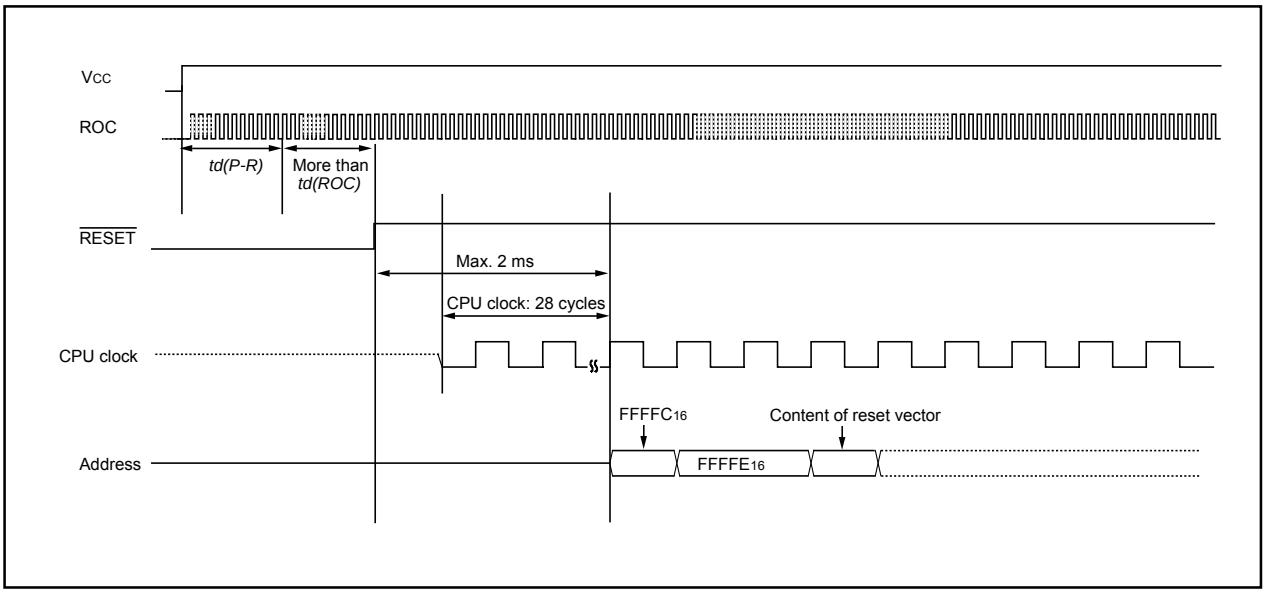


Figure 5.2 Reset Sequence

Table 5.1 Pin Status When $\overline{\text{RESET}}$ Pin Level is "L"

Pin Name	Status
P0 to P3, P6 to P10	Input port (high impedance)

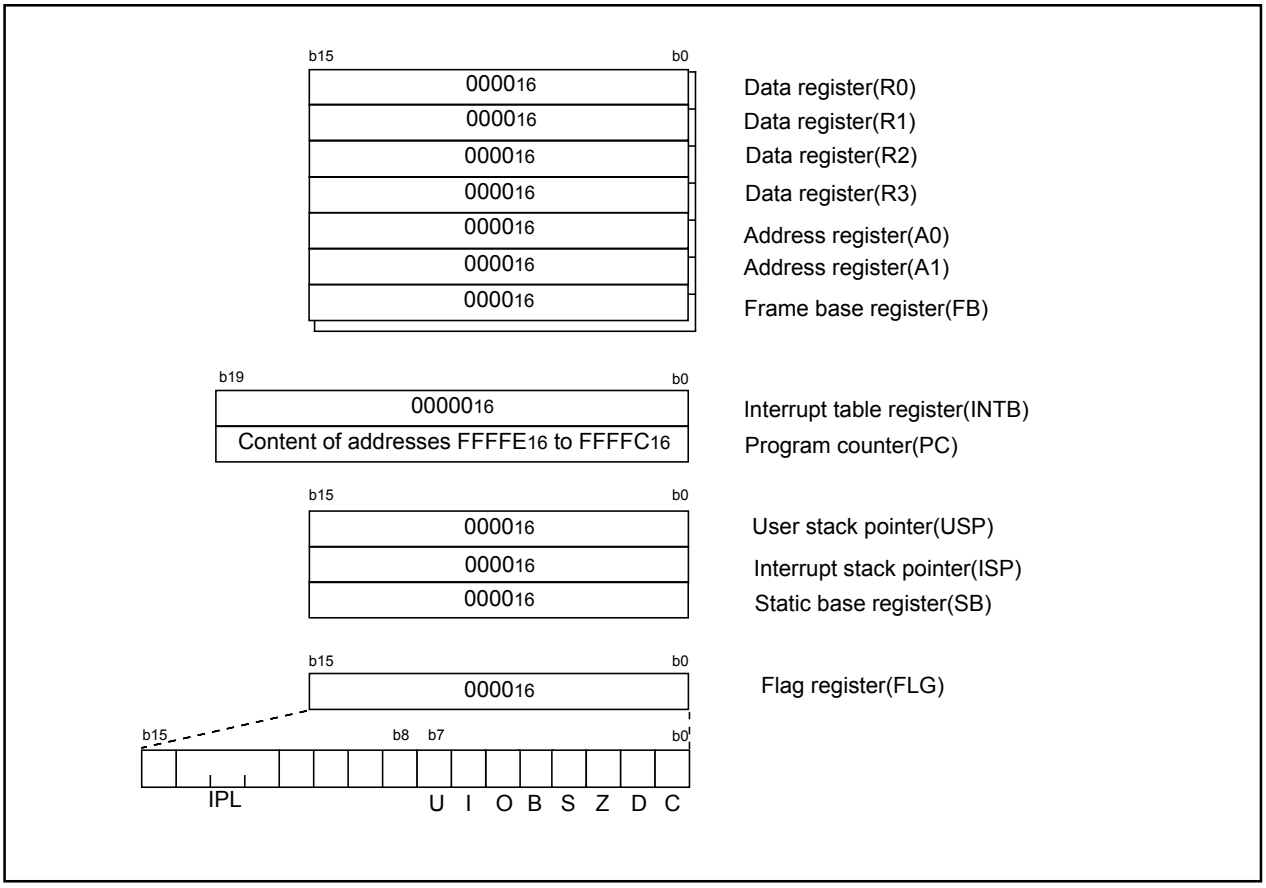


Figure 5.3 CPU Register Status After Reset

7.8.3 How to Use Oscillation Stop and Re-oscillation Detect Function

- The oscillation stop and re-oscillation detect interrupt shares the vector with the watchdog timer interrupt. If the oscillation stop, re-oscillation detection and watchdog timer interrupts both are used, read the CM22 bit in an interrupt routine to determine which interrupt source is requesting the interrupt.
- Where the main clock re-oscillated after oscillation stop, return the main clock to the CPU clock and peripheral function clock source by program. **Figure 7.13** shows the procedure for switching the clock source from the on-chip oscillator to the main clock.
- Simultaneously with oscillation stop, re-oscillation detection interrupt occurrence, the CM22 bit becomes 1. When the CM22 bit is set at 1, oscillation stop, re-oscillation detection interrupt are disabled. By setting the CM22 bit to 0 by program, oscillation stop, re-oscillation detection interrupt are enabled.
- If the main clock stops during low speed mode where the CM20 bit is 1, an oscillation stop, re-oscillation detection interrupt request is generated. At the same time, the on-chip oscillator starts oscillating. In this case, although the CPU clock is derived from the sub clock as it was before the interrupt occurred, the peripheral function clocks now are derived from the on-chip oscillator clock.
- To enter wait mode while using the oscillation stop, re-oscillation detection function, set the CM02 bit to 0 (peripheral function clocks not turned off during wait mode).
- Since the oscillation stop, re-oscillation detection function is provided in preparation for main clock stop due to external factors, set the CM20 bit to 0 (Oscillation stop, re-oscillation detection function disabled) where the main clock is stopped or oscillated by program, that is where the stop mode is selected or the CM05 bit is altered.
- This function cannot be used if the main clock frequency is 2 MHz or less. In that case, set the CM20 bit to 0.

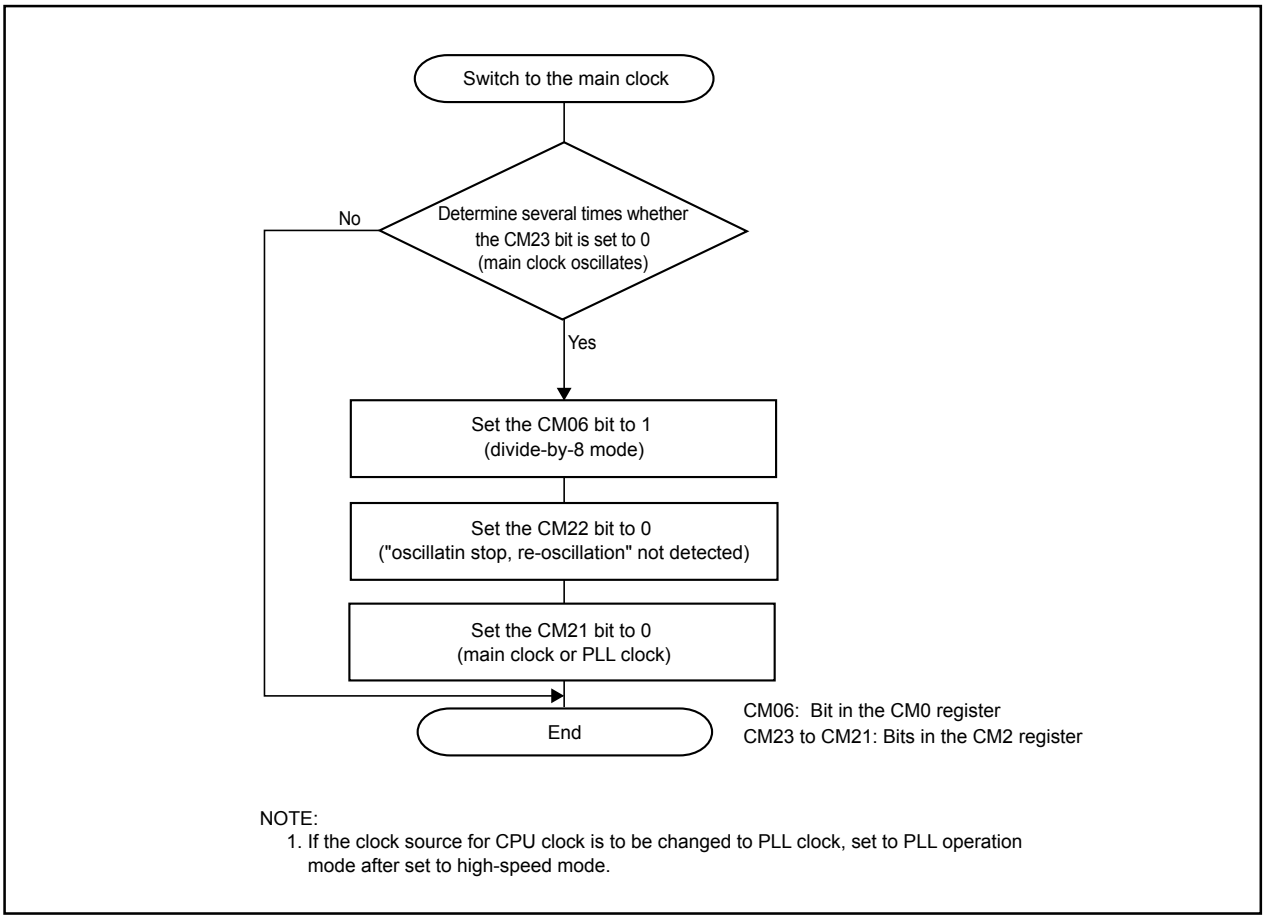
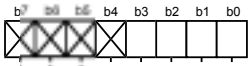


Figure 7.13 Procedure to Switch Clock Source From On-chip Oscillator to Main Clock

Interrupt Control Register(2)

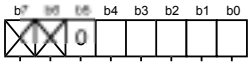
Symbol	Address	After Reset
ICOC0IC	0045₁₆	XXXXX000₂
ICOC1IC, IICIC(3)	0046₁₆	XXXXX000₂
BTIC, SCLDAIC(3)	0047₁₆	XXXXX000₂
BCNIC	004A₁₆	XXXXX000₂
DM0IC, DM1IC	004B₁₆, 004C₁₆	XXXXX000₂
ADIC, KUPIC(3)	004E₁₆	XXXXX000₂
S0TIC to S2TIC	0051₁₆, 0053₁₆, 004F₁₆	XXXXX000₂
S0RIC to S2RIC	0052₁₆, 0054₁₆, 0050₁₆	XXXXX000₂
TA0IC to TA4IC	0055₁₆ to 0059₁₆	XXXXX000₂
TB0IC to TB2IC	005A₁₆ to 005C₁₆	XXXXX000₂



Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0: Interrupt not requested 1: Interrupt requested	RW(1)
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the contents are undefined		—

NOTES:
1. This bit can only be reset by writing 0 (Do not write 1).
2. To rewrite the interrupt control registers, do so at a point that does not generate the interrupt request for that register. For details, refer to **21. 4 Interrupts**.
3. Use the IFSR2A register to select.

Symbol	Address	After Reset
INT3IC	0044₁₆	XX00X000₂
S4IC, INT5IC	0048₁₆	XX00X000₂
S3IC, INT4IC	0049₁₆	XX00X000₂
INT0IC to INT2IC	005D₁₆ to 005F₁₆	XX00X000₂



Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0 : Level 0 (interrupt disabled) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0: Interrupt not requested 1: Interrupt requested	RW(1)
POL	Polarity select bit	0: Selects falling edge (3, 4) 1: Selects rising edge	RW
— (b5)	Reserved bit	Set to 0	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the contents are undefined		—

NOTES:
1. This bit can only be reset by writing 0 (Do not write 1).
2. To rewrite the interrupt control register, do so at a point that does not generate the interrupt request for that register. For details, refer to **21.4 Interrupts**.
3. If the IFSRi bit in the IFSR register (i = 0 to 5) is 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge).
4. Set the POL bit in register S3IC or S4IC to 0 (falling edge) when the IFSR6 bit in the IFSR register is set to 0 (SI/O3 selected) or IFSR7 bit in the IFSR register to 0 (SI/O4 selected), respectively.

Figure 9.3 Interrupt Control Registers

Timer B2 Register (1)

(b15) b7 (b8) b0 b7 b0

Symbol	Address	After Reset
TB2	0395$_{16}$-0394$_{16}$	Undefined

Function	Setting Range	RW
Divide the count source by n + 1 where n = set value. Timer A1, A2 and A4 are started at every occurrence of underflow.	0000$_{16}$ to FFFF$_{16}$	RW

NOTE:
1. Access the register by 16 bit units.

Trigger Select Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRGSR	0383$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
TA1TGL	Timer A1 event/trigger select bit	To use the V-phase output control circuit, set these bits to "01$_2$"(TB2 underflow).	RW
TA1TGH			RW
TA2TGL	Timer A2 event/trigger select bit	To use the W-phase output control circuit, set these bits to "01$_2$"(TB2 underflow).	RW
TA2TGH			RW
TA3TGL	Timer A3 event/trigger select bit	b5 b4 0 0 : Input on TA3$_{IN}$ is selected (1) 0 1 : TB2 is selected (2) 1 0 : TA2 is selected (2) 1 1 : TA4 is selected (2)	RW
TA3TGH			RW
TA4TGL	Timer A4 event/trigger select bit	To use the U-phase output control circuit, set these bits to "01$_2$"(TB2 underflow).	RW
TA4TGH			RW

NOTES:
1. Set the corresponding port direction bit to 0 (input mode).
2. Overflow or underflow.

Count Start Flag

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After reset
TABSR	0380$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
TA0S	Timer A0 count start flag	0 : Stops counting 1 : Starts counting	RW
TA1S	Timer A1 count start flag		RW
TA2S	Timer A2 count start flag		RW
TA3S	Timer A3 count start flag		RW
TA4S	Timer A4 count start flag		RW
TB0S	Timer B0 count start flag		RW
TB1S	Timer B1 count start flag		RW
TB2S	Timer B2 count start flag		RW

Figure 12.31 TB2 Register, TRGSR Register, and TABSR Register

15.1.2 Repeat mode

In repeat mode, analog voltage applied to a selected pin is repeatedly converted to a digital code. **Table 15.4** shows the repeat mode specifications. **Figure 15.8** shows the operation example in repeat mode. **Figure 15.9** shows the ADCON0 to ADCON2 registers in repeat mode.

Table 15.4 Repeat Mode Specifications

Item	Specification
Function	Bits CH2 to CH0 in the ADCON0 register and the ADGSEL1 to ADGSEL0 bits in the ADCON2 register select pins. Analog voltage applied to a selected pin is repeatedly converted to a digital code
A/D Conversion Start Condition	• When the TRG bit in the ADCON0 register is 0 (software trigger) Set the ADST bit in the ADCON0 register to 1 (A/D conversion started) • When the TRG bit in the ADCON0 register is 1 (hardware trigger) The $\overline{\text{ADTRG}}$ pin input changes state from “H” to “L” after setting the ADST bit to 1 (A/D conversion started)
A/D Conversion Stop Condition	Set the ADST bit to 0 (A/D conversion halted)
Interrupt Request Generation Timing	None generated
Analog Input Pin	Select one pin from AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, and $AN3_0$ to $AN3_2$
Readout of A/D Conversion Result	Readout one of the AD0 to AD7 registers that corresponds to the selected pin

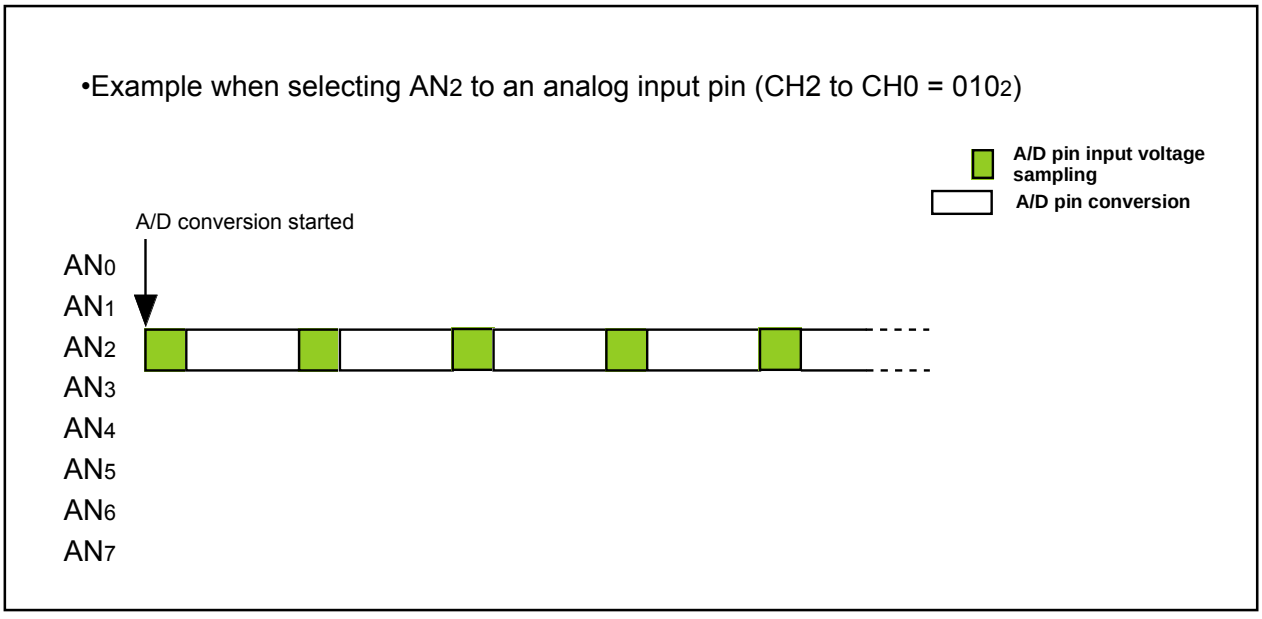


Figure 15.8 Operation Example in Repeat Mode

A/D Control Register 0 (1)

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
			1	1				ADCON0	03D6$_{16}$	00000XXX$_2$

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	Invalid in repeat sweep mode 0	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0	b4 b3 1 1: Repeat sweep mode 0 or repeat sweep mode 1	RW
MD1			RW
TRG	Trigger select bit	0: Software trigger 1: Hardware trigger ($\overline{\text{ADTRG}}$ trigger)	RW
ADST	A/D conversion start flag	0: A/D conversion disabled 1: A/D conversion started	RW
CKS0	Frequency select bit 0	See **Table 15.2**	RW

NOTE:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result will be undefined.

A/D Control Register 1 (1)

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
X	X	1			0			ADCON1	03D7$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D sweep pin select bit (2)	When repeat sweep mode 0 is selected, b1 b0 0 0: AN0 to AN1 (2 pins) 0 1: AN0 to AN3 (4 pins) 1 0: AN0 to AN5 (6 pins) 1 1: AN0 to AN7 (8 pins)	RW
SCAN1			RW
MD2	A/D operation mode select bit 1	0: Other than repeat sweep mode 1	RW
BITS	8/10-bit mode select bit	0: 8-bit mode 1: 10-bit mode	RW
CKS1	Frequency select bit 1	See **Table 15.2**	RW
VCUT	Vref connect Bit (3)	1: Vref connected	RW
$\overline{\text{(b7-b6)}}$	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result will be undefined.
2. AN00 to AN07, AN20 to AN27, and AN30 to AN32 can be used in the same way as AN0 to AN7. Use bits ADGSEL1 and ADGSEL 0 in the ADCON2 register to select the desired pin.
3. If the VCUT bit is reset from 0 (Vref unconnected) to 1 (Vref connected), wait for 1 µs or more before starting A/D conversion.

A/D Control Register 2(1)

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
X	X	0		0				ADCON2	03D4$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
SMP	A/D conversion method select bit	0: Without sample and hold 1: With sample and hold	RW
ADGSEL0	A/D input group select bit	b2 b1 0 0: Select port P10 group 0 1: Select port P9 group 1 0: Select port P0 group 1 1: Select port P1/P9 group	RW
ADGSEL1			RW
$\overline{\text{(b3)}}$	Reserved bit	Set to 0	RW
CKS2	Frequency select bit 2	See **Table 15.2**	RW
TRG1	Trigger select bit	Set to 0 in repeat sweep mode 0	RW
$\overline{\text{(b7-b6)}}$	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTE:
1. If the ADCON2 register is rewritten during A/D conversion, the conversion result will be undefined.

Figure 15.13 ADCON0 to ADCON2 Registers in Repeat Sweep Mode 0

I2C0 Start/stop Condition Control Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
S2D0	02E516	000110102

Bit Symbol	Bit Name	Function	RW
SSC0	START/STOP condition setting bits(1)	Setting for detection condition of START/STOP condition. See **Table 16.2**	RW
SSC1			RW
SSC2			RW
SSC3			RW
SSC4			RW
SIP	SCL/SDA interrupt pin polarity select bit	0: Active in falling edge 1: Active in rising edge	RW
SIS	SCL/SDA interrupt pin select bit	0: SDA enabled 1: SCL enabled	RW
STSPSEL	START/STOP condition generation select bit	0: Short setup/hold time mode 1: Long setup/hold time mode	RW

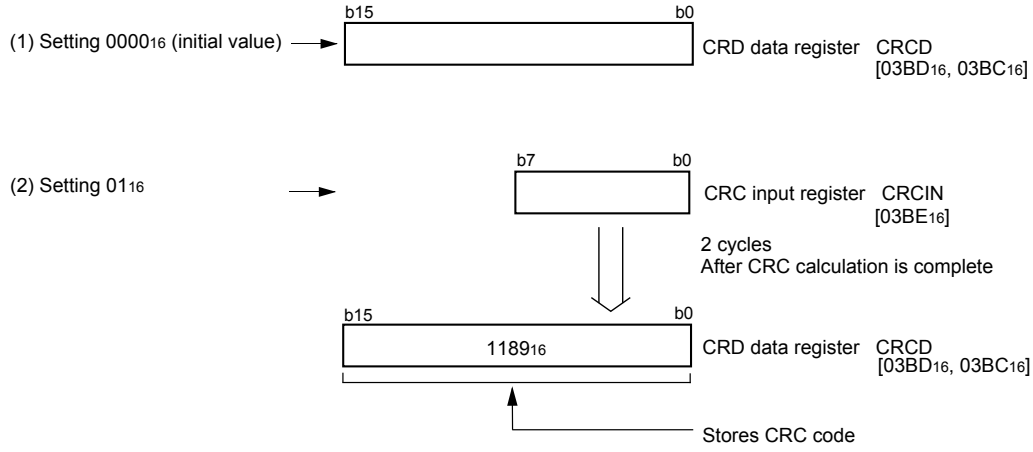
NOTE:
1. Do not set 000002 or odd values.

Figure 16.8 S2D0 Register

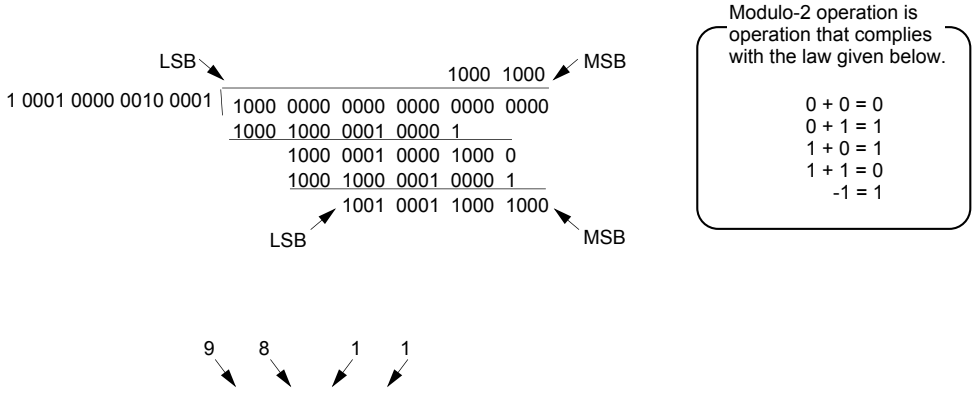
Table 16.2 Recommended setting (SSC4-SSC0) start/stop condition at each oscillation frequency

Oscillation f1 (MHz)	I2C bus system clock select	I2C bus system clock(MHz)	SSC4-SSC0(1)	SCL release time (cycle)	Setup time (cycle)	Hold time (cycle)
10	1 / 2f1(2)	5	XXX11110	6.2 µs (31)	3.2 µs (16)	3.0 µs (15)
8	1 / 2f1(2)	4	XXX11010	6.75 µs(27)	3.5 µs (14)	3.25 µs(13)
			XXX11000	6.25 µs(25)	3.25 µs (13)	3.0 µs (12)
8	1 / 8f1(2)	1	XXX00100	5.0 µs (5)	3.0 µs (3)	2.0 µs (2)
4	1 / 2f1(2)	2	XXX01100	6.5 µs (13)	3.5 µs (7)	3.0 µs (6)
			XXX01010	5.5 µs (11)	3.0 µs (6)	2.5 µs (5)
2	1 / 2f1(2)	1	XXX00100	5.0 µs (5)	3.0 µs (3)	2.0 µs (2)

NOTES:
1. Do not set odd values or 000002 to START/STOP condition setting bits (SSC4 to SSC0)
2. When the PCLK0 bit in the PCLKR register is set to 1.



The code resulting from sending 01_{16} in LSB first mode is (10000 0000).This the CRC code in the generating polynomial, $(X^{16} + X^{12} + X^5 + 1)$, becomes the remainder resulting from dividing (1000 0000)X^{16} by (1 0001 0000 0010 0001) in conformity with the modulo-2 operation.



Thus the CRC code becomes (1001 0001 1000 1000). Since the operation is in LSB first mode, the (1001 0001 1000 1000) corresponds to 1189_{16} in hexadecimal notation. If the CRC operation in MSB first mode is necessary, set the CRC mode selection bit to 1. CRC data register stores CRC code for MSB first mode.

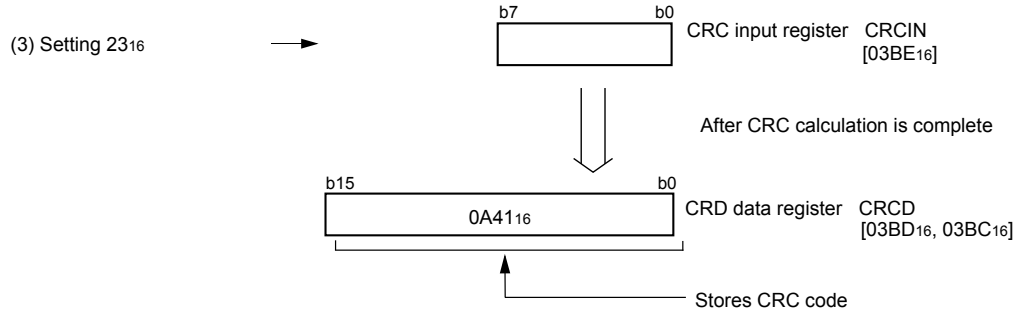
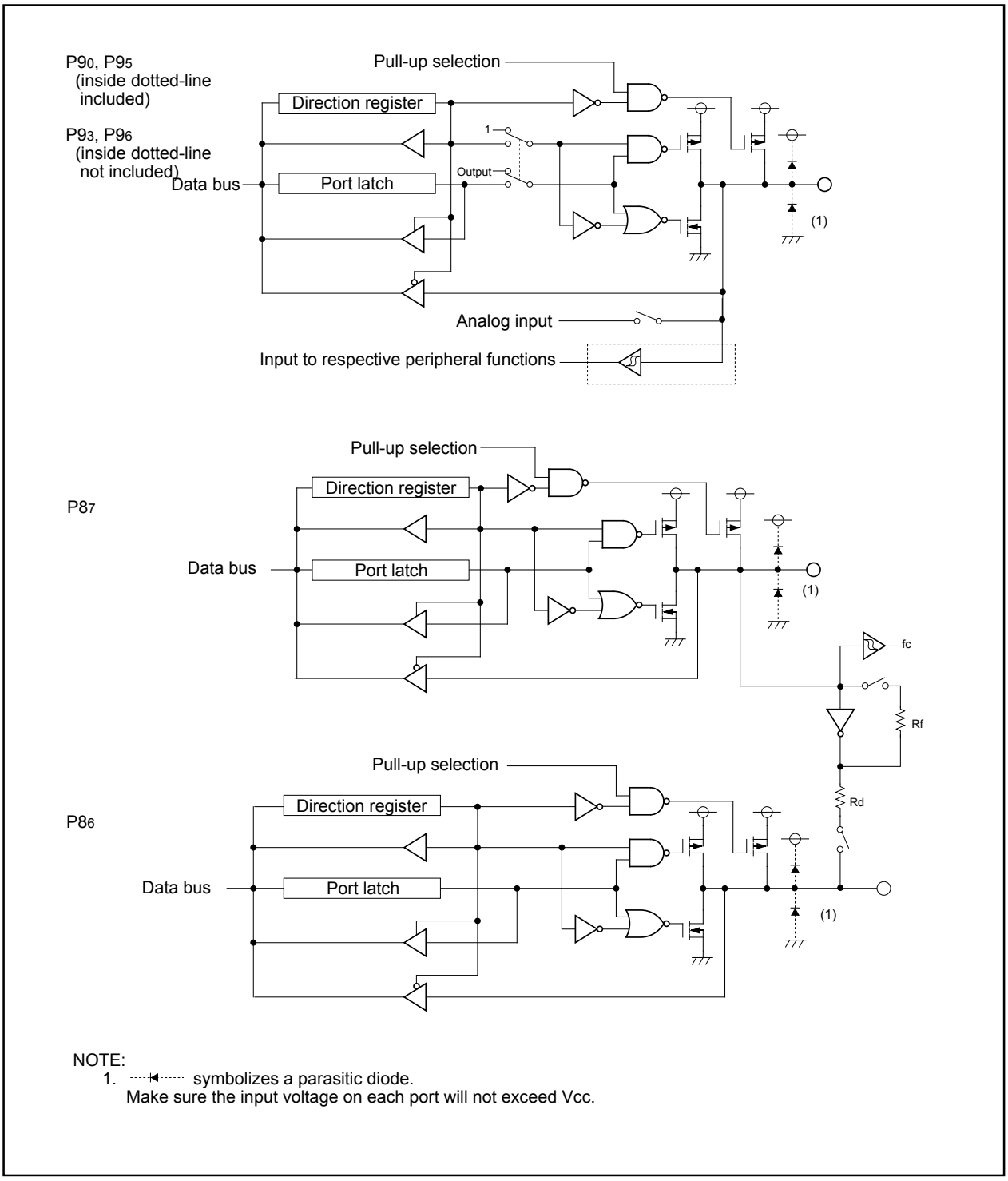


Figure 17.3 CRC Calculation



NOTE:
1. ⋯◂⋯ symbolizes a parasitic diode.
Make sure the input voltage on each port will not exceed Vcc.

Figure 18.4 I/O Ports (4)

19.2 Memory Map

The flash memory contains the user ROM area and the boot ROM area (reserved area). **Figures 19.1** and **19.2** show a block diagram of the flash memory. The user ROM area has space to store the MCU operation program in single-chip mode and two 2-Kbyte spaces: the block A and B.

The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite, standard serial input/output, or parallel input/output mode.

However, to rewrite program in block 0 and 1 in CPU rewrite mode, set the FMR02 bit in the FMR0 register to 1 (block 0, 1 rewrite enabled) and the FMR16 bit in the FMR1 register to 1 (blocks 0 to 4 rewrite enabled). Also, to rewrite program in blocks 2 to 4 in CPU rewrite mode, set the FMR16 bit in the FMR1 register to 1 (blocks 0 to 4 rewrite enabled). When the PM10 bit in the PM1 register is set to 1 (data space access enabled), block A and B can be available for use.

The boot ROM area (4-byte) is a reserved area. This boot ROM area has a standard serial I/O mode control program stored before shipping. Do not rewrite the boot ROM area.

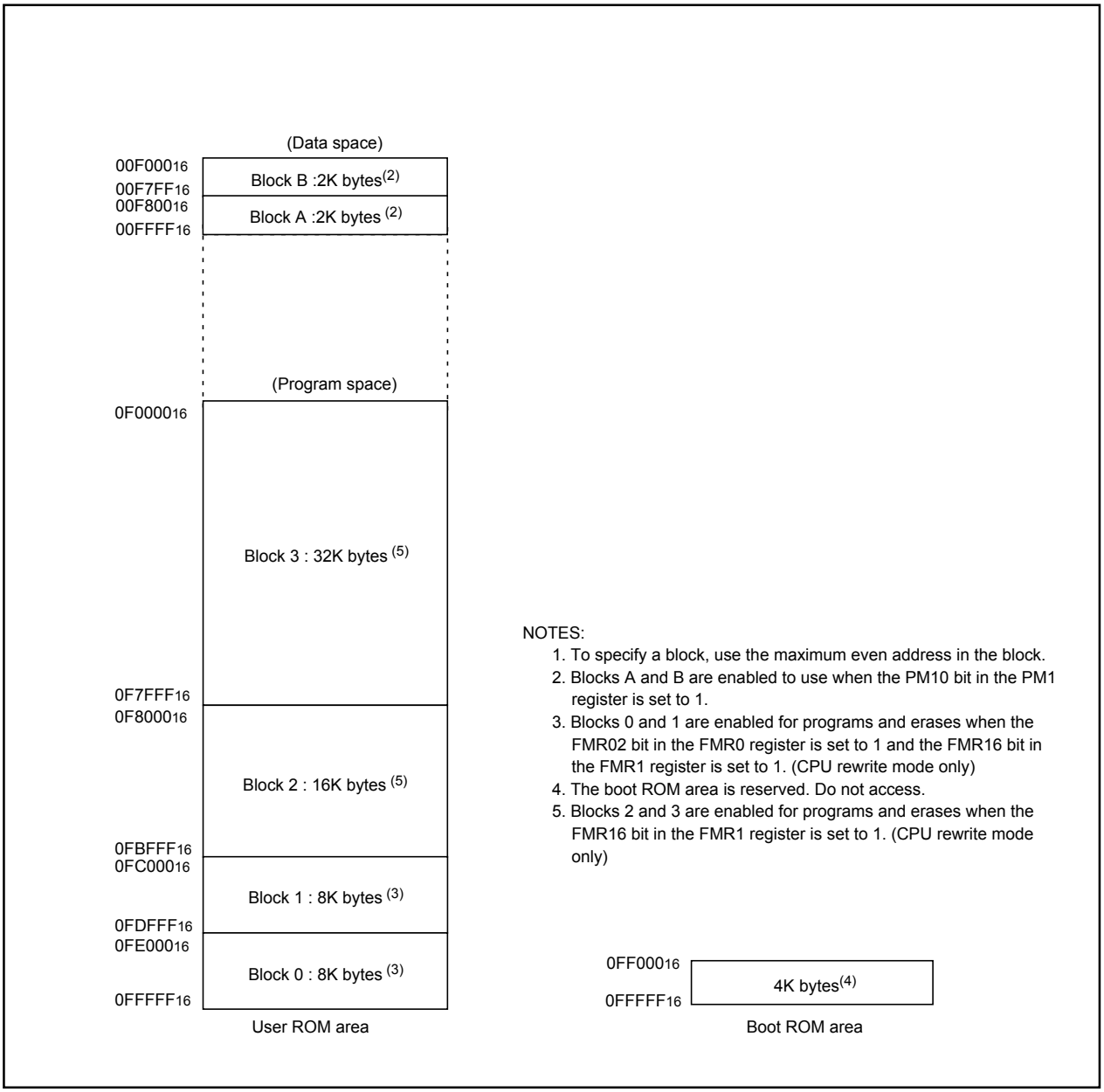


Figure 19.1 Flash Memory Block Diagram (ROM capacity 64 Kbytes)

Table 20.3 A/D Conversion Characteristics (1)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
-	Resolution		V_{REF} = V_{CC}			10	Bits
INL	Integral Nonlinearity Error	10 bit	V_{REF} = V_{CC} = 5 V			±3	LSB
			V_{REF} = V_{CC} = 3.3 V			±5	LSB
		8 bit	V_{REF} = V_{CC} = 3.3 V			±2	LSB
-	Absolute Accuracy	10 bit	V_{REF} = V_{CC} = 5 V			±3	LSB
			V_{REF} = V_{CC} = 3.3 V			±5	LSB
		8 bit	V_{REF} = V_{CC} = 3.3 V			±2	LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder		V_{REF} = V_{CC}	10		40	kΩ
t_{CONV}	10-bit Conversion Time Sample & Hold Function Available		V_{REF} = V_{CC} = 5 V, øAD = 10 MHz	3.3			µs
t_{CONV}	8-bit Conversion Time Sample & Hold Function Available		V_{REF} = V_{CC} = 5 V, øAD = 10 MHz	2.8			µs
V_{REF}	Reference Voltage			2.0		V_{CC}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Referenced to V_{CC} = AV_{CC} = V_{REF} = 3.3 to 5.5 V, V_{SS} = AV_{SS} = 0 V at Topr = -40 to 85° C unless otherwise specified.
2. Keep ϕAD frequency at 10 MHz or less. Additionally, divide the f_{AD} if V_{CC} is less than 4.2V, and make ϕAD frequency equal to or lower than f_{AD}/2.
3. When sample & hold function is disabled, keep ϕAD frequency at 250kHz or more in addition to the limitation in Note 2.
   When sample & hold function is enabled, keep ϕAD frequency at 1MHz or more in addition to the limitation in Note 2.
4. When sample & hold function is enabled, sampling time is 3/ ϕAD frequency.
   When sample & hold function is disabled, sampling time is 2/ ϕAD frequency.

V_{CC} = 5V

Table 20.7 Electrical Characteristics (1)

Symbol	Parameter			Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		I_{OH}=-5mA	V_{CC}-2.0		V_{CC}	V
V_{OH}	Output High ("H") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		I_{OH}=-200µA	V_{CC}-0.3		V_{CC}	V
V_{OH}	Output High ("H") Voltage	X_{OUT}	High Power	I_{OH}=-1mA	V_{CC}-2.0		V_{CC}	V
			Low Power	I_{OH}=-0.5mA	V_{CC}-2.0		V_{CC}	
	Output High ("H") Voltage	X_{COUT}	High Power	No load applied		2.5		V
			Low Power	No load applied		1.6		
V_{OL}	Output Low ("L") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		I_{OL}=5mA			2.0	V
V_{OL}	Output Low ("L") Voltage	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		I_{OL}=200µA			0.45	V
V_{OL}	Output Low ("L") Voltage	X_{OUT}	High Power	I_{OL}=1mA			2.0	V
			Low Power	I_{OL}=0.5mA			2.0	
	Output Low ("L") Voltage	X_{COUT}	High Power	No load applied		0		V
			Low Power	No load applied		0		
V_{T+}-V_{T-}	Hysteresis	$TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB2_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS2}$, SCL, SDA, $CLK0$-$CLK2$, $TA2_{OUT}$-$TA4_{OUT}$, $\overline{KI0}$-$\overline{KI3}$, $RXD0$-$RXD2$, $SIN3$, $SIN4$			0.2		1.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$			0.2		2.5	V
V_{T+}-V_{T-}	Hysteresis	X_{IN}			0.2		0.8	V
I_{IH}	Input High ("H") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$ X_{IN}, $\overline{RESET}$, CNV_{SS}		V_I=5V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$ X_{IN}, $\overline{RESET}$, CNV_{SS}		V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ to $P3_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_3$, $P9_5$ to $P9_7$, $P10_0$ to $P10_7$		V_I=0V	30	50	170	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}				1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}				15		MΩ
V_{RAM}	RAM Standby Voltage			In stop mode	2.0			V

NOTE:

1. Referenced to V_{CC}=4.2 to 5.5V, V_{SS}=0V at Topr=-40 to 85 ° C, f(BCLK)=20MHz unless otherwise specified.

V_{CC} = 5V

Table 20.8 Electrical Characteristics (2) (1)

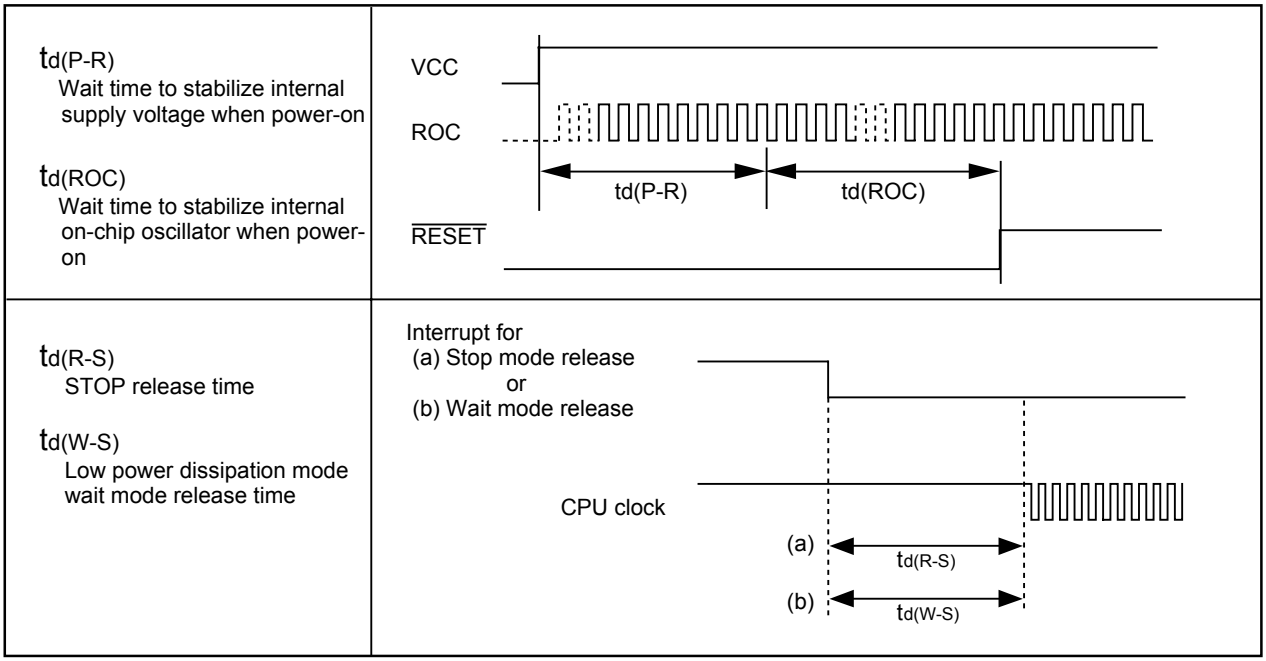
Symbol	Parameter	Measurement Condition			Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power Supply Current (V_{CC}=4.2 to 5.5V)	Output pins are left open and other pins are connected to V_{SS}	Mask ROM	f(BCLK) = 20 MHz, main clock, no division		18	25	mA
				On-chip oscillation $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz		2		mA
			Flash memory	f(BCLK) = 20 MHz, main clock, no division		18	25	mA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz		2		mA
			Flash memory program	f(BCLK) = 10 MHz, Vcc = 5.0 V		11		mA
			Flash memory erase	f(BCLK) = 10 MHz, Vcc = 5.0 V		11		mA
			Mask ROM	f(X_{CIN}) = 32 kHz, In low-power consumption mode, Program running on ROM(3)		25		µA
				On-chip oscillation $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz, In wait mode		50		µA
			Flash memory	f(BCLK) = 32 kHz, In low-power consumption mode, Program running on RAM(3)		25		µA
				f(BCLK) = 32kHz, In low-power consumption mode, Program running on flash memory(3)		450		µA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz, In wait mode		50		µA
			Mask ROM, Flash memory	f(BCLK) = 32 kHz, In wait mode(2), Oscillation capacity high		8.5		µA
				f(BCLK) = 32 kHz, In wait mode(2), Oscillation capacity low		3		µA
				While clock stops, Topr = 25° C		0.8	3	µA

NOTES:

1. Referenced to V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 85 ° C, f(BCLK) = 20 MHz unless otherwise specified.
2. With one timer operates, using f_{C32}.
3. This indicates the memory in which the program to be executed exists.

Table 20.44 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	V_{CC}=4.2 to 5.5V			2	ms
td(ROC)	Wait Time to Stabilize Internal On-chip Oscillator when Power-on				40	µs
td(S-R)	STOP Release Time				150	µs
td(W-S)	Low Power Dissipation Mode Wait Mode Release Time				150	µs



Vcc = 5V

Table 20.46 Electrical Characteristics (2) (1)

Symbol	Parameter	Measurement Condition			Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power Supply Current (V_{CC} = 4.2 to 5.5 V)	Output pins are left open and other pins are connected to V_{SS}	Mask ROM	f(BCLK) = 20 MHz, main clock, no division		18	25	mA
				On-chip oscillation $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz		2		mA
			Flash memory	f(BCLK) = 20 MHz, main clock, no division		18	25	mA
				f(BCLK) = 16 MHz, main clock, no division		14	20	mA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz		2		mA
			Flash memory program	f(BCLK) = 10 MHz, Vcc = 5.0 V		11		mA
			Flash memory erase	f(BCLK) = 10 MHz, Vcc = 5.0 V		11		mA
			Mask ROM	f(X_{CIN}) = 32 kHz, In low-power consumption mode, Program running on ROM(3)		25		µA
				On-chip oscillation $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz, In wait mode		50		µA
			Flash memory	f(BCLK) = 32 kHz, In low-power consumption mode, Program running on RAM(3)		25		µA
				f(BCLK) = 32 kHz, In low-power consumption mode, Program running on flash memory(3)		450		µA
				On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz, In wait mode		50		µA
			Mask ROM, Flash memory	f(BCLK) = 32 kHz, In wait mode(2), Oscillation capacity high		8.5		µA
				f(BCLK) = 32 kHz, In wait mode(2), Oscillation capacity low		3		µA
				While clock stops, Topr = 25° C		0.8	3	µA

NOTES:

1. Referenced to V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 105 ° C, f(BCLK) = 20 MHz / V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V at Topr = -40 to 125 ° C, f(BCLK) = 16 MHz, unless otherwise specified.
2. With one timer operates, using f_{C32}.
3. This indicates the memory in which the program to be executed exists.

21.14.14 Definition of Programming/Erasure Times

"Number of programs and erasure" refers to the number of erasure per block.
If the number of program and erasure is n (n=100 1,000 10,000) each block can be erased n times.
For example, if a 2K byte block A is erased after writing 1 word data 1024 times, each to a different address, this is counted as one program and erasure. However, data cannot be written to the same adrress more than once without erasing the block. (Rewrite prohibited)

21.14.15 Flash Memory Version Electrical Characteristics 10,000 E/W cycle product (U7)

When Block A or B E/W cycles exceed 100, set the FMR17 bit in the FMR1 register to 1 (1 wait) to select one wait state per block access for U7. When FMR17 is set to 1, one wait state is inserted per access to Block A or B - regardless of the value of PM17. Wait state insertion during access to all other blocks, as well as to internal RAM, is controlled by PM17 - regardless of the FMR17 bit setting.
To use the limited number of erasure efficiently, write to unused address within the block instead of rewite. Erase block only after all possible addresses are used. For example, an 8-word program can be written 128 times before erase becomes necessary.
Maintaining an equal number of erasure between Block A and B will also improve efficiency.
We recommend keeping track of the number of times erasure is used.

21.14.16 Boot Mode

An undefined value is sometimes output in the I/O port until the internal power supply becomes stable when "H" is applied to the CNVSS pin and "L" is applied to the $\overline{\text{RESET}}$ pin.
When setting the CNVSS pin to "H", the following procedure is required:

(1) Apply an "L" signal to the $\overline{\text{RESET}}$ pin and the CNVSS pin.
(2) Bring VCC to more than 2.7V, and wait at least 2msec. (Internal power supply stable waiting time)
(3) Apply an "H" signal to the CNVSS pin.
(4) Apply an "H" signal to the $\overline{\text{RESET}}$ pin.

When the CNVSS pin is “H” and RESET pin is “L”, P67 pin is connected to the pull-up resister.

Rev.	Date	Description	
		Page	Summary
		365	• **21.4.6 Rewrite the Interrupt Control Register** Example 1 modified
		371	• **21.6.3 Three-phase Motor Control Timer Function** newly added
		372	• **21.7.1 Rewrite the G1IR Register** Description modified
		373	• **21.7.4 IC/OC Base Timer Interrupt** Section newly added
		381	• **21.13.1 Internal ROM Area** partially added
		383	• **21.14.9 Interrupts EW Mode 1** Description about watchdog timer interrupt deleted • **21.14.10 How to Access** partially deleted • **21.14.13 Regarding Programming/Erasure Times and Execution Time** Description partially modified
		-	**Functional Comparison** • **Difference between M16C/28 Group and M16C/29 Group (Normal-ver.)** is deleted
		388	• **Appendix 2.1 Difference between M16C/28 Group Normal-ver. and m16C/28 Group T-ver./V-ver.** flash memory added