Renesas Electronics America Inc - M30281FATHP#U3AAC9 Datasheet

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Voltage - Supply (Vcc/Vdd)	-
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Oscillator Type	-
Operating Temperature	-
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Table 4.2 SFR Information(2)(1)

Address	Register	Symbol	After Reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆	INT3 interrupt control register	INT3IC	XX00X000₂
0045₁₆	IC/OC 0 interrupt control register	ICOC0IC	XXXXX000₂
0046₁₆	IC/OC 1 interrupt control register, I²C bus interface interrupt control register	ICOC1IC, IICIC	XXXXX000₂
0047₁₆	IC/OC base timer interrupt control register, SCLSDA interrupt control register	BTIC, SCLDAIC	XXXXX000₂
0048₁₆	SI/O4 interrupt control register, INT5 interrupt control register	S4IC, INT5IC	XX00X000₂
0049₁₆	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00X000₂
004A₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX000₂
004B₁₆	DMA0 interrupt control register	DM0IC	XXXXX000₂
004C₁₆	DMA1 interrupt control register	DM1IC	XXXXX000₂
004D₁₆	Key input interrupt control register	KUPIC	XXXXX000₂
004E₁₆	A/D conversion interrupt control register	ADIC	XXXXX000₂
004F₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX000₂
0050₁₆	UART2 receive interrupt control register	S2RIC	XXXXX000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000₂
0055₁₆	Timer A0 interrupt control register	TA0IC	XXXXX000₂
0056₁₆	Timer A1 interrupt control register	TA1IC	XXXXX000₂
0057₁₆	Timer A2 interrupt control register	TA2IC	XXXXX000₂
0058₁₆	Timer A3 interrupt control register	TA3IC	XXXXX000₂
0059₁₆	Timer A4 interrupt control register	TA4IC	XXXXX000₂
005A₁₆	Timer B0 interrupt control register	TB0IC	XXXXX000₂
005B₁₆	Timer B1 interrupt control register	TB1IC	XXXXX000₂
005C₁₆	Timer B2 interrupt control register	TB2IC	XXXXX000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00X000₂
005E₁₆	INT1 interrupt control register	INT1IC	XX00X000₂
005F₁₆	INT2 interrupt control register	INT2IC	XX00X000₂
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

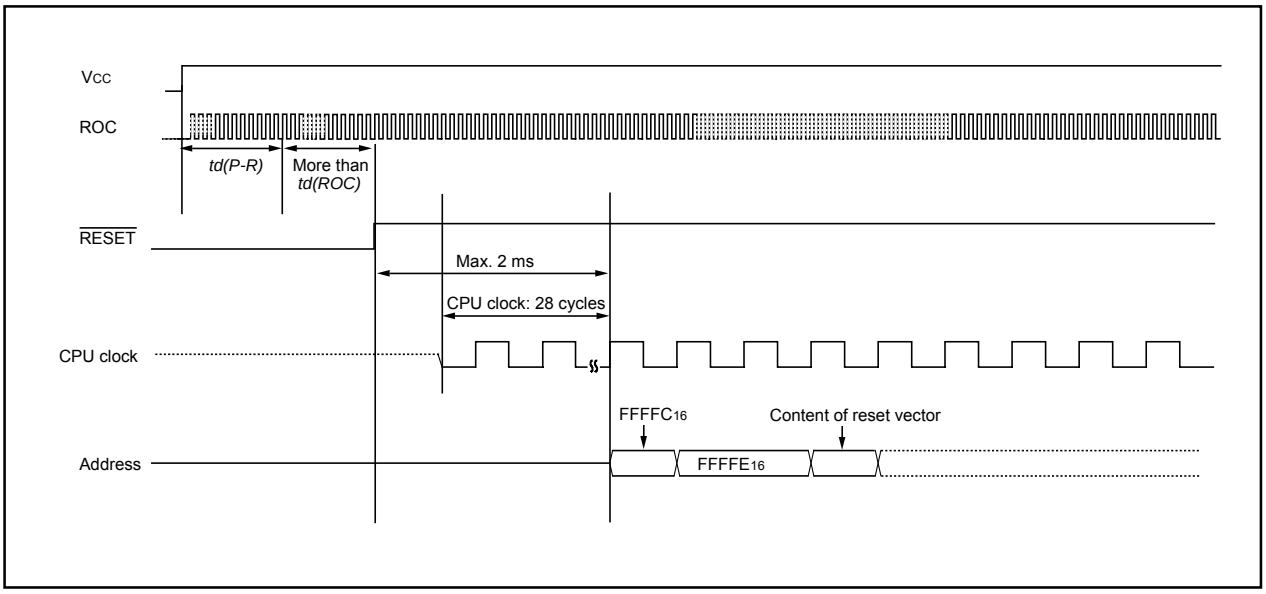


Figure 5.2 Reset Sequence

Table 5.1 Pin Status When $\overline{\text{RESET}}$ Pin Level is "L"

Pin Name	Status
P0 to P3, P6 to P10	Input port (high impedance)

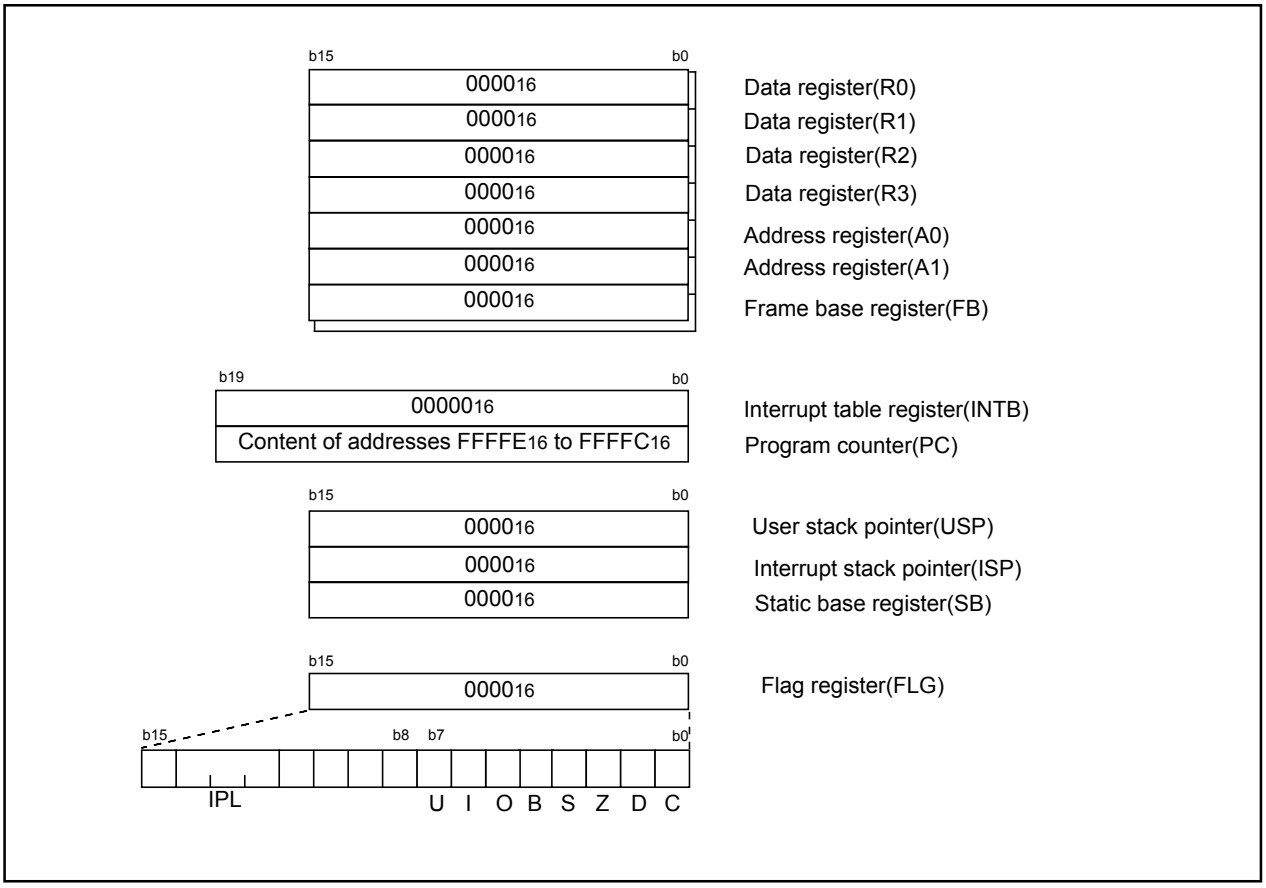


Figure 5.3 CPU Register Status After Reset

9.4 Interrupt Sequence

An interrupt sequence (the device behavior from the instant an interrupt is accepted to the instant the interrupt routine is executed) is described here.

If an interrupt occurs during execution of an instruction, the processor determines its priority when the execution of the instruction is completed, and transfers control to the interrupt sequence from the next cycle. If an interrupt occurs during execution of either the SMOVB, SMOVF, SSTR or RMPA instruction, the processor temporarily suspends the instruction being executed, and transfers control to the interrupt sequence.

The CPU behavior during the interrupt sequence is described below. **Figure 9.5** shows time required for executing the interrupt sequence.

(1) The CPU gets interrupt information (interrupt number and interrupt request priority level) by reading the address 0000_{16}. Then it clears the IR bit for the corresponding interrupt to 0 (interrupt not requested).

(2) The FLG register immediately before entering the interrupt sequence is saved to the CPU's internal temporary register(Note).

(3) The I, D and U flags in the FLG register become as follows:
The I flag is cleared to 0 (interrupts disabled).
The D flag is cleared to 0 (single-step interrupt disabled).
The U flag is cleared to 0 (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt Nos. 32 to 63 is executed.

(4) The CPU's internal temporary register(1) is saved to the stack.

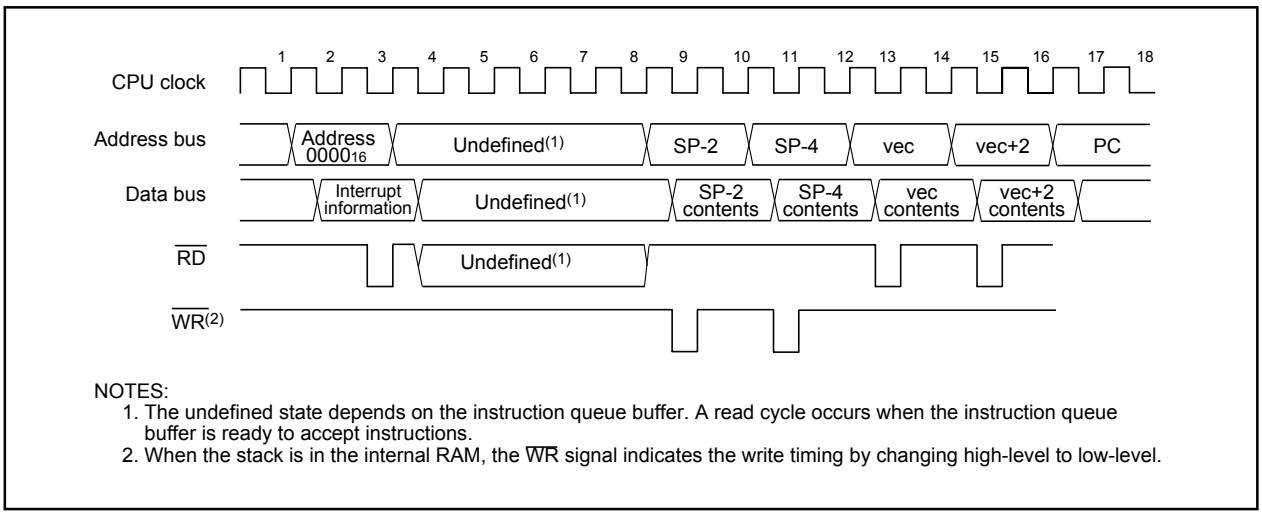
(5) The PC is saved to the stack.

(6) The interrupt priority level of the accepted interrupt is set in the IPL.

(7) The start address of the relevant interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, the processor resumes executing instructions from the start address of the interrupt routine.

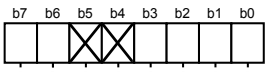
NOTE:
1. This register cannot be used by user.



NOTES:
1. The undefined state depends on the instruction queue buffer. A read cycle occurs when the instruction queue buffer is ready to accept instructions.
2. When the stack is in the internal RAM, the $\overline{WR}$ signal indicates the write timing by changing high-level to low-level.

Figure 9.5 Time Required for Executing Interrupt Sequence

DMA0 Request Cause Select Register



Symbol	Address	After Reset
DM0SL	03B8$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
DSEL0	DMA request cause select bit	Refer to note (1)	RW
DSEL1			RW
DSEL2			RW
DSEL3			RW
—— (b5-b4)	Nothing is assigned. When write, set to 0. When read, their content are 0		——
DMS	DMA request cause expansion select bit	0: Basic cause of request 1: Extended cause of request	RW
DSR	Software DMA request bit	A DMA request is generated by setting this bit to 1 when the DMS bit is 0 (basic cause) and bits DSEL3 to DSEL0 are 0001$_2$ (software trigger). The value of this bit when read is 0	RW

NOTE:
1. The causes of DMA0 requests can be selected by a combination of DMS bit and bits DSEL3 to DSEL0 in the manner described below.

DSEL3 to DSEL0	DMS=0(basic cause of request)	DMS=1(extended cause of request)
0 0 0 0$_2$	Falling edge of $\overline{\text{INT0}}$ pin	IC/OC base timer
0 0 0 1$_2$	Software trigger	–
0 0 1 0$_2$	Timer A0	IC/OC channel 0
0 0 1 1$_2$	Timer A1	IC/OC channel 1
0 1 0 0$_2$	Timer A2	–
0 1 0 1$_2$	Timer A3	–
0 1 1 0$_2$	Timer A4	Two edges of $\overline{\text{INT0}}$ pin
0 1 1 1$_2$	Timer B0	–
1 0 0 0$_2$	Timer B1	–
1 0 0 1$_2$	Timer B2	–
1 0 1 0$_2$	UART0 transmit	IC/OC channel 2
1 0 1 1$_2$	UART0 receive	IC/OC channel 3
1 1 0 0$_2$	UART2 transmit	IC/OC channel 4
1 1 0 1$_2$	UART2 receive	IC/OC channel 5
1 1 1 0$_2$	A/D conversion	IC/OC channel 6
1 1 1 1$_2$	UART1 transmit	IC/OC channel 7

Figure 11.2 DM0SL Register

Timer Bi Mode Register (i= 0 to 1)

b7	b6	b5	b4	b3	b2	b1	b0
						0	0

Symbol: TB0MR to TB1MR
Address: 039B16 to 039C16
After Reset: 00XX00002

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0: Timer mode or A/D trigger mode	RW
TMOD1			RW
MR0	Invalid in A/D trigger mode Either 0 or 1 is enabled		RW
MR1			RW
MR2	TB0MR register Set to 0 in A/D trigger mode		RW
	TB1MR register Nothing is assigned. If necessary, set to 0. When read, its content is undefined		—
MR3	When write in A/D trigger mode, set to 0. When read in A/D trigger mode, the content is undefined		RO
TCK0	Count source select bit (1)	b7 b6 0 0: f1 or f2 0 1: f8 1 0: f32 1 1: fC32	RW
TCK1			RW

NOTE:
1. When this bit is used in delayed trigger mode 0, set the same count source to the timer B0 and timer B1.

Figure 12.23 TBiMR Register in A/D Trigger Mode

Timer B2 special mode register (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	0	0		1	1		

Symbol: TB2SC
Address: 039E16
After Reset: X00000002

Bit Symbol	Bit Name	Function	RW
PWCON	Timer B2 reload timing switch bit (2)	0: Timer B2 underflow 1: Timer A output at odd-numbered	RW
IVPCR1	Three-phase output port $\overline{SD}$ control bit 1 (3, 4, 7)	0: Three-phase output forcible cutoff by $\overline{SD}$ pin input (high impedance) disabled 1: Three-phase output forcible cutoff by $\overline{SD}$ pin input (high impedance) enabled	RW
TB0EN	Timer B0 operation mode select bit	0: Other than A/D trigger mode 1: A/D trigger mode (5)	RW
TB1EN	Timer B1 operation mode select bit	0: Other than A/D trigger mode 1: A/D trigger mode (5)	RW
TB2SEL	Trigger select bit (6)	0: TB2 interrupt 1: Underflow of TB2 interrupt generation frequency setting counter [ICTB2]	RW
$\overline{\text{(b6-b5)}}$	Reserved bits	Set to 0	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, its content is 0		—

NOTES:
1. Write to this register after setting the PRC1 bit in the PRCR register to 1 (write enabled).
2. If the INV11 bit is 0 (three-phase mode 0) or the INV06 bit is 1 (triangular wave modulation mode), set this bit to 0 (timer B2 underflow).
3. When setting the IVPCR1 bit to 1 (three-phase output forcible cutoff by $\overline{SD}$ pin input enabled), set the PD8_5 bit to 0 (= input mode).
4. Related pins are U(P80), $\overline{U}$(P81), V(P72), $\overline{V}$(P73), W(P74), $\overline{W}$(P75). After forcible cutoff, input "H" to the P85/$\overline{NMI}$/$\overline{SD}$ pin. Set the IVPCR1 bit to 0, and this forcible cutoff will be reset. If "L" is input to the P85/$\overline{NMI}$/$\overline{SD}$ pin, a three-phase motor control timer output will be disabled (INV03=0). At this time, when the IVPCR1 bit is 0, the target pins changes to programmable I/O port. When the IVPCR1 bit is 1, the target pins changes to high-impedance state regardless of which functions of those pins are used.
5. When this bit is used in delayed trigger mode 0, set bits TB0EN and TB1EN to 1 (A/D trigger mode).
6. When setting the TB2SEL bit to 1 (underflow of TB2 interrupt generation frequency setting counter[ICTB2]), set the INV02 bit to 1 (three-phase motor control timer function).
7. Refer to "**18.6 Digital Debounce function**" for the $\overline{SD}$ input.

Figure 12.24 TB2SC Register in A/D Trigger Mode

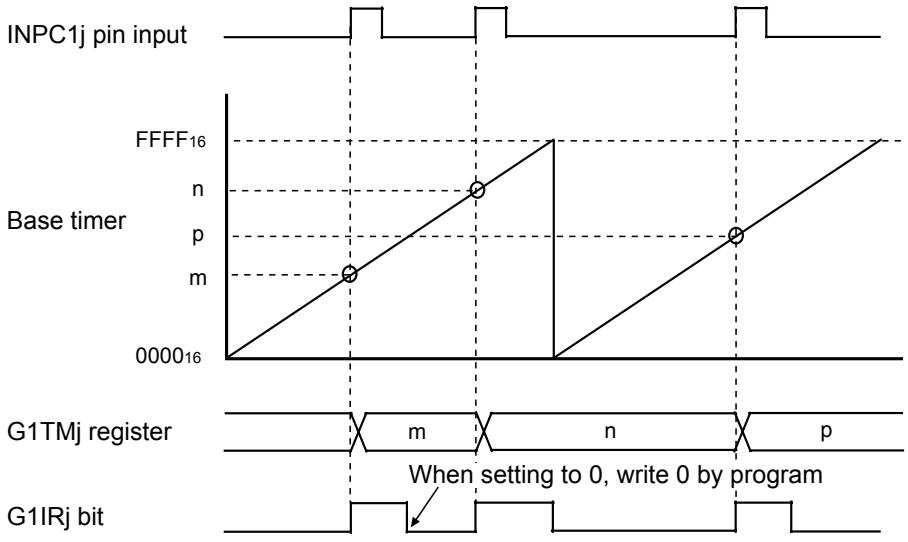
Table 13.6 Register Settings Associated with the Time Measurement Function

Register	Bit	Function
G1TMCRj	CTS1 to CTS0	Select time measurement trigger
	DF1 to DF0	Select the digital filter function
	GT, GOC, GSC	Select the gate function
	PR	Select the prescaler function
G1TPRk	-	Setting value of prescaler
G1FS	FSCj	Set to 1 (time measurement function)
G1FE	IFEj	Set to 1 (channel j function enabled)

j = 0 to 7 k = 6, 7

Bit configurations and function varys with channels used.

Registers associated with the time measurement function must be set after setting registers associated with the base timer.



j = 0 to 7
G1IRj bit: Bits in the G1IR register

The above applies to the following condition.

- Bits CTS1 to CTS0 in the G1TMCRj registers are set to 01_2 (rising edge). The PR bit is set to 0 (no prescaler used) and the GT bit is set to 0 (no gate function used).
- Bits RTS4, RTS2, and RTS1 in registers G1BCR0 and G1BCR1 are set to 0 (no base timer reset). Bits UD1 to UD0 bits are set to 00_2 (counter increment mode).

Set the base timer to 0000_{16} (setting the RST1 bit to 1, and bits RST4 and RST2 to 0), when the base timer value matches the G1PO0 register setting. The base timer is set to 0000_{16} after it reaches *the G1PO0 register value + 2*.

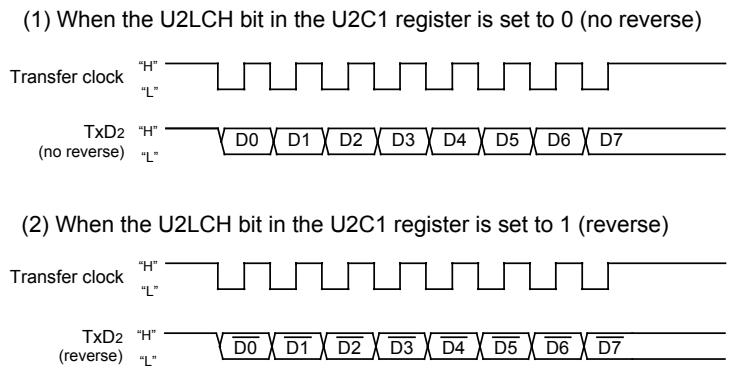
Figure 13.19 Time Measurement Function (1)

14.1.1.4 Continuous receive mode

When the UiRRM bit (i=0 to 2) is set to 1 (continuous receive mode), the TI bit in the UiC1 register is set to “0” (data present in the UiTB register) by reading the UiRB register. In this case, i.e., UiRRM bit is set to 1, do not write dummy data to the UiTB register in a program. The U0RRM and U1RRM bits are the bit 2 and bit 3 in the UCON register, respectively, and the U2RRM bit is the bit 5 in the U2C1 register.

14.1.1.5 Serial data logic switch function (UART2)

When the U2LCH bit in the U2C1 register is set to 1 (reverse), the data written to the U2TB register has its logic reversed before being transmitted. Similarly, the received data has its logic reversed when read from the U2RB register. **Figure 14.13** shows serial data logic.

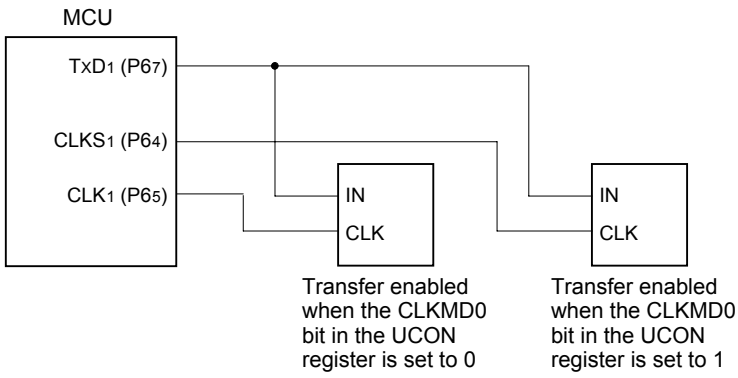


NOTE:
1. This applies to the case where the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock) and the UFORM bit is set to 0 (LSB first).

Figure 14.13 Serial data logic switch timing

14.1.1.6 Transfer clock output from multiple pins function (UART1)

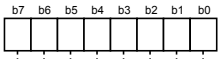
The CLKMD1 to CLKMD0 bits in the UCON register can choose one from two transfer clock output pins. (See **Figure 14.14**) This function is valid when the internal clock is selected for UART1.



NOTES:
1. This applies to the case where the CKDIR bit in the U1MRregister is set to 0 (internal clock) and the CLKMD1 bit in the UCON register is set to 1 (transfer clock output from multiple pins).
2. This applies to the case where U1MAP bit in PACR register is set to 0 (P67 to P64).

Figure 14.14 Transfer Clock Output From Multiple Pins

A/D Control Register 0 (1)



Symbol	Address	After Reset
ADCON0	$03D6_{16}$	$00000XXX_2$

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit	Function varies with each operation mode	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0	b4 b3 0 0: One-shot mode or Delayed trigger mode 0,1 0 1: Repeat mode 1 0: Single sweep mode or Simultaneous sample sweep mode 1 1: Repeat sweep mode 0 or Repeat sweep mode 1	RW
MD1			RW
TRG	Trigger select bit	0: Software trigger 1: Hardware trigger	RW
ADST	A/D conversion start flag	0: A/D conversion disabled 1: A/D conversion started	RW
CKS0	Frequency select bit 0	See **Table 15.2**	RW

NOTE:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result will be undefined.

A/D Control Register 1 (1)

Symbol	Address	After Reset
ADCON1	$03D7_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D sweep pin select bit	Function varies with each operation mode	RW
SCAN1			RW
MD2	A/D operation mode select bit 1	0 : Other than repeat sweep mode 1 1 : Repeat sweep mode 1	RW
BITS	8/10-bit mode select bit	0 : 8-bit mode 1 : 10-bit mode	RW
CKS1	Frequency select bit 1	See **Table 15.2**	RW
VCUT	Vref connect Bit (2)	0 : Vref not connected 1 : Vref connected	RW
$\overline{\text{(b7-b6)}}$	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result will be undefined.
2. If the VCUT bit is reset from 0 (Vref unconnected) to 1 (Vref connected), wait for 1 µs or more before starting A/D conversion.

A/D Control Register 2(1)

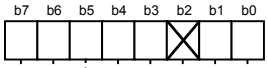
Symbol	Address	After Reset
ADCON2	$03D4_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SMP	A/D conversion method select bit	0: Without sample and hold 1: With sample and hold	RW
ADGSEL0	A/D input group select bit	b2 b1 0 0: Select port P10 group 0 1: Select port P9 group 1 0: Select port P0 group 1 1: Select port P1/P9 group	RW
ADGSEL1			RW
$\overline{\text{(b3)}}$	Reserved bit	Set to 0	RW
CKS2	Frequency select bit 2	See **Table 15.2**	RW
TRG1	Trigger select bit	Function varies with each operation mode	RW
$\overline{\text{(b7-b6)}}$	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTE:
1. If the ADCON2 register is rewritten during A/D conversion, the conversion result will be undefined.

Figure 15.2 ADCON0 to ADCON2 Registers

A/D Conversion Status Register 0 (1)



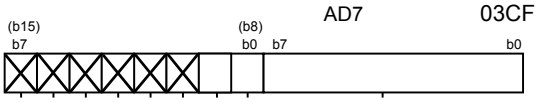
Symbol	Address	After reset
ADSTAT0	03D3₁₆	00₁₆

Bit Symbol	Bit Name	Function	RW
ADERR0	AN1 trigger status flag	0: AN1 trigger did not occur during AN0 conversion 1: AN1 trigger occured during AN0 conversion	RW
ADERR1	Conversion termination flag	0: Conversion not terminated 1: Conversion terminated by Timer B0 underflow	RW
(b2)	Nothing is assigned. If necessary, set to 0. When read, its content is 0		—
ADTCSF	Delayed trigger sweep status flag	0: Sweep not in progress 1: Sweep in progress	RO
ADSTT0	AN0 conversion status flag	0: AN0 conversion not in progress 1: AN0 conversion in progress	RO
ADSTT1	AN1 conversion status flag	0: AN1 conversion not in progress 1: AN1 conversion in progress	RO
ADSTRT0	AN0 conversion completion status flag	0: AN0 conversion not completed 1: AN0 conversion completed	RW
ADSTRT1	AN1 conversion completion status flag	0: AN1 conversion not completed 1: AN1 conversion completed	RW

NOTE:
1. ADSTAT0 register is valid only when the DTE bit in the ADTRGCON register is set to 1.

A/D Register i (i=0 to 7)

Symbol	Address	After Reset
AD0	03C1₁₆ to 03C0₁₆	Undefined
AD1	03C3₁₆ to 03C2₁₆	Undefined
AD2	03C5₁₆ to 03C4₁₆	Undefined
AD3	03C7₁₆ to 03C6₁₆	Undefined
AD4	03C9₁₆ to 03C8₁₆	Undefined
AD5	03CB₁₆ to 03CA₁₆	Undefined
AD6	03CD₁₆ to 03CC₁₆	Undefined
AD7	03CF₁₆ to 03CE₁₆	Undefined



Function		RW
When the BITS bit in the ADCON1 register is 1 (10-bit mode)	When the BITS bit in the ADCON1 register is 0 (8-bit mode)	RW
Eight low-order bits of A/D conversion result	A/D conversion result	RO
Two high-order bits of A/D conversion result	When read, its content is undefined	RO
Nothing is assigned. If necessary, set to 0. When read, its content is 0		—

Figure 15.4 ADSTAT0 Register and AD0 to AD7 Registers

A/D Control Register 0 (1)

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
			0	0				ADCON0	03D6$_{16}$	00000XXX$_2$

Bit Symbol	Bit Name	Function	RW
CH0	Analog input pin select bit (2, 3)	b2 b1 b0 0 0 0: Select AN0 0 0 1: Select AN1 0 1 0: Select AN2 0 1 1: Select AN3 1 0 0: Select AN4 1 0 1: Select AN5 1 1 0: Select AN6 1 1 1: Select AN7	RW
CH1			RW
CH2			RW
MD0	A/D operation mode select bit 0 (3)	b4 b3 0 0: One-shot mode or delayed trigger mode 0,1	RW
MD1			RW
TRG	Trigger select bit	0: Software trigger 1: Hardware trigger ($\overline{\text{ADTRG}}$ trigger)	RW
ADST	A/D conversion start flag	0: A/D conversion disabled 1: A/D conversion started	RW
CKS0	Frequency select bit 0	See **Table 15.2**	RW

NOTES:
1. If the ADCON0 register is rewritten during A/D conversion, the conversion result will be undefined.
2. AN00 to AN07, AN20 to AN27, and AN30 to AN32 can be used in the same way as AN0 to AN7. Use bits ADGSEL1 and ADGSEL 0 in the ADCON2 register to select the desired pin.
3. After rewriting bits MD1 and MD0, set bits CH2 to CH0 over again using an another instruction.

A/D Control Register 1 (1)

b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
X	X	1			0			ADCON1	03D7$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
SCAN0	A/D sweep pin select bit	Invalid in one-shot mode	RW
SCAN1			RW
MD2	A/D operation mode select bit 1	0: Other than repeat sweep mode 1	RW
BITS	8/10-bit mode select bit	0: 8-bit mode 1: 10-bit mode	RW
CKS1	Frequency select bit 1	See **Table 15.2**	RW
VCUT	Vref connect Bit (2)	1: Vref connected	RW
$\overline{\text{(b7-b6)}}$	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTES:
1. If the ADCON1 register is rewritten during A/D conversion, the conversion result will be undefined.
2. If the VCUT bit is reset from 0 (Vref unconnected) to 1 (Vref connected), wait for 1 µs or more before starting A/D conversion.

A/D Control Register 2(1)

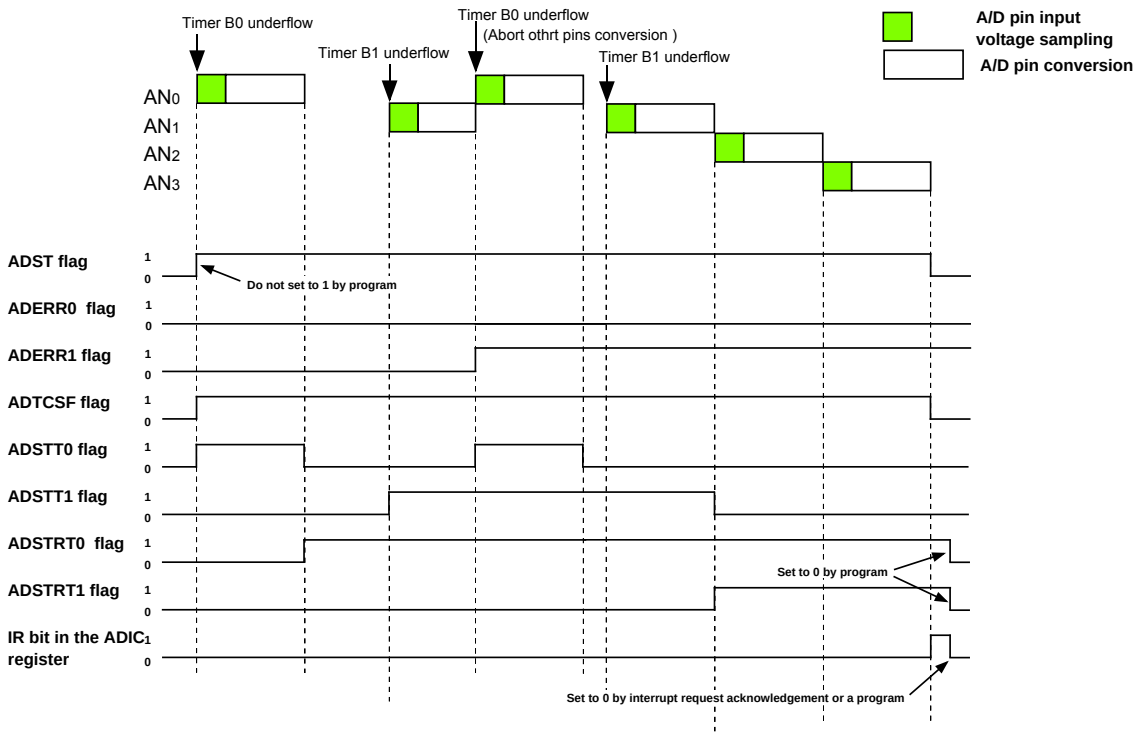
b7	b6	b5	b4	b3	b2	b1	b0	Symbol	Address	After Reset
X	X	0		0				ADCON2	03D4$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
SMP	A/D conversion method select bit	0: Without sample and hold 1: With sample and hold	RW
ADGSEL0	A/D input group select bit	b2 b1 0 0: Select port P10 group 0 1: Select port P9 group 1 0: Select port P0 group 1 1: Select port P1/P9 group	RW
ADGSEL1			RW
$\overline{\text{(b3)}}$	Reserved bit	Set to 0	RW
CKS2	Frequency select bit 2	See **Table 15.2**	RW
TRG1	Trigger select bit	Set to 0 in one-shot mode	RW
$\overline{\text{(b7-b6)}}$	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTE:
1. If the ADCON2 register is rewritten during A/D conversion, the conversion result will be undefined.

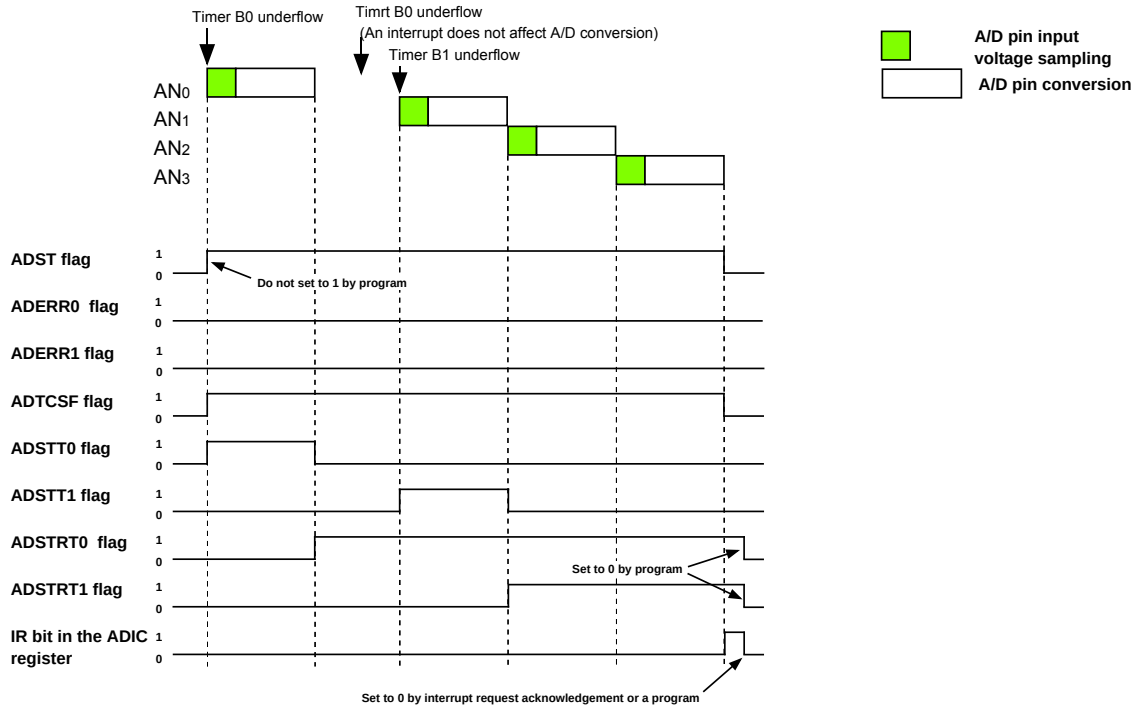
Figure 15.7 ADCON0 to ADCON2 Registers in One-Shot Mode

•Example 3: When Timer B0 underflow is generated during A/D pin conversion of any pins except AN0 pin



ADST flag: Bit 6 in the ADCON0 register
ADERR0, ADERR1, ADTCSF, ADSTT0, ADSTT1, ADSTRT0 and ADSTRT1 flag: bits 0, 1, 3, 4, 5, 6 and 7 in the ADSTAT0 register

•Example 4: After Timer B0 underflow is generated and when Timer B0 underflow is generated again before Timer B1 underflow is genetaed



ADST flag: Bit 6 in the ADCON0 register
ADERR0, ADERR1, ADTCSF, ADSTT0, ADSTT1, ADSTRT0 and ADSTRT1 flag: bits 0, 1, 3, 4, 5, 6 and 7 in the ADSTAT0 register

Figure 15.21 Each Flag Operation in ADSTAT0 Register Associated with the Operation Example in Delayed Trigger Mode 0 (2)

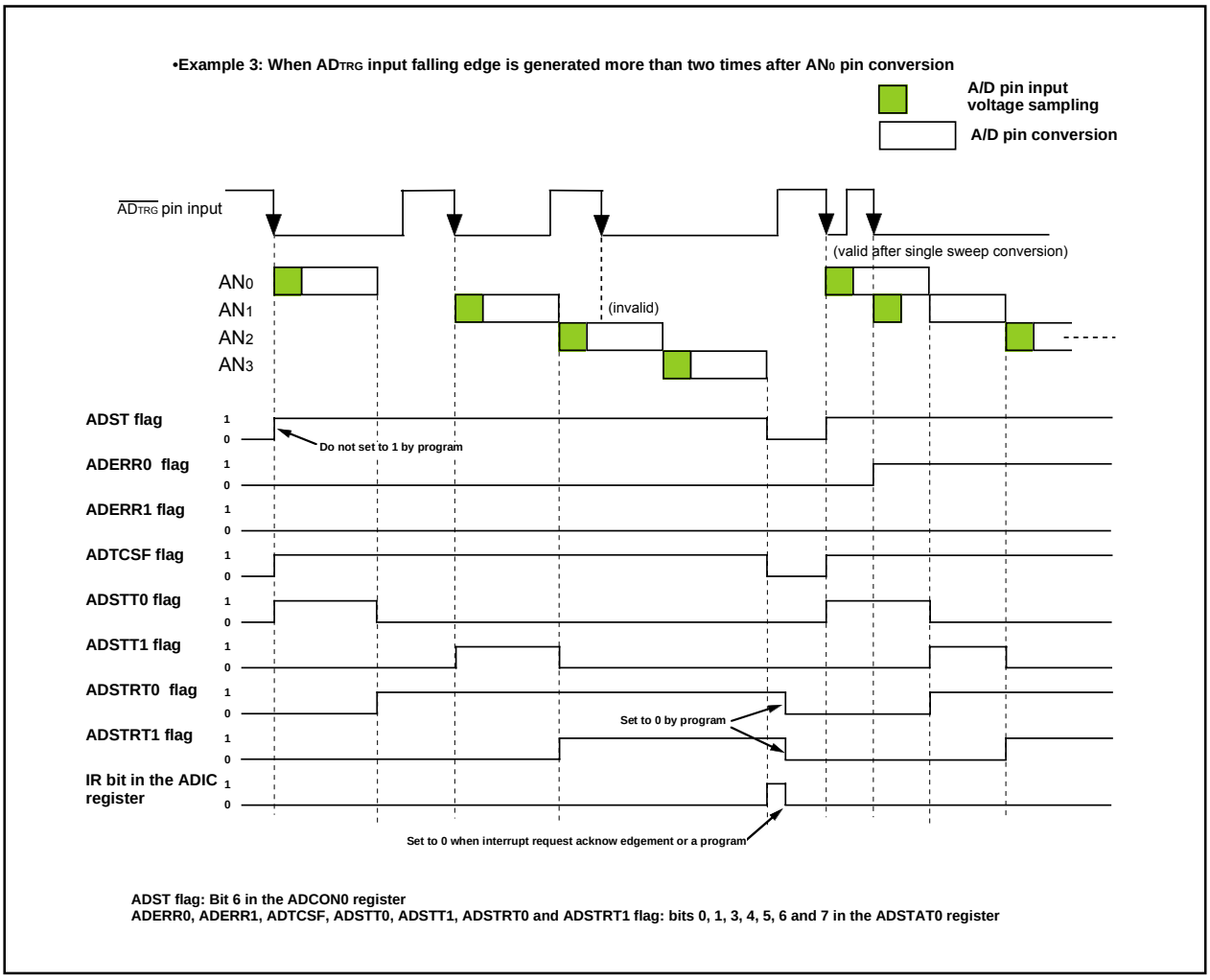


Figure 15.26 Each Flag Operation in ADSTAT0 Register Associated with the Operation Example in Delayed Trigger Mode 1 (2)

16.3 I2C0 Clock Control Register (S20 register)

The S20 register is used to set theACK control, SCL mode and the SCL frequency.

16.3.1 Bits 0 to 4: SCL Frequency Control Bits (CCR0–CCR4)

These bits control the SCL frequency. See **Table 16.3** .

16.3.2 Bit 5: SCL Mode Specification Bit (FAST MODE)

The FAST MODE bit selects SCL mode. When the FAST MODE bit is set to 0, standard clock mode is entered. When it is set to 1, high-speed clock mode is entered.

When using the high-speed clock mode I2C bus standard (400 kbits/s maximum) to connect buses, set the FAST MODE bit to 1 (select SCL mode as high-speed clock mode) and use the I2C bus system clock (VIIC) at 4 MHz or more frequency.

16.3.3 Bit 6: ACK Bit (ACKBIT)

The ACKBIT bit sets the SDA status when an ACK clock(1) is generated. When the ACKBIT bit is set to “0”, ACK is returned and te clock applied to SDA becomes "L" when ACK clock is generated. When it is set to 1, ACK is not returned and the clock clock applied to SDA maintains "H" at ACK clock generation.

When the ACKBIT bit is set to 0, the address data is received. When the slave address matches with the address data, SDA becomes "L" automatically (ACK is returned). When the slave address and the address data are not matched, SDA becomes "H" (ACK is not returned).

NOTE:

1. ACK clock: Clock for acknowledgment

16.3.4 Bit 7: ACK Clock Bit (ACK-CLK)

The ACK-CLK bit set a clock for data transfer acknowledgement. When the ACK-CLK bit is set to 0, ACK clock is not generated after data is transferred. When it is set to 1, a master generates ACK clock every one-bit data transfer is completed. The device, which transmits address data and control data, leave SDA pin open (apply "H" signal to SDA) when ACK clock is generated. The device which receives data, receives the generated ACKBIT bit.

NOTE:

1.Do not rewrite the S20 register, other than the ACKBIT bit during data transfer. If data is written to other than the ACKBIT bit during transfer, the I2C bus clock circuit is reset and the data may not be transferred successfully.

16.14 Precautions

(1) Access to the registers of I2C bus interface circuit

The following is precautions when read or write the control registers of I2C bus interface circuit

•S00 register

Do not rewrite the S00 register during data transfer. If the bits in the S00 register are rewritten, the bit counter for transfer is reset and data may not be transferred successfully.

•S1D0 register

Bits BC2 o BC0 are set to 0002 when START condition is detected or when 1-byte data transfer is completed. Do not read or write the S1D0 register at this timing. Otherwise, data may be read or written unsuccessfully. **Figures 16.22** and **16.23** show the bit counter reset timing.

•S20 register

Do not rewrite the S20 register except the ACKBIT bit during transfer. If the bits in the S20 register except ACKBIT bit are rewritten, the I2C bus clock circuit is reset and data may be transferred incompletely.

•S3D0 register

Rewrite bits ICK4 to ICK0 in the S3D0 register when the ES0 bit in the S1D0 register is set to 0 (I2C bus interface is disabled). When the WIT bit is read, the internal WAIT flag is read. Therefore, do not use the bit managing instruction(read-modify-write instruction) to access the S3D0 register.

•S10 register

Do not use the bit managing instruction (read-modify-write instruction) because all bits in the S10 register will be changed, depending on the communication conditions. Do not read/write when te communication mode select bits, bits MST and TRX, are changing their value. Otherwise, data may be read or written unsuccessfully. **Figures 16.21** to **16.23** show the timing when bits MST and TRX change.

$\overline{NMI}$ Digital Debounce Register (1,2)

b7 b0

Symbol	Address	After Reset
NDDR	033E16	FF16

Function	Setting Range	RW
If the set value =n, - n = 0 to FE16; a signal with pulse width, greater than (n+1)/f8, is input into $\overline{NMI}$ / $\overline{SD}$ - n = FF16; the digital debounce filter is disabled and all signals are input	0016 to FF16	RW

NOTES:
1. Set the PACR register by the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enable).
2. When using the $\overline{NMI}$ interrupt to exit from stop mode, set the NDDR registert to FF16 before entering stop mode.

P17 Digital Debounce Register(1)

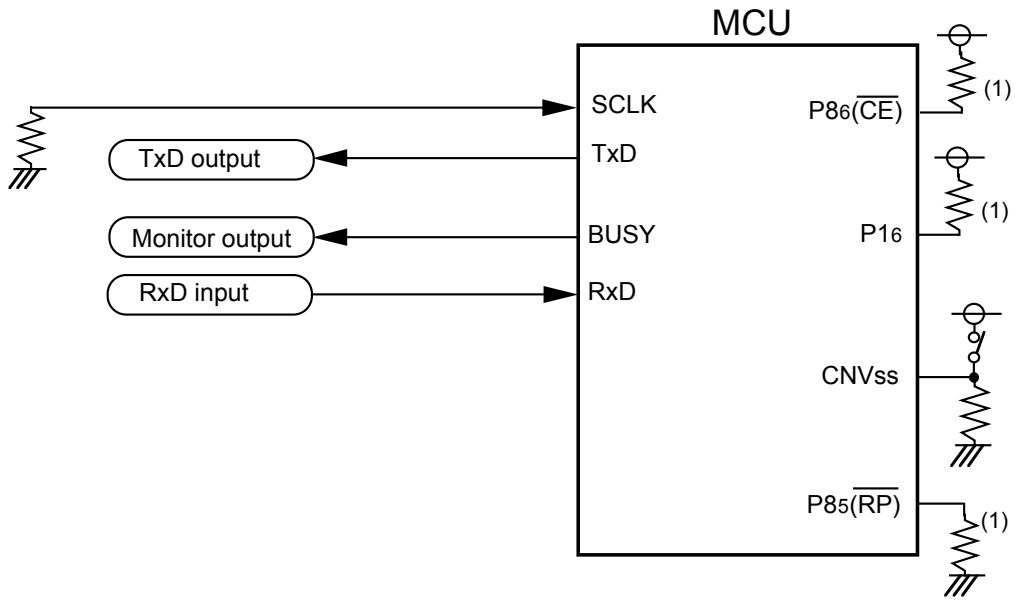
b7 b0

Symbol	Address	After Reset
P17DDR	033F16	FF16

Function	Setting Range	RW
If the set value =n, - n = 0 to FE16; a signal with pulse width, greater than (n+1)/f8, is input into INPC17/ $\overline{INT5}$ - n = FF16; the digital debounce filter is disabled and all signals are input	0016 to FF16	RW

NOTE:
1. When using the $\overline{INT5}$ interrupt to exit from stop mode, set the P17DDR registert to FF16 before entering stop mode.

Figure 18.11 NDDR and P17DDR Registers



(1) In this example, a selector controls the input voltage applied to CNVss to switch between single-chip mode and standard serial I/O mode.

NOTE:
1. Set the following, either or both.
   - Connect the $\overline{CE}$ pin to Vcc
   - Connect the $\overline{RP}$ pin to Vss and the P1 6 pin to Vcc

Figure 19.17 Circuit Application in Standard Serial I/O Mode 2

VCC = 5V

Timing Requirements

(VCC=5V, VSS=0V, at Topr=-40 to 125°C unless otherwise specified)

Table 20.54 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 20.55 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 20.56 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 20.57 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Width	125		ns

Table 20.58 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	70		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 20.59 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

21.14.9 Interrupts

EW Mode 0

- Any interrupt which has a vector in the variable vector table can be used providing that its vector is transferred into the RAM area.
- The $\overline{\text{NMI}}$ and watchdog timer interrupts can be used because the FMR0 register and FMR1 register are initialized when one of those interrupts occurs. The jump addresses for those interrupt service routines should be set in the fixed vector table.
  Because the rewrite operation is halted when a $\overline{\text{NMI}}$ or watchdog timer interrupt occurs, the rewrite program must be executed again after exiting the interrupt service routine.
- The address match interrupt cannot be used because the flash memory's internal data is referenced.

EW Mode 1

- Make sure that any interrupt which has a vector in the variable vector table or address match interrupt will not be accepted during the auto program period or auto erase period with erase-suspend function disabled.
- The $\overline{\text{NMI}}$ interrupt can be used because the FMR0 register and FMR1 register are initialized when this interrupt occurs. The jump address for the interrupt service routine should be set in the fixed vector table.
  Because the rewrite operation is halted when a $\overline{\text{NMI}}$ interrupt occurs, the rewrite program must be executed again after exiting the interrupt service routine.

21.14.10 How to Access

To set the FMR01, FMR02, FMR11 or FMR16 bit to 1, set the subject bit to 1 immediately after setting to 0. Do not generate an interrupt or a DMA transfer between the instruction to set the bit to 0 and the instruction to set the bit to 1. Set the bit when the PM24 bit is set to 1 ($\overline{\text{NMI}}$ funciton) and a high-level ("H") signal is applied to the $\overline{\text{NMI}}$ pin.

21.14.11 Writing in the User ROM Area

EW Mode 0

- If the power supply voltage drops while rewriting any block in which the rewrite control program is stored, a problem may occur that the rewrite control program is not correctly rewritten and, consequently, the flash memory becomes unable to be rewritten thereafter. In this case, standard serial I/O or parallel I/O mode should be used.

EW Mode 1

- Avoid rewriting any block in which the rewrite control program is stored.

21.14.12 DMA Transfer

In EW mode 1, make sure that no DMA transfers will occur while the FMR00 bit in the FMR0 register is set to 0(during the auto program or auto erase period).

21.14.13 Regarding Programming/Erasure Times and Execution Time

As the number of programming/erasure times increases, so does the execution time for software commands (program command and block erase command).
The software commands are aborted by hardware reset 1, $\overline{\text{NMI}}$ interrupt, and watchdog timer interrupt. If a software command is aborted by such reset or interrupt, the affected block must be erased before reexecuting the aborted command.

Appendix 2.2 Difference between M16C/28 Group T-/V-ver. and M16C/29 Group T-/V-ver. (1)

Item	Description	M16C/28(T-ver./V-ver.)	M16C/29(T-ver./V-ver.)
Protection	Function of the PRC0 bit	Enable to set the CM0, CM1, CM2, POCR, PLC0 and PCLKR registers	Enable to set the CM0, CM1, CM2, POCR, PLC0, PCLKR and CCLKR registers
Interrupt	The IFSR20 bit setting in the IFSR2A register	Set to 1	Set to 0
	The b1 bit in the IFSR2A register	Not available (reserved bit)	Interrupt cause switching bit (0: A/D conversion, 1:key input)
	The b2 bit in the IFSR2A register	Not available (reserved bit)	Interrupt cause switching bit (0: CAN0 wake-up/ error)
	Interrupt cause in the Interrupt number 13	Key input interrupt	CAN0 error
	Interrupt cause in the Interrupt number 14	Key input interrupt	A/D, key input interrupt
CAN module	compatible to 2.0B	Not available (all related registers are reserved registers)	Available (1 channel)
Pin Function	2 pins (80-pin/85-pin package), 62 pins (64-pin package)	$P9_3$/$AN2_4$	$P9_3$/$AN2_4$/CTX
	3 pins (80-pin/85-pin package), 64 pins (64-pin package)	$P9_2$/$TB2_{IN}$	$P9_2$/$AN3_2$/$TB2_{IN}$/CRX
Flash Memory	$P9_3$ in standard serial I/O mode	I/O	CTX output

I: Input O: Output I/O: Input and output

NOTE:
1. Since the M16C/28 group uses the common emulator used in the M16C/29 group, all the functions are available for M16C/28. When evaluating M16C/28 group, do not access to the SFR which is not built-in the M16C/28 gorup. Refere to hardware manual for details and electrical characteristics.

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HARDWARE MANUAL
M16C/28 Group (T-ver./V-ver.)

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