# Renesas Electronics America Inc - M30281FATHP#U3AAD6 Datasheet

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| Program Memory Size | - |
| Program Memory Type | - |
| EEPROM Size | - |
| RAM Size | - |
| Voltage - Supply (Vcc/Vdd) | - |
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| Oscillator Type | - |
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# Table of Contents

**Table 1.11 Pin Description (64-Pin and 80-Pin Packages) (Continued)**

| Classification | Symbol | I/O Type | Function |
|---|---|---|---|
| Timer S | $INPC1_0$ to $INPC1_7$ | I | Input pins for the time measurement function |
| | $OUTC1_0$ to $OUTC1_7$ | O | Output pins for the waveform generating function |
| I/O Ports | $P0_0$ to $P0_3$<br>$P1_5$ to $P1_7$<br>$P2_0$ to $P2_7$<br>$P3_0$ to $P3_3$<br>$P6_0$ to $P6_7$<br>$P7_0$ to $P7_7$<br>$P8_0$ to $P8_7$<br>$P9_0$ to $P9_3$<br>$P10_0$ to $P10_7$ | I/O | CMOS I/O ports which have a direction register determines an individual pin is used as an input port or an output port. A pull-up resistor is selectable for every 4 input ports. |

I : Input O : Output I/O : Input and output

## 7.7 System Clock Protective Function

When the main clock is selected for the CPU clock source, this function protects the clock from modifications in order to prevent the CPU clock from becoming halted by run-away.

If the PM21 bit in the PM2 register is set to 1 (clock modification disabled), the following bits are protected against writes:

- Bits CM02, CM05, and CM07 in CM0 register
- Bits CM10 and CM11 in CM1 register
- CM20 bit in CM2 register
- All bits in the PLC0 register

Before the system clock protective function can be used, the following register settings must be made while the CM05 bit in the CM0 register is 0 (main clock oscillating) and CM07 bit is 0 (main clock selected for the CPU clock source):

(1) Set the PRC1 bit in the PRCR register to 1 (enable writes to PM2 register).

(2) Set the PM21 bit in the PM2 register to 1 (disable clock modification).

(3) Set the PRC1 bit in the PRCR register to 0 (disable writes to PM2 register).

Do not execute the WAIT instruction when the PM21 bit is 1.

## 7.8 Oscillation Stop and Re-oscillation Detect Function

The oscillation stop and re-oscillation detect function detects the re-oscillation after stop of main clock oscillation circuit. When the oscillation stop and re-oscillation detection occurs, the oscillation stop detect function is reset or oscillation stop and re-oscillation detection interrupt is generated, depending on the CM27 bit set in the CM2 register. The oscillation stop detect function is enabled or disabled by the CM20 bit in the CM2 register. **Table 7.8** lists a specification overview of the oscillation stop and re-oscillation detect function.

**Table 7.8 Specification Overview of Oscillation Stop and Re-oscillation Detect Function**

| Item | Specification |
|---|---|
| Oscillation stop detectable clock and frequency bandwidth | $f(X_{IN}) \geq 2$ MHz |
| Enabling condition for oscillation stop, re-oscillation detection function | Set CM20 bit to 1(enable) |
| Operation at oscillation stop, re-oscillation detection | •Reset occurs (when CM27 bit =0)<br>•Oscillation stop, re-oscillation detection interrupt occurs(when CM27 bit =1) |

## Interrupt Request Register (1)

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| Symbol | Address | After Reset |
|---|---|---|
| G1IR | $0330_{16}$ | Undefined |

| Bit Symbol | Bit Name | Function | RW |
|---|---|---|---|
| G1IR0 | Interrupt request, Ch0 | 0 : No interrupt request<br>1 : Interrupt requested | RW |
| G1IR1 | Interrupt request, Ch1 | | RW |
| G1IR2 | Interrupt request, Ch2 | | RW |
| G1IR3 | Interrupt request, Ch3 | | RW |
| G1IR4 | Interrupt request, Ch4 | | RW |
| G1IR5 | Interrupt request, Ch5 | | RW |
| G1IR6 | Interrupt request, Ch6 | | RW |
| G1IR7 | Interrupt request, Ch7 | | RW |

NOTE:
1. When writing 0 to each bit in the G1IR register, use the following instruction:
AND, BCLR

**Figure 13.9 G1IR Register**

**Table 14.7** lists the functions of the input/output pins in UART mode. **Table 14.8** lists the $P6_4$ pin functions during UART mode. Note that for a period from when the UARTi operation mode is selected to when transfer starts, the TxDi pin outputs an “H”. (If the N-channel open-drain output is selected, this pin is in a high-impedance state.)

**Table 14.7 I/O Pin Functions in UART mode(1)**

| Pin Name | Function | Method of Selection |
|---|---|---|
| TxDi (i = 0 to 2) ($P6_3$, $P6_7$, $P7_0$) | Serial data output | (Outputs "H" when performing reception only) |
| RxDi ($P6_2$, $P6_6$, $P7_1$) | Serial data input | PD6_2 bit, PD6_6 bit in the PD6 register and the PD7_1 bit in the PD7 register (Can be used as an input port when performing transmission only) |
| CLKi ($P6_1$, $P6_5$, $P7_2$) | Input/output port | Set the CKDIR bit in the UiMR register to 0 |
| | Transfer clock input | Set the CKDIR bit in the UiMR register to 1<br>Set the PD6_1 bit and PD6_5 bit in the PD6 register to 0, PD7_2 bit in the PD7 register to 0 |
| $\overline{CTS}i/\overline{RTS}i$ ($P6_0$, $P6_4$, $P7_3$) | $\overline{CTS}$ input | Set the CRD bit in the UiC0 register to 0<br>Set the CRS bit in the UiC0 register to 0<br>Set the PD6_0 bit and PD6_4 bit in the PD6 register to 0, the PD7_3 bit in the PD7 register 0 |
| | $\overline{RTS}$ output | Set the CRD bit in the UiC0 register to 0<br>Set the CRS bit in the UiC0 register to 1 |
| | Input/output port | Set the CRD bit in the UiC0 register 1 |

NOTE:
1. When the U1MAP bit in PACR register is set to 1 ($P7_3$ to $P7_0$), UART1 pin is assgined to $P7_3$ to $P7_0$.

**Table 14.8 $P6_4$ Pin Functions in UART mode (1)**

| Pin Function | Bit Set Value | | | | |
|---|---|---|---|---|---|
| | U1C0 register | | UCON register | | PD6 register |
| | CRD | CRS | RCSP | CLKMD1 | PD6_4 |
| $P6_4$ | 1 | — | 0 | 0 | Input: 0, Output: 1 |
| $\overline{CTS}_1$ | 0 | 0 | 0 | 0 | 0 |
| $\overline{RTS}_1$ | 0 | 1 | 0 | 0 | — |
| $\overline{CTS}_0$ (2) | 0 | 0 | 1 | 0 | 0 |

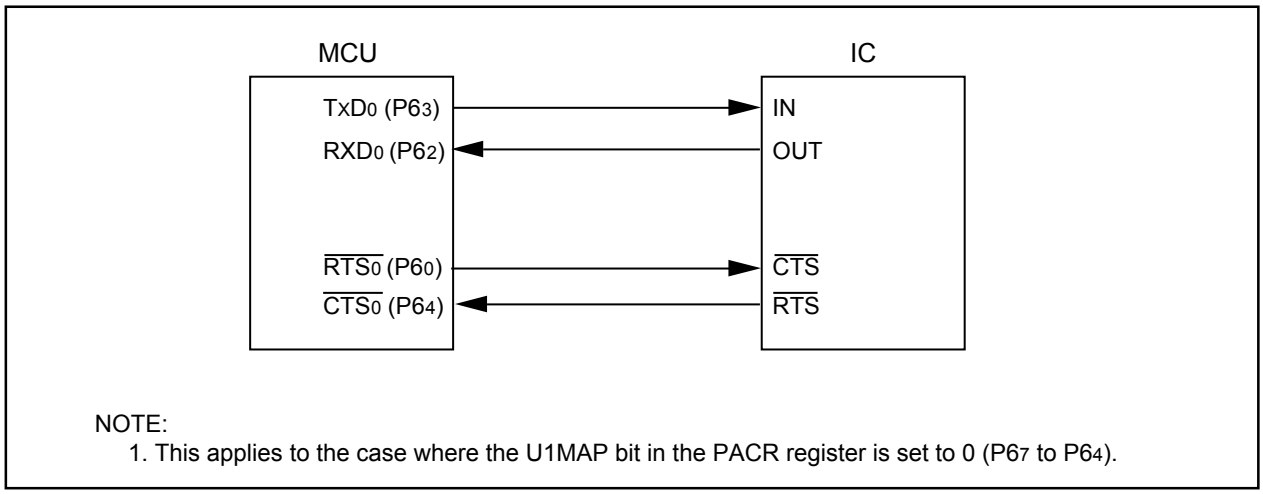
NOTES:
1. When the U1MAP bit in PACR register is 1 ($P7_3$ to $P7_0$), this table lists the $P7_0$ functions.
2. In addition to this, set the CRD bit in the U0C0 register to 0 ($\overline{CTS}_0/\overline{RTS}_0$ enabled) and the CRS bit in the U0C0 register to 1 ($\overline{RTS}_0$ selected).

#### 14.1.2.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Separate Function (UART0)

This function separates $\overline{\text{CTS}}_0/\overline{\text{RTS}}_0$, outputs $\overline{\text{RTS}}_0$ from the $P6_0$ pin, and accepts as input the $\overline{\text{CTS}}_0$ from the $P6_4$ pin or $P7_0$ pin. To use this function, set the register bits as shown below.

- The CRD bit in the U0C0 register is set to 0 (enables UART0 $\overline{\text{CTS}}/\overline{\text{RTS}}$)
- The CRS bit in the U0C0 register is set to 1 (outputs UART0 $\overline{\text{RTS}}$)
- The CRD bit in the U1C0 register is set to 0 (enables UART1 $\overline{\text{CTS}}/\overline{\text{RTS}}$)
- The CRS bit in the U1C0 register is set to 0 (inputs UART1 $\overline{\text{CTS}}$)
- The RCSP bit in the UCON register is set to 1 (inputs $\overline{\text{CTS}}_0$ from the $P6_4$ pin or $P7_0$ pin)
- The CLKMD1 bit in the UCON register is set to 0 ($CLKS_1$ not used)

Note that when using the $\overline{\text{CTS}}/\overline{\text{RTS}}$ separate function, UART1 $\overline{\text{CTS}}/\overline{\text{RTS}}$ separate function cannot be used.




NOTE:
1. This applies to the case where the U1MAP bit in the PACR register is set to 0 ($P6_7$ to $P6_4$).

**Figure 14.21 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Separate Function**

#### 14.1.3.1 Detection of Start and Stop Condition

Whether a start or a stop condition has been detected is determined.

A start condition-detected interrupt request is generated when the SDA2 pin changes state from high to low while the SCL2 pin is in the high state. A stop condition-detected interrupt request is generated when the SDA2 pin changes state from low to high while the SCL2 pin is in the high state.

Because the start and stop condition-detected interrupts share the interrupt control register and vector, check the BBS bit in the U2SMR register to determine which interrupt source is requesting the interrupt.

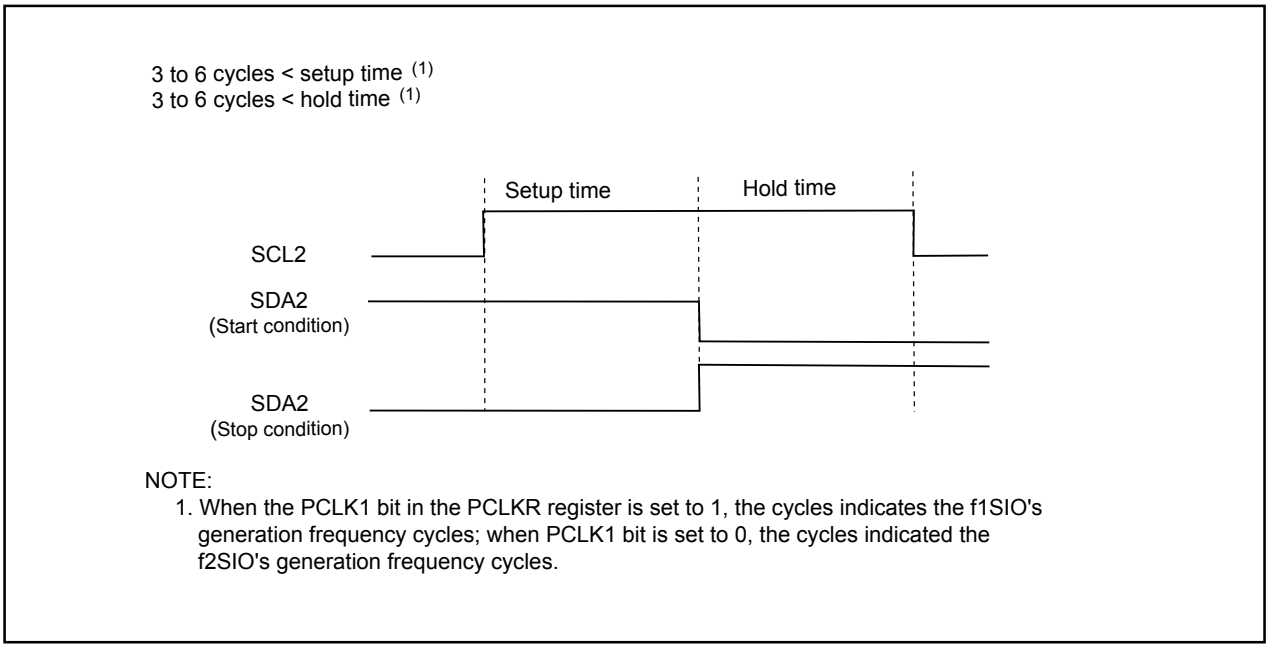



**Figure 14.24 Detection of Start and Stop Condition**

#### 14.1.3.2 Output of Start and Stop Condition

A start condition is generated by setting the STAREQ bit in the U2SMR4 register to 1 (start).

A restart condition is generated by setting the RSTAREQ bit in the U2SMR4 register to 1 (start).

A stop condition is generated by setting the STPREQ bit in the U2SMR4 register to 1 (start).

The output procedure is described below.

(1) Set the STAREQ bit, RSTAREQ bit or STPREQ bit to 1 (start).

(2) Set the STSPSEL bit in the U2SMR4 register to 1 (output).

Make sure that no interrupts or DMA transfers will occur between (1) and (2).

The function of the STSPSEL bit is shown in **Table 14.14** and **Figure 14.25**.

## 14.2 SI/O3 and SI/O4

**Note**

The SI/O4 interrupt of peripheral function interrupt is not available in the 64-pin package.

SI/O3 and SI/O4 are exclusive clock-synchronous serial I/Os.

**Figure 14.35** shows the block diagram of SI/O3 and SI/O4, and **Figure 14.36** shows the SI/O3 and SI/O4-related registers.

**Table 14.20** shows the specifications of SI/O3 and SI/O4.

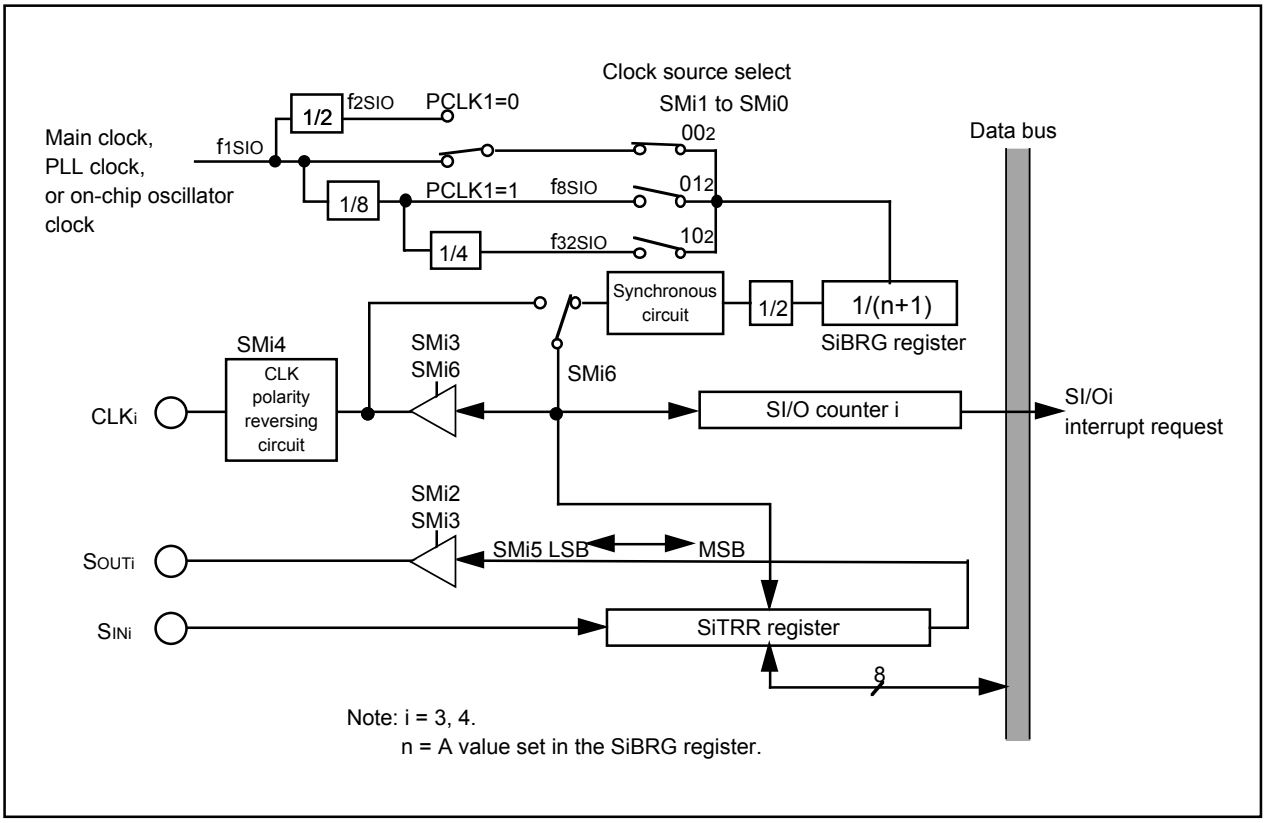



**Figure 14.35 SI/O3 and SI/O4 Block Diagram**

A/D Trigger Control Register (1)

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | 1 | 1 | 1 | 1 |

| Symbol | Address | After Reset |
|---|---|---|
| ADTRGCON | $03D2_{16}$ | $00_{16}$ |

| Bit Symbol | Bit Name | Function | RW |
|---|---|---|---|
| SSE | A/D operation mode select bit 2 | Simultaneous sample sweep mode or delayed trigger mode 0, 1 | RW |
| DTE | A/D operation mode select bit 3 | Delayed trigger mode 0, 1 | RW |
| HPTRG0 | $AN_0$ trigger select bit | See **Table 15.11** | RW |
| HPTRG1 | $AN_1$ trigger select bit | See **Table 15.11** | RW |
| — (b7-b4) | Nothing is assigned. If necessary, set to 0. When read, the content is 0 | | — |

NOTE:
1. If ADTRGCON is rewritten during A/D conversion, the conversion result will be undefined.

**Figure 15.23 ADTRGCON Register in Delayed Trigger Mode 0**

**Table 15.11 Trigger Select Bit Setting in Delayed Trigger Mode 0**

| TRG | TRG1 | HPTRG0 | HPTRG1 | Trigger |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | Timer B0, B1 underflow |

I2C0 Control Register 1

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

| Symbol | Address | After Reset |
|---|---|---|
| S3D0 | 02E616 | 001100002 |

| Bit Symbol | Bit Name | Function | RW |
|---|---|---|---|
| SIM | The interrupt enable bit for STOP condition detection | 0: Disable the I2C bus interface interrupt of STOP condition detection<br>1: Enable the I2C bus interface interrupt of STOP condition detection | RW |
| WIT | The interrupt enable bit for data receive completion | 0: Disable the I2C bus interface interrupt of data receive completion<br>1: Enable the I2C bus interface interrupt of data receive completion<br><br>When setting NACK (ACK bit = 0), write 0 | RW |
| PED | SDA/port function switch bit(1) | 0: SDA I/O pin<br>1: Port output pin | RW |
| PEC | SCL/port function switch bit(1) | 0: SCL I/O pin<br>1: Port output pin | RW |
| SDAM | The logic value monitor bit of SDA output | 0: SDA output logic value = 0<br>1: SDA output logic value = 1 | RO |
| SCLM | The logic value monitor bit of SCL output | 0: SCL output logic value = 0<br>1: SCL output logic value = 1 | RO |
| ICK0 | I2C bus system clock selection bits,<br>if bits ICK4 to ICK2 in the S4D0 register is 0002 | b7 b6<br>0 0 : VIIC =1/2 fIIC<br>0 1 : VIIC =1/4 fIIC<br>1 0 : VIIC =1/8 fIIC<br>1 1 : Reserved (2) | RW |
| ICK1 | | | RW |

NOTE:
1. Bits PED and PEC are enabled when the ES0 bit in the S1D0 register is set to 1 (I2C bus interface enabled).
2. When the PCLK0 bit in the PCLKR register is set to 0, fIIC=f2. When the PCLK0 bit in the PCLKR register is set to 1, fIIC=f1.

**Figure 16.6 S3D0 Register**

## 16.5 I2C0 Status Register (S10 register)

The S10 register monitors the I2C bus interface status. When using the S10 register to check the status, use the 6 low-order bits for read only.

### 16.5.1 Bit 0: Last Receive Bit (LRB)

The LRB bit stores the last bit value of received data. It can also be used to confirm whether ACK is received. If the ACK-CLK bit in the S20 register is set to 1 (with ACK clock) and ACK is returned when the ACK clock is generated, the LRB bit is set to 0. If ACK is not returned, the LRB bit is set to 1. When the ACK-CLK bit is set to 0 (no ACK clock), the last bit value of received data is input. When writing data to the S00 register, the LRB bit is set to 0.

### 16.5.2 Bit 1: General Call Detection Flag (ADR0)

When the ALS bit in the S1D0 register is set to 0 (addressing format), this ADR0 flag is set to 1 by receiving the general calls(1),whose address data are all 0, in slave mode.
The ADR0 flag is set to 0 when STOP or START conditions is detected or when the IHR bit in the S1D0 register is set to 1 (reset).

NOTE:
1. General call: A master device transmits the general call address $00_{16}$ to all slaves. When the master device transmits the general call, all slave devices receive the controlled data after general call.

### 16.5.3 Bit 2: Slave Address Comparison Flag (AAS)

The AAS flag indicates a comparison result of the slave address data after enabled by setting the ALS bit in the S1D0 register to 0 (addressing format).
The AAS flag is set to 1 when the 7 bits of the address data are matched with the slave address stored into the S0D0 register, or when a general call is received, in slave receive mode. The AAS flag is set to 0 by writing data to the S00 register. When the ES0 bit in the S1D0 register is set to 0 (I2C bus interface disabled) or when the IHR bit in the S1D0 register is set to 1 (reset), the AAS flag is also set to 0.

### 16.5.4 Bit 3: Arbitration Lost Detection Flag (AL)(1)

In master transmit mode, if an "L" signal is applied to the SDA pin by other than the MCU, the AL flag is set to 1 by determining that the arbitration is los and the TRX bit in the S10 register is set to 0 (receive mode) at the same time. The MST bit in the S10 register is set to 0 (slave mode) after transferring the bytes which lost the arbitration.
The arbitration lost can be detected only in master transmit mode. When writing data to the S00 register, the AL flag is set to 0. When the ES0 bit in the S1D0 register is set to 0 (I2C bus interface disabled) or when the IHR bit in the S1D0 register is set to 1 (reset), the AL flag is set to 0.

NOTE:
1. Arbitration lost: communication disabled as a master

### 16.13.2 Example of Slave Receive

For example, a slave receives data as shown below when following conditions are met: high-speed clock mode, SCL frequency of 400 kHz, ACK clock added and addressing format.

1) Set a slave address in the 7 high-order bits in the S0D0 register
2) Set A5$_{16}$ to the S20 register, 000$_2$ to bits ICK4 to ICK2 in the S4D0 register, and 00$_{16}$ to the S3D0 register to generate an ACK clock and set SCL clock frequency at 400kHz ($f_1$ = 8 MHz, $f_{IIC}$ = $f_1$)
3) Set 00$_{16}$ to the S10 register to reset transmit/receive mode
4) Set 08$_{16}$ to the S1D0 register to enable data communication
5) When a START condition is received, addresses are compared
6) •When the transmitted addresses are all 0 (general call), the ADR0 bit in the S10 register is set to 1 and an I2C bus interface interrupt request signal is generated.
   •When the transmitted addresses match with the address set in 1), the ASS bit in the S10 register is set to 1 and an I2C bus interface interrupt request signal is generated.
   •In other cases, bits ADR0 and AAS are set to 0 and I2C bus interface interrupt request signal is not generated.
7) Write dummy data to the S00 register.
8) After receiving 1-byte data, an ACK-CLK bit is automatically returned and an I2C bus interface interrupt request signal is generated.
9) To determine whether the ACK should be returned depending on contents in the received data, set dummy data to the S00 register to receive data after setting the WIT bit in te S3D0 register to 1 (enable the I2C bus interface interrupt of data receive completion). Because the I2C bus interface interrupt is generated when the 1-byte data is received, set the ACKBIT bit to 1 or 0 to output a signal from the ACKBIT bit.
10) When receiving more than 1-byte control data, repeat steps 7) and 8) or 7) and 9).
11) When a STOP condition is detected, the communication is ended.

$\overline{NMI}$ Digital Debounce Register (1,2)

b7 b0

| Symbol | Address | After Reset |
|---|---|---|
| NDDR | 033E16 | FF16 |

| Function | Setting Range | RW |
|---|---|---|
| If the set value =n,<br>- n = 0 to FE16; a signal with pulse width, greater than (n+1)/f8, is input into $\overline{NMI}$ / $\overline{SD}$<br>- n = FF16; the digital debounce filter is disabled and all signals are input | 0016 to FF16 | RW |

NOTES:
1. Set the PACR register by the next instruction after setting the PRC2 bit in the PRCR register to 1 (write enable).
2. When using the $\overline{NMI}$ interrupt to exit from stop mode, set the NDDR registert to FF16 before entering stop mode.

P17 Digital Debounce Register(1)

b7 b0

| Symbol | Address | After Reset |
|---|---|---|
| P17DDR | 033F16 | FF16 |

| Function | Setting Range | RW |
|---|---|---|
| If the set value =n,<br>- n = 0 to FE16; a signal with pulse width, greater than (n+1)/f8, is input into INPC17/ $\overline{INT5}$<br>- n = FF16; the digital debounce filter is disabled and all signals are input | 0016 to FF16 | RW |

NOTE:
1. When using the $\overline{INT5}$ interrupt to exit from stop mode, set the P17DDR registert to FF16 before entering stop mode.

**Figure 18.11 NDDR and P17DDR Registers**

**Table 20.41 A/D Conversion Characteristics (1)**

| Symbol | Parameter | | Measurement Condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| - | Resolution | | $V_{REF}$ = $V_{CC}$ | | | 10 | Bits |
| INL | Integral Nonlinearity Error | 10 bit | $V_{REF}$ = $V_{CC}$ = 5 V | | | ±3 | LSB |
| | | 8 bit | $V_{REF}$ = $V_{CC}$ = 5 V | | | ±2 | LSB |
| - | Absolute Accuracy | 10 bit | $V_{REF}$ = $V_{CC}$ = 5 V | | | ±3 | LSB |
| | | 8 bit | $V_{REF}$ = $V_{CC}$ = 5 V | | | ±2 | LSB |
| DNL | Differential Nonlinearity Error | | | | | ±1 | LSB |
| - | Offset Error | | | | | ±3 | LSB |
| - | Gain Error | | | | | ±3 | LSB |
| $R_{LADDER}$ | Resistor Ladder | | $V_{REF}$ = $V_{CC}$ | 10 | | 40 | kΩ |
| $t_{CONV}$ | 10-bit Conversion Time Sample & Hold Function Available | | $V_{REF}$ = $V_{CC}$ = 5 V, øAD = 10 MHz | 3.3 | | | µs |
| $t_{CONV}$ | 8-bit Conversion Time Sample & Hold Function Available | | $V_{REF}$ = $V_{CC}$ = 5 V, øAD = 10 MHz | 2.8 | | | µs |
| $V_{REF}$ | Reference Voltage | | | 2.0 | | $V_{CC}$ | V |
| $V_{IA}$ | Analog Input Voltage | | | 0 | | $V_{REF}$ | V |

NOTES:
1. Referenced to $V_{CC}$ = $AV_{CC}$ = $V_{REF}$ = 4.2 to 5.5 V, $V_{SS}$ = $AV_{SS}$ = 0 V at Topr = -40 to 125 ° C unless otherwise specified.
2. Keep ϕAD frequency at 10 MHz or less.
3. When sample & hold function is disabled, keep ϕAD frequency at 250kHz or more in addition to the limitation in Note 2.
   When sample & hold function is enabled, keep ϕAD frequency at 1MHz or more in addition to the limitation in Note 2.
4. When sample & hold function is enabled, sampling time is 3/ ϕAD frequency.
   When sample & hold function is disabled, sampling time is 2/ ϕAD frequency.

Vcc = 5V

**Table 20.46 Electrical Characteristics (2) (1)**

| Symbol | Parameter | Measurement Condition | | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $I_{CC}$ | Power Supply Current ($V_{CC}$ = 4.2 to 5.5 V) | Output pins are left open and other pins are connected to $V_{SS}$ | Mask ROM | f(BCLK) = 20 MHz, main clock, no division | | 18 | 25 | mA |
| | | | | On-chip oscillation $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz | | 2 | | mA |
| | | | Flash memory | f(BCLK) = 20 MHz, main clock, no division | | 18 | 25 | mA |
| | | | | f(BCLK) = 16 MHz, main clock, no division | | 14 | 20 | mA |
| | | | | On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz | | 2 | | mA |
| | | | Flash memory program | f(BCLK) = 10 MHz, Vcc = 5.0 V | | 11 | | mA |
| | | | Flash memory erase | f(BCLK) = 10 MHz, Vcc = 5.0 V | | 11 | | mA |
| | | | Mask ROM | f($X_{CIN}$) = 32 kHz, In low-power consumption mode, Program running on ROM(3) | | 25 | | µA |
| | | | | On-chip oscillation $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz, In wait mode | | 50 | | µA |
| | | | Flash memory | f(BCLK) = 32 kHz, In low-power consumption mode, Program running on RAM(3) | | 25 | | µA |
| | | | | f(BCLK) = 32 kHz, In low-power consumption mode, Program running on flash memory(3) | | 450 | | µA |
| | | | | On-chip oscillation, $f_{2(ROC)}$ selected, f(BCLK) = 1 MHz, In wait mode | | 50 | | µA |
| | | | Mask ROM, Flash memory | f(BCLK) = 32 kHz, In wait mode(2), Oscillation capacity high | | 8.5 | | µA |
| | | | | f(BCLK) = 32 kHz, In wait mode(2), Oscillation capacity low | | 3 | | µA |
| | | | | While clock stops, Topr = 25° C | | 0.8 | 3 | µA |

NOTES:

1. Referenced to $V_{CC}$ = 4.2 to 5.5 V, $V_{SS}$ = 0 V at Topr = -40 to 105 ° C, f(BCLK) = 20 MHz / $V_{CC}$ = 4.2 to 5.5 V, $V_{SS}$ = 0 V at Topr = -40 to 125 ° C, f(BCLK) = 16 MHz, unless otherwise specified.
2. With one timer operates, using $f_{C32}$.
3. This indicates the memory in which the program to be executed exists.

Vcc = 5V

**Timing Requirements**

**(Vcc=5V, Vss=0V, at Topr=-40 to 125°C unless otherwise specified)**

**Table 20.48 Timer A Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 100 | | ns |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 40 | | ns |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width | 40 | | ns |

**Table 20.49 Timer A Input (Gating Input in Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 400 | | ns |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 200 | | ns |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width | 200 | | ns |

**Table 20.50 Timer A Input (External Trigger Input in One-shot Timer Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 200 | | ns |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width | 100 | | ns |

**Table 20.51 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(TAH)}$ | TAiIN Input High ("H") Width | 100 | | ns |
| $t_{w(TAL)}$ | TAiIN Input Low ("L") Width | 100 | | ns |

**Table 20.52 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(UP)}$ | TAiOUT Input Cycle Time | 2000 | | ns |
| $t_{w(UPH)}$ | TAiOUT Input High ("H") Width | 1000 | | ns |
| $t_{w(UPL)}$ | TAiOUT Input Low ("L") Width | 1000 | | ns |
| $t_{su(UP-TIN)}$ | TAiOUT Input Setup Time | 400 | | ns |
| $t_{h(TIN-UP)}$ | TAiOUT Input Hold Time | 400 | | ns |

**Table 20.53 Timer A Input (Two-phase Pulse Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN Input Cycle Time | 800 | | ns |
| $t_{su(TAIN-TAOUT)}$ | TAiOUT Input Setup Time | 200 | | ns |
| $t_{su(TAOUT-TAIN)}$ | TAiIN Input Setup Time | 200 | | ns |

VCC = 5V

**Timing Requirements**

**(VCC=5V, VSS=0V, at Topr=-40 to 125°C unless otherwise specified)**

**Table 20.54 Timer B Input (Counter Input in Event Counter Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on one edge) | 100 | | ns |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width (counted on one edge) | 40 | | ns |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width (counted on one edge) | 40 | | ns |
| $t_{c(TB)}$ | TBiIN Input Cycle Time (counted on both edges) | 200 | | ns |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width (counted on both edges) | 80 | | ns |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width (counted on both edges) | 80 | | ns |

**Table 20.55 Timer B Input (Pulse Period Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width | 200 | | ns |

**Table 20.56 Timer B Input (Pulse Width Measurement Mode)**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TB)}$ | TBiIN Input Cycle Time | 400 | | ns |
| $t_{w(TBH)}$ | TBiIN Input High ("H") Width | 200 | | ns |
| $t_{w(TBL)}$ | TBiIN Input Low ("L") Width | 200 | | ns |

**Table 20.57 A/D Trigger Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max | |
| $t_{c(AD)}$ | $\overline{ADTRG}$ Input Cycle Time (required for trigger) | 1000 | | ns |
| $t_{w(ADL)}$ | $\overline{ADTRG}$ Input Low ("L") Width | 125 | | ns |

**Table 20.58 Serial I/O**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi Input Cycle Time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi Input High ("H") Width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi Input Low ("L") Width | 100 | | ns |
| $t_{d(C-Q)}$ | TxDi Output Delay Time | | 80 | ns |
| $t_{h(C-Q)}$ | TxDi Hold Time | 0 | | ns |
| $t_{su(D-C)}$ | RxDi Input Setup Time | 70 | | ns |
| $t_{h(C-Q)}$ | RxDi Input Hold Time | 90 | | ns |

**Table 20.59 External Interrupt $\overline{INTi}$ Input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{INTi}$ Input High ("H") Width | 250 | | ns |
| $t_{w(INL)}$ | $\overline{INTi}$ Input Low ("L") Width | 250 | | ns |

# 21.13 Mask ROM Version

## 21.13.1 Internal ROM Area

In the masked ROM version, do not write to internal ROM area. Writing to the area may increase power consumption.

## 21.13.2 Reserved Bit

The b3 to b0 in addresses $0FFFFF_{16}$ are reserved bits. Set these bits to $1111_2$.

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