Renesas Electronics America Inc - M30281FATHP#U3AAM1 Datasheet

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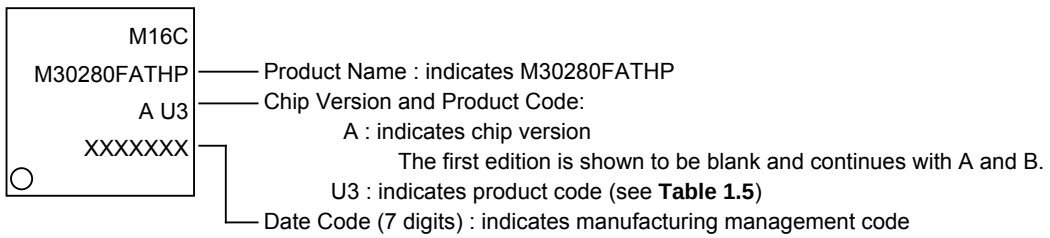
(1) Flash Memory Version, PLQP0080KB-A (80P6Q-A), T-ver.



(2) Flash Memory Version, PLQP0064KB-A (64P6Q-A), T-ver.

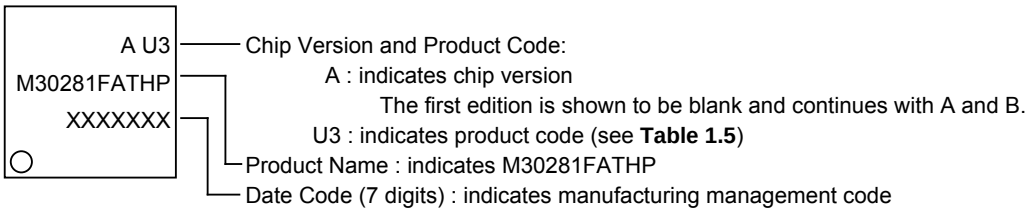
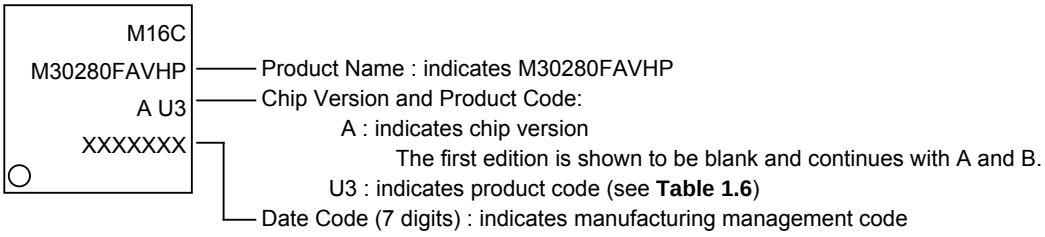


Figure 1.4 Marking Diagram of Flash Memory Version - M16C/28 Group T-ver. (Top View)

(1) Flash Memory Version, PLQP0080KB-A (80P6Q-A), V-ver.



(2) Flash Memory Version, PLQP0064KB-A (64P6Q-A), V-ver.

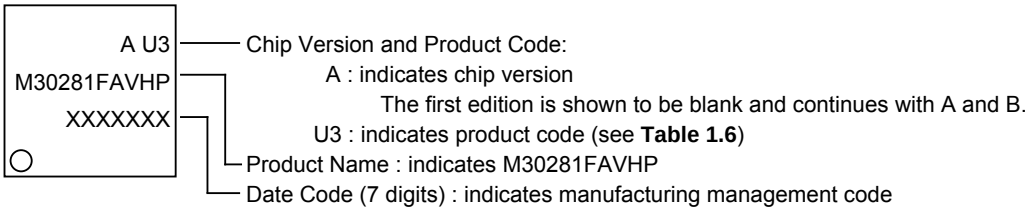


Figure 1.5 Marking Diagram of Flash Memory version - M16C/28 Group V-ver. (Top View)

Table 4.7 SFR Information(7)(1)

Address	Register	Symbol	After Reset
03C0₁₆	A/D register 0	AD0	XX₁₆
03C1₁₆			XX₁₆
03C2₁₆	A/D register 1	AD1	XX₁₆
03C3₁₆			XX₁₆
03C4₁₆	A/D register 2	AD2	XX₁₆
03C5₁₆			XX₁₆
03C6₁₆	A/D register 3	AD3	XX₁₆
03C7₁₆			XX₁₆
03C8₁₆	A/D register 4	AD4	XX₁₆
03C9₁₆			XX₁₆
03CA₁₆	A/D register 5	AD5	XX₁₆
03CB₁₆			XX₁₆
03CC₁₆	A/D register 6	AD6	XX₁₆
03CD₁₆			XX₁₆
03CE₁₆	A/D register 7	AD7	XX₁₆
03CF₁₆			XX₁₆
03D0₁₆			
03D1₁₆			
03D2₁₆	A/D trigger control register	ADTRGCON	00₁₆
03D3₁₆	A/D status register 0	ADSTAT0	00000X00₂
03D4₁₆	A/D control register 2	ADCON2	00₁₆
03D5₁₆			
03D6₁₆	A/D control register 0	ADCON0	00000XXX₂
03D7₁₆	A/D control register 1	ADCON1	00₁₆
03D8₁₆			
03D9₁₆			
03DA₁₆			
03DB₁₆			
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 register	P0	XX₁₆
03E1₁₆	Port P1 register	P1	XX₁₆
03E2₁₆	Port P0 direction register	PD0	00₁₆
03E3₁₆	Port P1 direction register	PD1	00₁₆
03E4₁₆	Port P2 register	P2	XX₁₆
03E5₁₆	Port P3 register	P3	XX₁₆
03E6₁₆	Port P2 direction register	PD2	00₁₆
03E7₁₆	Port P3 direction register	PD3	00₁₆
03E8₁₆			
03E9₁₆			
03EA₁₆			
03EB₁₆			
03EC₁₆	Port P6 register	P6	XX₁₆
03ED₁₆	Port P7 register	P7	XX₁₆
03EE₁₆	Port P6 direction register	PD6	00₁₆
03EF₁₆	Port P7 direction register	PD7	00₁₆
03F0₁₆	Port P8 register	P8	XX₁₆
03F1₁₆	Port P9 register	P9	XX₁₆
03F2₁₆	Port P8 direction register	PD8	00₁₆
03F3₁₆	Port P9 direction register	PD9	000X0000₂
03F4₁₆	Port P10 register	P10	XX₁₆
03F5₁₆			
03F6₁₆	Port P10 direction register	PD10	00₁₆
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆	Pull-up control register 0	PUR0	00₁₆
03FD₁₆	Pull-up control register 1	PUR1	00₁₆
03FE₁₆	Pull-up control register 2	PUR2	00₁₆
03FF₁₆	Port control register	PCR	00₁₆

NOTE:
1. The blank areas are reserved and cannot be used by users.

X : Undefined

Watchdog Timer Control Register

b7	b6	b5	b4	b3	b2	b1	b0
	0	0					

Symbol	Address	After Reset
WDC	$000F_{16}$	$00XXXXXX_2$

Bit Symbol	Bit Name	Function	RW
(b4-b0)	High-order bit of watchdog timer		RO
$\overline{(b5)}$	Reserved bit	Set to 0	RW
$\overline{(b6)}$	Reserved bit	Set to 0	RW
WDC7	Prescaler select bit	0 : Divided by 16 1 : Divided by 128	RW

Watchdog Timer Start Register

b7	b0

Symbol	Address	After Reset
WDTS	$000E_{16}$	Undefined

Function	RW
The watchdog timer is initialized and starts counting after a write instruction to this register. The watchdog timer value is always initialized to $7FFF_{16}$ regardless of whatever value is written.	WO

Figure 10.2 WDC Register and WDTS Register

10.1 Count Source Protective Mode

In this mode, a on-chip oscillator clock is used for the watchdog timer count source. The watchdog timer can be kept being clocked even when CPU clock stops as a result of run-away.

Before this mode can be used, the following register settings are required:

(1) Set the PRC1 bit in the PRCR register to 1 (enable writes to PM1 and PM2 registers).

(2) Set the PM12 bit in the PM1 register to 1 (reset when the watchdog timer underflows).

(3) Set the PM22 bit in the PM2 register to 1 (on-chip oscillator clock used for the watchdog timer count source).

(4) Set the PRC1 bit in the PRCR register to 0 (disable writes to PM1 and PM2 registers).

(5) Write to the WDTS register (watchdog timer starts counting).

Setting the PM22 bit to 1 results in the following conditions

- The on-chip oscillator continues oscillating even if the CM21 bit in the CM2 register is set to "0" (main clock or PLL clock) (system clock of count source selected by the CM21 bit is valid)
- The on-chip oscillator starts oscillating, and the on-chip oscillator clock becomes the watchdog timer count source.

$$\text{Watchdog timer period} = \frac{\text{Watchdog timer count (32768)}}{\text{on-chip oscillator clock}}$$

- The CM10 bit in the CM1 register is disabled against write. (Writing a 1 has no effect, nor is stop mode entered.)
- The watchdog timer does not stop when in wait mode.

12.1.1 Timer Mode

In timer mode, the timer counts a count source generated internally (see **Table 12.1**). **Figure 12.7** shows TAiMR register in timer mode.

Table 12.1 Specifications in Timer Mode

Item	Specification
Count source	f_1, f_2, f_8, f_{32}, f_{C32}
Count operation	• Decrement • When the timer underflows, it reloads the reload register contents and continues counting
Divide ratio	1/(n+1) n: set value of TAi register (i= 0 to 4) 0000_{16} to $FFFF_{16}$
Count start condition	Set TAiS bit in the TABSR register to 1 (start counting)
Count stop condition	Set TAiS bit to 0 (stop counting)
Interrupt request generation timing	Timer underflow
TAiIN pin function	I/O port or gate input
TAiOUT pin function	I/O port or pulse output
Read from timer	Count value can be read by reading TAi register
Write to timer	• When not counting and until the 1st count source is input after counting start Value written to TAi register is written to both reload register and counter • When counting (after 1st count source input) Value written to TAi register is written to only reload register (Transferred to counter when reloaded next)
Select function	• Gate function Counting can be started and stopped by an input signal to TAiIN pin • Pulse output function Whenever the timer underflows, the output polarity of TAiOUT pin is inverted. When not counting, the pin outputs a low.

Timer Ai Mode Register (i=0 to 4)

b7	b6	b5	b4	b3	b2	b1	b0
		0				0	0

Symbol: TA0MR to TA4MR
Address: 0396_{16} to $039A_{16}$
After Reset: 00_{16}

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0: Timer mode	RW
TMOD1			RW
MR0	Pulse output function select bit	0: Pulse is not output (TAiOUT pin is a normal port pin) 1: Pulse is output (TAiOUT pin is a pulse output pin)	RW
MR1	Gate function select bit	b4 b3 0 0: } Gate function not available (TAiIN pin functions as I/O port) 0 1: } 1 0: Counts while input on the TAiIN pin is low (1) 1 1: Counts while input on the TAiIN pin is high (1)	RW
MR2			RW
MR3	Set to 0 in timer mode		RW
TCK0	Count source select bit	b7 b6 0 0: f_1 or f_2 0 1: f_8 1 0: f_{32} 1 1: f_{C32}	RW
TCK1			RW

NOTE:
1. The port direction bit for the TAiIN pin must be set to 0 (input mode).

Figure 12.7 Timer Ai Mode Register in Timer Mode

12.2 Timer B

Figure 12.15 shows a block diagram of the timer B. **Figures 12.16** and **12.17** show registers related to the timer B.

Timer B supports the following four modes. Use bits TMOD1 and TMOD0 in the TBiMR register (i = 0 to 2) to select the desired mode.

- Timer mode: The timer counts the internal count source.
- Event counter mode: The timer counts the external pulses or overflows and underflows of other timers.
- Pulse period/pulse width measurement mode: The timer measures the pulse period or pulse width of external signal.
- A/D trigger mode: The timer starts counting by one trigger until the count value becomes 0000_{16}. This mode is used together with simultaneous sample sweep mode or delayed trigger mode 0 of A/D converter to start A/D conversion.

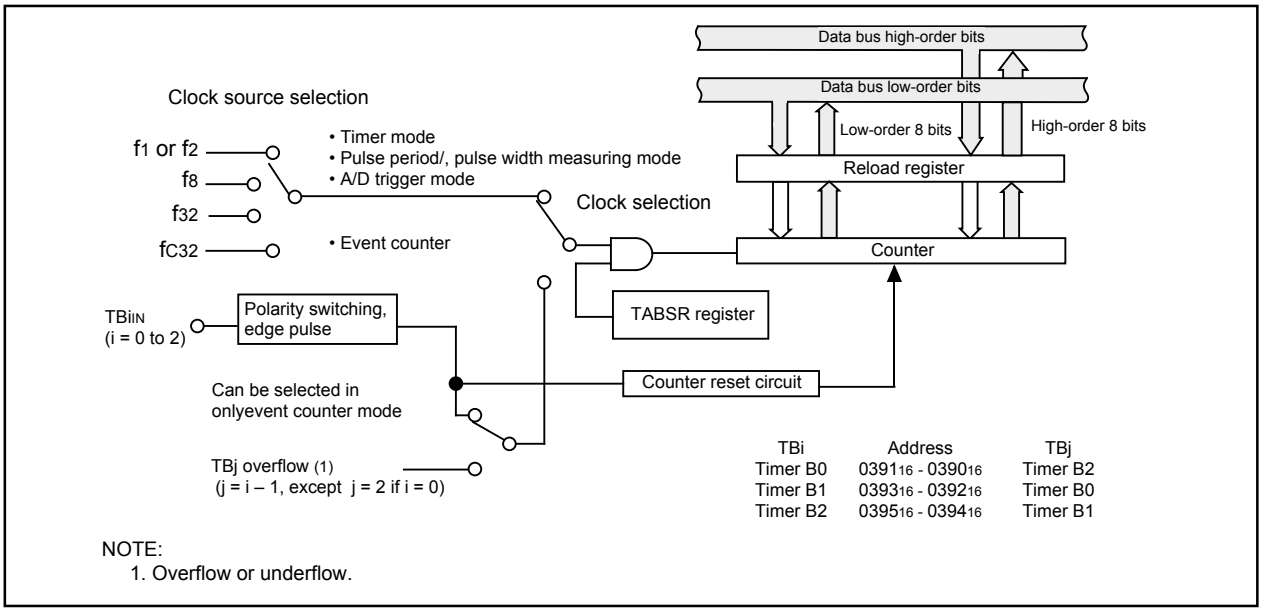


Figure 12.15 Timer B Block Diagram

Timer Bi Mode Register (i=0 to 2)

Symbol	Address	After Reset
TB0MR to TB2MR	039B16 to 039D16	00XX0000₂

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0 : Timer mode or A/D trigger mode 0 1 : Event counter mode 1 0 : Pulse period measurement mode, pulse width measurement mode 1 1 : Do not set	RW
TMOD1			RW
MR0	———	Function varies with each operation mode	RW
MR1			RW
MR2			RW(1) —— (2)
MR3			RO
TCK0	Count source select bit	Function varies with each operation mode	RW
TCK1			RW

NOTES:
1. Timer B0.
2. Timer B1, Timer B2.

Figure 12.16 TB0MR to TB2MR Registers

Timer Bi Mode Register (i= 0 to 1)

b7	b6	b5	b4	b3	b2	b1	b0
						0	0

Symbol: TB0MR to TB1MR
Address: 039B16 to 039C16
After Reset: 00XX00002

Bit Symbol	Bit Name	Function	RW
TMOD0	Operation mode select bit	b1 b0 0 0: Timer mode or A/D trigger mode	RW
TMOD1			RW
MR0	Invalid in A/D trigger mode Either 0 or 1 is enabled		RW
MR1			RW
MR2	TB0MR register Set to 0 in A/D trigger mode		RW
	TB1MR register Nothing is assigned. If necessary, set to 0. When read, its content is undefined		—
MR3	When write in A/D trigger mode, set to 0. When read in A/D trigger mode, the content is undefined		RO
TCK0	Count source select bit (1)	b7 b6 0 0: f1 or f2 0 1: f8 1 0: f32 1 1: fC32	RW
TCK1			RW

NOTE:
1. When this bit is used in delayed trigger mode 0, set the same count source to the timer B0 and timer B1.

Figure 12.23 TBiMR Register in A/D Trigger Mode

Timer B2 special mode register (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	0	0		1	1		

Symbol: TB2SC
Address: 039E16
After Reset: X00000002

Bit Symbol	Bit Name	Function	RW
PWCON	Timer B2 reload timing switch bit (2)	0: Timer B2 underflow 1: Timer A output at odd-numbered	RW
IVPCR1	Three-phase output port $\overline{SD}$ control bit 1 (3, 4, 7)	0: Three-phase output forcible cutoff by $\overline{SD}$ pin input (high impedance) disabled 1: Three-phase output forcible cutoff by $\overline{SD}$ pin input (high impedance) enabled	RW
TB0EN	Timer B0 operation mode select bit	0: Other than A/D trigger mode 1: A/D trigger mode (5)	RW
TB1EN	Timer B1 operation mode select bit	0: Other than A/D trigger mode 1: A/D trigger mode (5)	RW
TB2SEL	Trigger select bit (6)	0: TB2 interrupt 1: Underflow of TB2 interrupt generation frequency setting counter [ICTB2]	RW
$\overline{\text{(b6-b5)}}$	Reserved bits	Set to 0	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, its content is 0		—

NOTES:
1. Write to this register after setting the PRC1 bit in the PRCR register to 1 (write enabled).
2. If the INV11 bit is 0 (three-phase mode 0) or the INV06 bit is 1 (triangular wave modulation mode), set this bit to 0 (timer B2 underflow).
3. When setting the IVPCR1 bit to 1 (three-phase output forcible cutoff by $\overline{SD}$ pin input enabled), set the PD8_5 bit to 0 (= input mode).
4. Related pins are U(P80), $\overline{U}$(P81), V(P72), $\overline{V}$(P73), W(P74), $\overline{W}$(P75). After forcible cutoff, input "H" to the P85/$\overline{NMI}$/$\overline{SD}$ pin. Set the IVPCR1 bit to 0, and this forcible cutoff will be reset. If "L" is input to the P85/$\overline{NMI}$/$\overline{SD}$ pin, a three-phase motor control timer output will be disabled (INV03=0). At this time, when the IVPCR1 bit is 0, the target pins changes to programmable I/O port. When the IVPCR1 bit is 1, the target pins changes to high-impedance state regardless of which functions of those pins are used.
5. When this bit is used in delayed trigger mode 0, set bits TB0EN and TB1EN to 1 (A/D trigger mode).
6. When setting the TB2SEL bit to 1 (underflow of TB2 interrupt generation frequency setting counter[ICTB2]), set the INV02 bit to 1 (three-phase motor control timer function).
7. Refer to "**18.6 Digital Debounce function**" for the $\overline{SD}$ input.

Figure 12.24 TB2SC Register in A/D Trigger Mode

13.4 Time Measurement Function

In synchronization with an external trigger input, the value of the base timer is stored into the G1TMj register (j=0 to 7). **Table 13.5** shows specifications of the time measurement function. **Table 13.6** shows register settings associated with the time measurement function. **Figures 13.19** and **13.20** display operational timing of the time measurement function. **Figure 13.21** shows operational timing of the prescaler function and the gate function.

Table 13.5 Time Measurement Function Specifications

Item	Specification
Measurement channel	Channels 0 to 7
Selecting trigger input polarity	Rising edge, falling edge, both edges of the INPC1j pin (1)
Measurement start condition	The IFEj bit in the G1FE register should be set to 1 (channels j function enabled) when the FSCj bit (j=0 to 7) in the G1FS register is set to 1 (time measurement function selected).
Measurement stop condition	The IFEj bit should be set to 0 (channel j function disabled)
Time measurement timing	•No prescaler : every time a trigger signal is applied •Prescaler (for channel 6 and channel 7): every *G1TPRk (k=6,7) register value +1* times a trigger signal is applied
Interrupt request generation timing	The G1IRi bit (i=0 to 7) in the interrupt request register (See **Figure 13.9**) is set to 1 at time measurement timing
INPC1j pin function (1)	Trigger input pin
Selectable function	• Digital filter function The digital filter samples a trigger input signal level every f_1, f_2 or f_{BT1} cycles and passes pulse signal matching trigger input signal level three times • Prescaler function (for channel 6 and channel 7) Time measurement is executed every *G1TPRk register value +1* times a trigger signal is applied • Gate function (for channel 6 and channel 7) After time measurement by the first trigger input, trigger input cannot be accepted. However, while the GOC bit in the G1TMCRk register is set to 1 (gate cleared by matching the base timer with the G1POp register (p=4 when k=6, p=5 when k=7)), trigger input can be accepted again by matching the base timer value with the G1POp register setting • Digital Debounce function (for channel7) See **13.6.2 Digital Debounce Function for P17/$\overline{\text{INT5}}$/INPC17** and **18.6 Digital Debounce Function** for details

NOTE:
1. The INPC10 to INPC17 pins

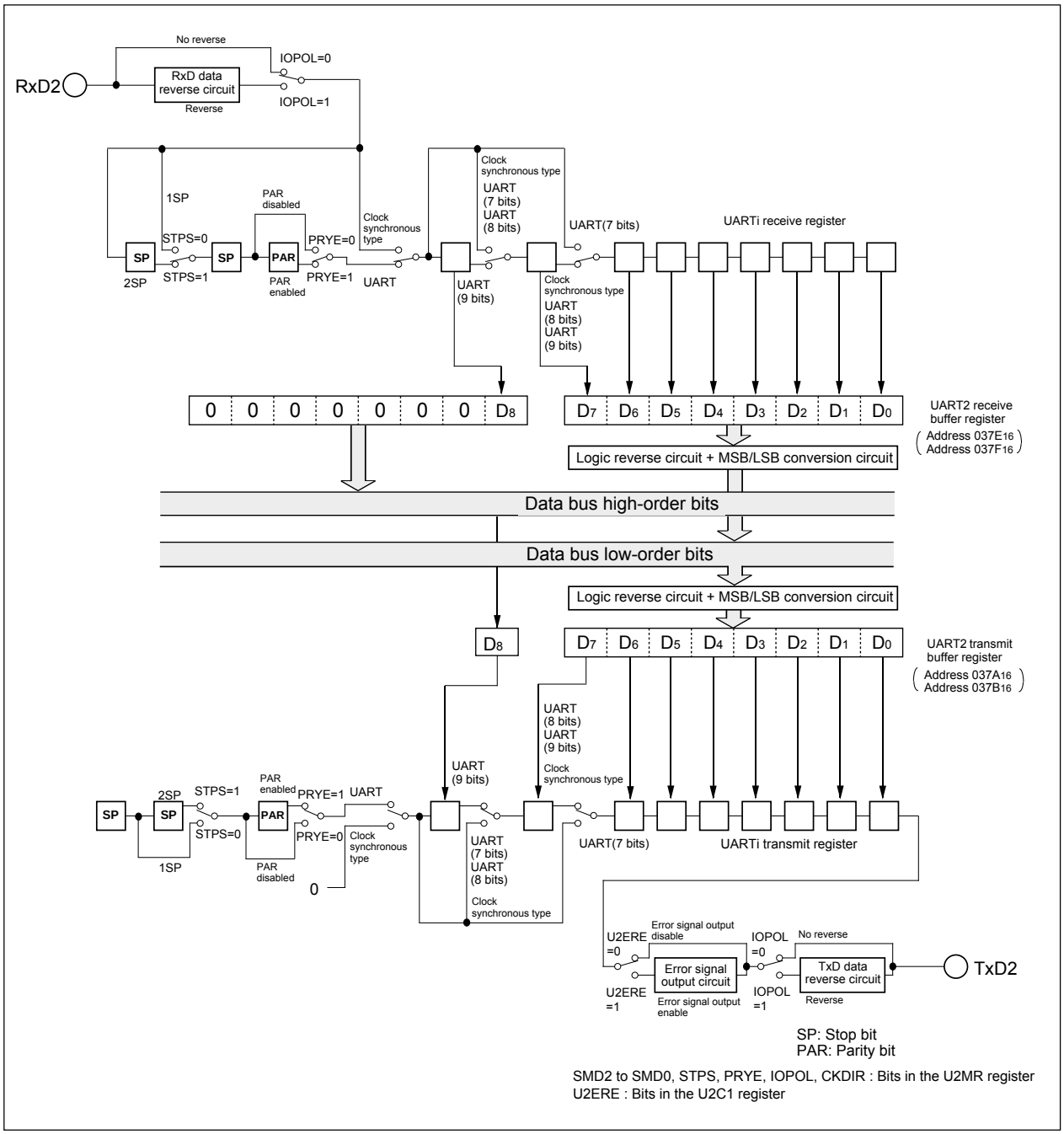


Figure 14.3 Block diagram of UART2 transmit/receive unit

UARTi Transmit/receive Mode Register (i=0, 1)

b7	b6	b5	b4	b3	b2	b1	b0
0							

Symbol	Address	After Reset
U0MR, U1MR	$03A0_{16}$, $03A8_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O mode select bit (2)	b2 b1 b0 0 0 0 : Serial I/O disabled 0 0 1 : Clock synchronous serial I/O mode 1 0 0 : UART mode transfer data 7 bit long 1 0 1 : UART mode transfer data 8 bit long 1 1 0 : UART mode transfer data 9 bit long Do not set the value other than the above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock (1)	RW
STPS	Stop bit length select bit	0 : One stop bit 1 : Two stop bits	RW
PRY	Odd/even parity select bit	Effective when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
$\overline{\text{(b7)}}$	Reserve bit	Set to 0	RW

NOTES:
1. Set the corresponding port direction bit for each CLKi pin to 0 (input mode).
2. To receive data, set the corresponding port direction bit for each RxDi pin to 0.

UART2 Transmit/receive Mode Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
U2MR	0378_{16}	00_{16}

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O mode select bit (2)	b2 b1 b0 0 0 0 : Serial I/O disabled 0 0 1 : Clock synchronous serial I/O mode 0 1 0 : I^2C bus mode(3) 1 0 0 : UART mode transfer data 7 bit long 1 0 1 : UART mode transfer data 8 bit long 1 1 0 : UART mode transfer data 9 bits long Do not set the value other than the above	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock (1)	RW
STPS	Stop bit length select bit	0 : One stop bit 1 : Two stop bits	RW
PRY	Odd/even parity select bit	Effective when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
IOPOL	TxD, RxD I/O polarity reverse bit	0 : No reverse 1 : Reverse	RW

NOTES:
1. Set the corresponding port direction bit for each CLK2 pin to 0 (input mode).
2. To receive data, set the corresponding port direction bit for each RxD2 pin to 0 (input mode).
3. Set the corresponding port direction bit for SCL_2 and SDA_2 pins to 0 (input mode).

Figure 14.5 U0MR to U2MR Registers

I2C0 Control Register 2

b7	b6	b5	b4	b3	b2	b1	b0
	0						

Symbol	Address	After Reset
S4D0	02E716	0016

Bit Symbol	Bit Name	Function	RW
TOE	Time out detection function enable bit	0: Disabled 1: Enabled	RW
TOF	Time out detection flag	0: Not detected 1: Detected	RO
TOSEL	Time out detection time select bit	0: Long time 1: Short time	RW
ICK2	I2C bus system clock select bits	b5 b4 b3 0 0 0 VIIC set by ICK1 and ICK0 bits in S3D0 register 0 0 1 VIIC = 1/2.5 fIIC 0 1 0 VIIC = 1/3 fIIC 0 1 1 VIIC = 1/5 fIIC 1 0 0 VIIC = 1/6 fIIC (1)	RW
ICK3			RW
ICK4			RW
(b6)	Reserved bit	Set to 0	RW
SCPIN	STOP condition detection interrupt request bit	0: No I2C bus interface interrupt request 1: I2C bus interface interrupt request	RW

NOTE:
1. When the PCLK0 bit in the PCLKR register is set to 0, fIIC = f2. When the PCLK0 bit is set to 1, fIIC=f1.

Figure 16.7 S4D0 Register

I2C0 Start/stop Condition Control Register

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
S2D0	02E516	000110102

Bit Symbol	Bit Name	Function	RW
SSC0	START/STOP condition setting bits(1)	Setting for detection condition of START/STOP condition. See **Table 16.2**	RW
SSC1			RW
SSC2			RW
SSC3			RW
SSC4			RW
SIP	SCL/SDA interrupt pin polarity select bit	0: Active in falling edge 1: Active in rising edge	RW
SIS	SCL/SDA interrupt pin select bit	0: SDA enabled 1: SCL enabled	RW
STSPSEL	START/STOP condition generation select bit	0: Short setup/hold time mode 1: Long setup/hold time mode	RW

NOTE:
1. Do not set 000002 or odd values.

Figure 16.8 S2D0 Register

Table 16.2 Recommended setting (SSC4-SSC0) start/stop condition at each oscillation frequency

Oscillation f1 (MHz)	I2C bus system clock select	I2C bus system clock(MHz)	SSC4-SSC0(1)	SCL release time (cycle)	Setup time (cycle)	Hold time (cycle)
10	1 / 2f1(2)	5	XXX11110	6.2 µs (31)	3.2 µs (16)	3.0 µs (15)
8	1 / 2f1(2)	4	XXX11010	6.75 µs(27)	3.5 µs (14)	3.25 µs(13)
			XXX11000	6.25 µs(25)	3.25 µs (13)	3.0 µs (12)
8	1 / 8f1(2)	1	XXX00100	5.0 µs (5)	3.0 µs (3)	2.0 µs (2)
4	1 / 2f1(2)	2	XXX01100	6.5 µs (13)	3.5 µs (7)	3.0 µs (6)
			XXX01010	5.5 µs (11)	3.0 µs (6)	2.5 µs (5)
2	1 / 2f1(2)	1	XXX00100	5.0 µs (5)	3.0 µs (3)	2.0 µs (2)

NOTES:
1. Do not set odd values or 000002 to START/STOP condition setting bits (SSC4 to SSC0)
2. When the PCLK0 bit in the PCLKR register is set to 1.

16.3 I2C0 Clock Control Register (S20 register)

The S20 register is used to set theACK control, SCL mode and the SCL frequency.

16.3.1 Bits 0 to 4: SCL Frequency Control Bits (CCR0–CCR4)

These bits control the SCL frequency. See **Table 16.3** .

16.3.2 Bit 5: SCL Mode Specification Bit (FAST MODE)

The FAST MODE bit selects SCL mode. When the FAST MODE bit is set to 0, standard clock mode is entered. When it is set to 1, high-speed clock mode is entered.

When using the high-speed clock mode I2C bus standard (400 kbits/s maximum) to connect buses, set the FAST MODE bit to 1 (select SCL mode as high-speed clock mode) and use the I2C bus system clock (VIIC) at 4 MHz or more frequency.

16.3.3 Bit 6: ACK Bit (ACKBIT)

The ACKBIT bit sets the SDA status when an ACK clock(1) is generated. When the ACKBIT bit is set to “0”, ACK is returned and te clock applied to SDA becomes "L" when ACK clock is generated. When it is set to 1, ACK is not returned and the clock clock applied to SDA maintains "H" at ACK clock generation.

When the ACKBIT bit is set to 0, the address data is received. When the slave address matches with the address data, SDA becomes "L" automatically (ACK is returned). When the slave address and the address data are not matched, SDA becomes "H" (ACK is not returned).

NOTE:

1. ACK clock: Clock for acknowledgment

16.3.4 Bit 7: ACK Clock Bit (ACK-CLK)

The ACK-CLK bit set a clock for data transfer acknowledgement. When the ACK-CLK bit is set to 0, ACK clock is not generated after data is transferred. When it is set to 1, a master generates ACK clock every one-bit data transfer is completed. The device, which transmits address data and control data, leave SDA pin open (apply "H" signal to SDA) when ACK clock is generated. The device which receives data, receives the generated ACKBIT bit.

NOTE:

1.Do not rewrite the S20 register, other than the ACKBIT bit during data transfer. If data is written to other than the ACKBIT bit during transfer, the I2C bus clock circuit is reset and the data may not be transferred successfully.

16.5 I2C0 Status Register (S10 register)

The S10 register monitors the I2C bus interface status. When using the S10 register to check the status, use the 6 low-order bits for read only.

16.5.1 Bit 0: Last Receive Bit (LRB)

The LRB bit stores the last bit value of received data. It can also be used to confirm whether ACK is received. If the ACK-CLK bit in the S20 register is set to 1 (with ACK clock) and ACK is returned when the ACK clock is generated, the LRB bit is set to 0. If ACK is not returned, the LRB bit is set to 1. When the ACK-CLK bit is set to 0 (no ACK clock), the last bit value of received data is input. When writing data to the S00 register, the LRB bit is set to 0.

16.5.2 Bit 1: General Call Detection Flag (ADR0)

When the ALS bit in the S1D0 register is set to 0 (addressing format), this ADR0 flag is set to 1 by receiving the general calls(1),whose address data are all 0, in slave mode.
The ADR0 flag is set to 0 when STOP or START conditions is detected or when the IHR bit in the S1D0 register is set to 1 (reset).

NOTE:
1. General call: A master device transmits the general call address 00_{16} to all slaves. When the master device transmits the general call, all slave devices receive the controlled data after general call.

16.5.3 Bit 2: Slave Address Comparison Flag (AAS)

The AAS flag indicates a comparison result of the slave address data after enabled by setting the ALS bit in the S1D0 register to 0 (addressing format).
The AAS flag is set to 1 when the 7 bits of the address data are matched with the slave address stored into the S0D0 register, or when a general call is received, in slave receive mode. The AAS flag is set to 0 by writing data to the S00 register. When the ES0 bit in the S1D0 register is set to 0 (I2C bus interface disabled) or when the IHR bit in the S1D0 register is set to 1 (reset), the AAS flag is also set to 0.

16.5.4 Bit 3: Arbitration Lost Detection Flag (AL)(1)

In master transmit mode, if an "L" signal is applied to the SDA pin by other than the MCU, the AL flag is set to 1 by determining that the arbitration is los and the TRX bit in the S10 register is set to 0 (receive mode) at the same time. The MST bit in the S10 register is set to 0 (slave mode) after transferring the bytes which lost the arbitration.
The arbitration lost can be detected only in master transmit mode. When writing data to the S00 register, the AL flag is set to 0. When the ES0 bit in the S1D0 register is set to 0 (I2C bus interface disabled) or when the IHR bit in the S1D0 register is set to 1 (reset), the AL flag is set to 0.

NOTE:
1. Arbitration lost: communication disabled as a master

16.5.5 Bit 4: I2C bus Interface Interrupt Request Bit (PIN)

The PIN bit generates an I2C bus interface interrupt request signal. Every one byte data is ransferred, the PIN bit is changed from 1 to 0. At the same time, an I2C bus interface interrupt request is generated. The PIN bit is synchronized with the last clock of the internal transfer clock (when ACK-CLK=1, the last clock is the ACK clock: when the ACK-CLK=0, the last clock is the 8th clock) and it becomes 0. The interrupt request is generated on the falling edge of the PIN bit. When the PIN bit is set to 0, the clock applied to SCL maintains "L" and further clock generation is disabled. When the ACK-CLK bit is set to 1 and the WIT bit in the S3D0 register is set to 1 (enable the I2C bus interface interrupt of data receive completion). The PIN bit is synchronized with the last clock and the falling edge of the ACK clock. Then, the PIN bit is set to 0 and I2C bus interface interrupt request is generated. **Figure 16.11** shows the timing of the I2C bus interface interrupt request generation.

The PIN bit is set to 1 in one of the following conditions:

- •When data is written to the S00 register
- •When data is written to the S20 register (when the WIT bit is set to 1 and the internal WAIT flag is set to 1)
- •When the ES0 bit in the S1D0 register is set to 0 (I2C bus interface disabled)
- •When the IHR bit in the S1D0 register is set to 1(reset)

The PIN bit is set to 0 in one of the following conditions:

- •With completion of 1-byte data transmit (including a case when arbitration lost is detected)
- •With completion of 1-byte data receive
- •When the ALS bit in the S1D0 register is set to 0 (addressing format) and slave address is matched or general call address is received successfully in slave receive mode
- •When the ALS bit is set to 1 (free format) and the address data is received successfully in slave receive mode

16.5.6 Bit 5: Bus Busy Flag (BB)

The BB flag indicates the operating conditions of the bus system. When the BB flag is set to 0, a bus system is not in use and a START condition can be generated. The BB flag is set and reset based on an input signal of the SCL and SDA pins either in master mode or in slave mode. When the START condition is detected, the BB flag is set to 1. On the other hand, when the STOP condition is detected, the BB flag is set to 0. Bits SSC4 to SSC0 in the S2D0 register decide to detect between the START condition and the STOP condition. When the ES0 bit in the S1D0 register is set to 0 (I2C bus interface disabled) or when the IHR bit in the S1D0 register is set to 1 (reset), the BB flag is set to 0. Refer to **16.9 START Condition Generation Method and 16.11 STOP Condition Generation Method**.

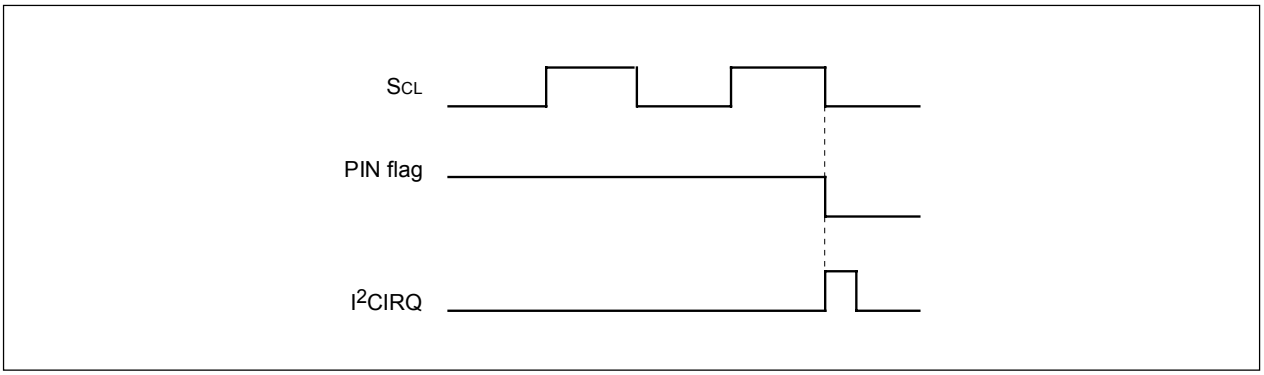


Figure 16.11 Interrupt request signal generation timing

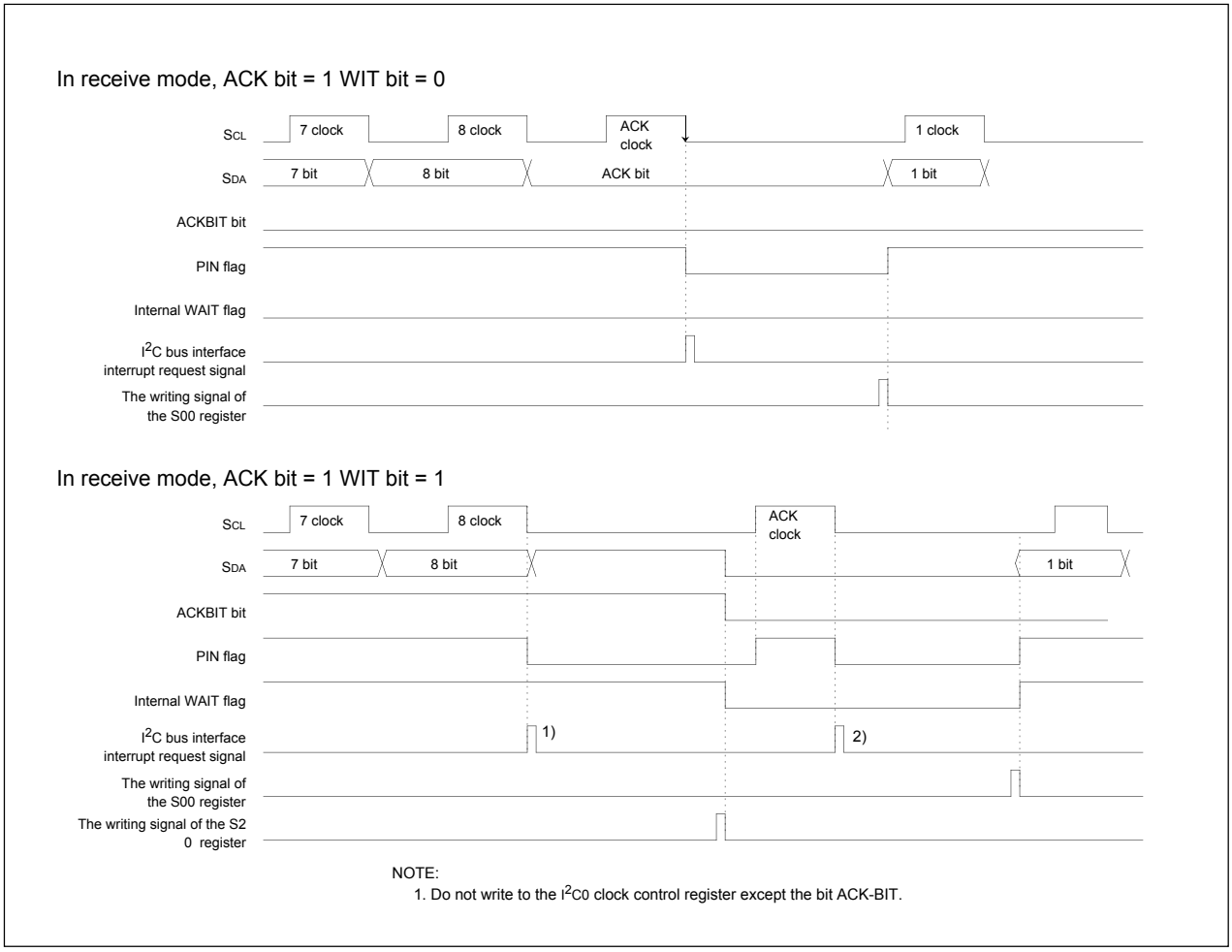


Figure 16.12 The timing of the interrupt generation at the completion of the data receive

16.6.3 Bits 2,3 : Port Function Select Bits PED, PEC

If the ES0 bit in the S1D0 register is set to 1 (I^2C bus interface enabled), the SDAMM functions as an output port. When the PED bit is set to 1 and the SCLMM functions as an output port when the PEC bit is set to 1. Then the setting values of bits P2_0 and P2_1 in the port P2 register are output to the I^2C bus, regardless of he internal SCL/SDA output signals. (SCL/SDA pins are onnected to I^2C bus interface circuit)

The bus data can be read by reading the port pi direction register in input mode, regardless of the setting values of the PED and PEC bits. **Table 16.5** shows the port specification.

Table 16.5 Port specifications

Pin Name	ES9 Bit	PED Bit	$P2_0$ Port Direction Register	Function
$P2_0$	0	-	0/1	Port I/O function
	1	0	-	SDA I/O function
	1	1	-	SDA input function, port output function
Pin Name	ES0 Bit	PEC Bit	$P2_1$ Port Direction Register	Function
$P2_1$	0	-	0/1	Port I/O function
	1	0	-	SCL I/O function
	1	1	-	SCL input function, port output funcion

18. Programmable I/O Ports

Note

Ports P04 to P07, P10 to P14 , P34 to P37 and P95 to P97 are not available in 64-pin package.

The programmable input/output ports (hereafter referred to simply as “I/O ports”) consist of 71 lines P0, P1, P2, P3, P6, P7, P8, P9, P10 (except P94) for the 80-pin package, or 55 lines P00 to P03, P15 to P17, P2, P30 to P33, P6, P7, P8, P90 to P93, P10 for the 64-pin package. Each port can be set for input or output every line by using a direction register, and can also be chosen to be or not be pulled high in sets of 4 lines.
Figures 18.1 to **18.4** show the I/O ports. **Figure 18.5** shows the I/O pins.
Each pin functions as an I/O port, a peripheral function input/output.
For details on how to set peripheral functions, refer to each functional description in this manual. If any pin is used as a peripheral function input, set the direction bit for that pin to 0 (input mode). Any pin used as an output pin for peripheral functions is directed for output no matter how the corresponding direction bit is set.

18.1 Port Pi Direction Register (PDi Register, i = 0 to 3, 6 to 10)

Figure 18.6 shows the direction registers.
This register selects whether the I/O port is to be used for input or output. The bits in this register correspond one for one to each port.

18.2 Port Pi Register (Pi Register, i = 0 to 3, 6 to 10)

Figure 18.7 shows the Pi registers.
Data input/output to and from external devices are accomplished by reading and writing to the Pi register. The Pi register consists of a port latch to hold the output data and a circuit to read the pin status. For ports set for input mode, the input level of the pin can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register.
For ports set for output mode, the port latch can be read by reading the corresponding Pi register, and data can be written to the port latch by writing to the Pi register. The data written to the port latch is output from the pin. The bits in the Pi register correspond one for one to each port.

18.3 Pull-up Control Register 0 to 2 (PUR0 to PUR2 Registers)

Figure 18.8 shows registers PUR0 to PUR2.
Registers PUR0 to PUR2 select whether the pins, divided into groups of four pins, are pulled up or not. The pins, selected by setting the bits in registers PUR0 to PUR2 to 1 (pull-up), are pulled up when the direction registers are set to 0 (input mode). The pins are pulled up regardless of the pins’ function.

18.4 Port Control Register (PCR Register)

Figure 18.9 shows the port control register.
When the P1 register is read after setting the PCR0 bit in the PCR register to 1, the corresponding port latch can be read no matter how the PD1 register is set.

19.3 Functions To Prevent Flash Memory from Rewriting

The flash memory has a built-in ROM code protect function for parallel I/O mode and a built-in ID code check function for standard input/output mode to prevent the flash memory from reading or rewriting.

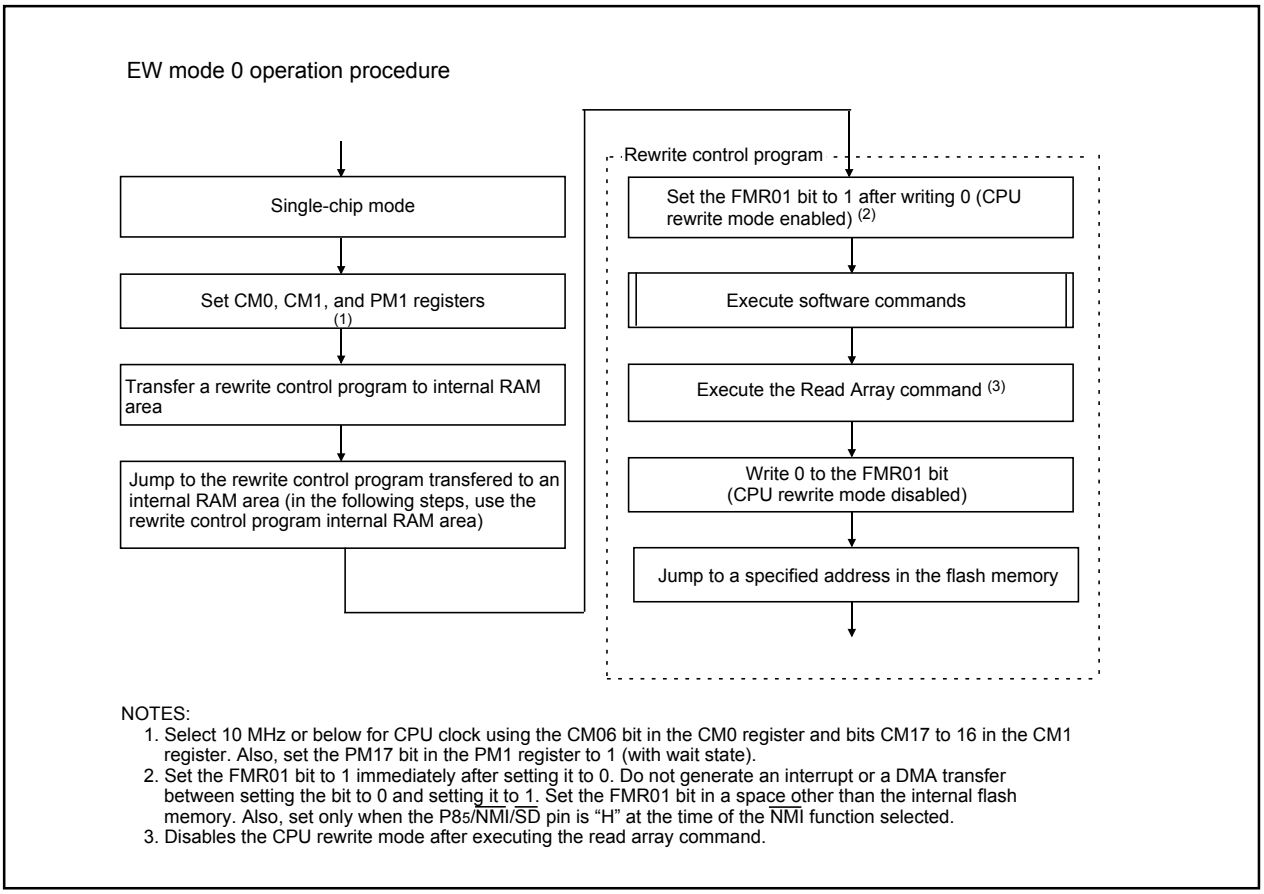
19.3.1 ROM Code Protect Function

The ROM code protect function disables reading or changing the contents of the on-chip flash memory in parallel I/O mode. **Figure 19.3** shows the ROMCP address. The ROMCP address is located in a user ROM area. To enable ROM code protect, set the ROMCP1 bit to 00_2, 01_2, or 10_2 and set the bits 5 to 0 to 111111_2.

To cancel ROM code protect, erase the block including the the ROMCP register in CPU rewrite mode or standard serial I/O mode.

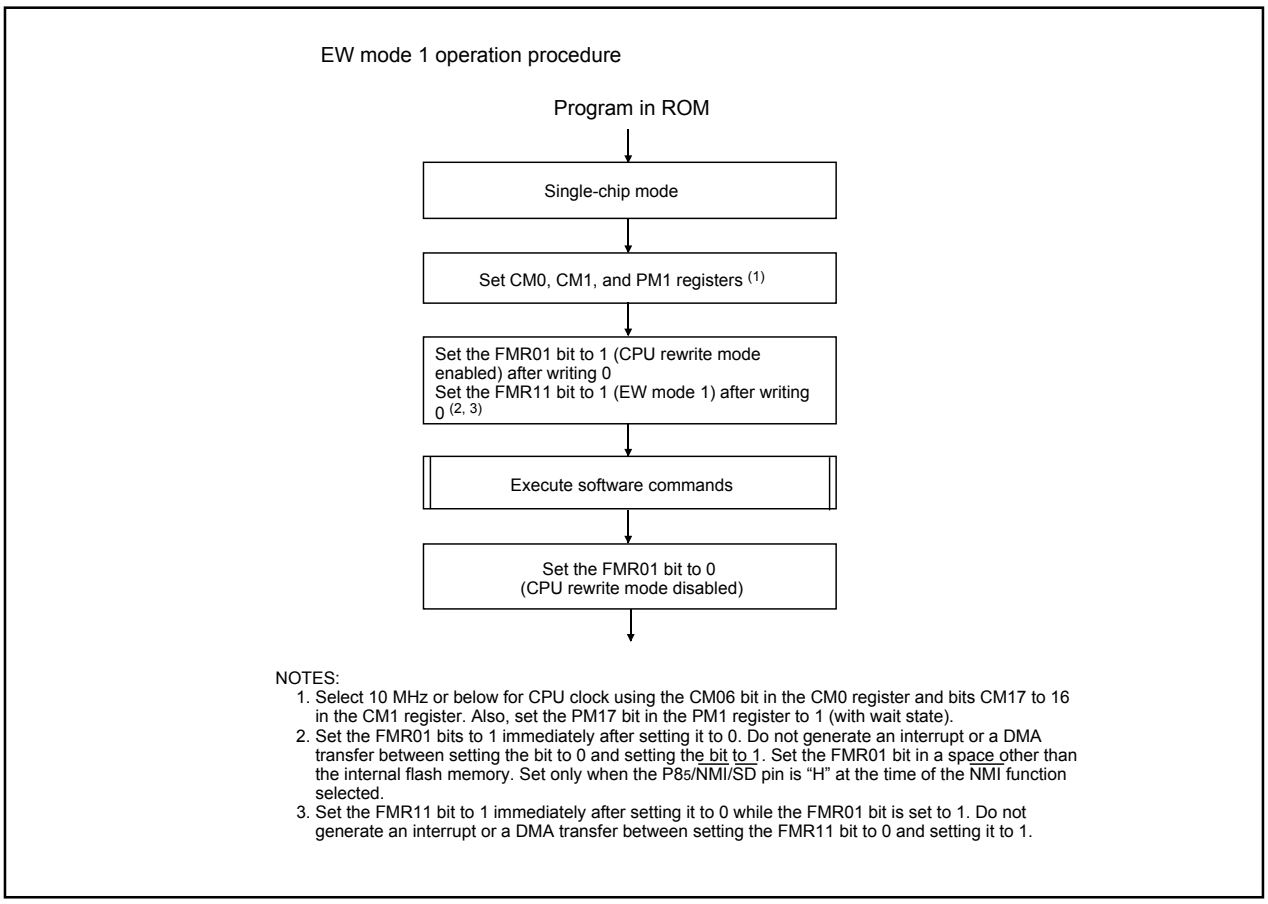
19.3.2 ID Code Check Function

Use the ID code check function in standard serial input/output mode. Unless the flash memory is blank, the ID code sent from the programmer and the 7-byte ID code written in the flash memory are compared for match. If the ID codes do not match, the commands sent from the programmer are not acknowledged. The ID code consists of 8-bit data, starting with the first byte, into addresses, $0FFFDF_{16}$, $0FFFE3_{16}$, $0FFFEB_{16}$, $0FFFEF_{16}$, $0FFFF3_{16}$, $0FFFF7_{16}$, and $0FFFFB_{16}$. The flash memory must have a program with the ID code set in these addresses.



NOTES:
1. Select 10 MHz or below for CPU clock using the CM06 bit in the CM0 register and bits CM17 to 16 in the CM1 register. Also, set the PM17 bit in the PM1 register to 1 (with wait state).
2. Set the FMR01 bit to 1 immediately after setting it to 0. Do not generate an interrupt or a DMA transfer between setting the bit to 0 and setting it to 1. Set the FMR01 bit in a space other than the internal flash memory. Also, set only when the P8$_5$/$\overline{\text{NMI}}$/$\overline{\text{SD}}$ pin is "H" at the time of the $\overline{\text{NMI}}$ function selected.
3. Disables the CPU rewrite mode after executing the read array command.

Figure 19.7 Setting and Resetting of EW Mode 0



NOTES:
1. Select 10 MHz or below for CPU clock using the CM06 bit in the CM0 register and bits CM17 to 16 in the CM1 register. Also, set the PM17 bit in the PM1 register to 1 (with wait state).
2. Set the FMR01 bits to 1 immediately after setting it to 0. Do not generate an interrupt or a DMA transfer between setting the bit to 0 and setting the bit to 1. Set the FMR01 bit in a space other than the internal flash memory. Set only when the P8$_5$/$\overline{\text{NMI}}$/$\overline{\text{SD}}$ pin is "H" at the time of the $\overline{\text{NMI}}$ function selected.
3. Set the FMR11 bit to 1 immediately after setting it to 0 while the FMR01 bit is set to 1. Do not generate an interrupt or a DMA transfer between setting the FMR11 bit to 0 and setting it to 1.

Figure 19.8 Setting and Resetting of EW Mode 1

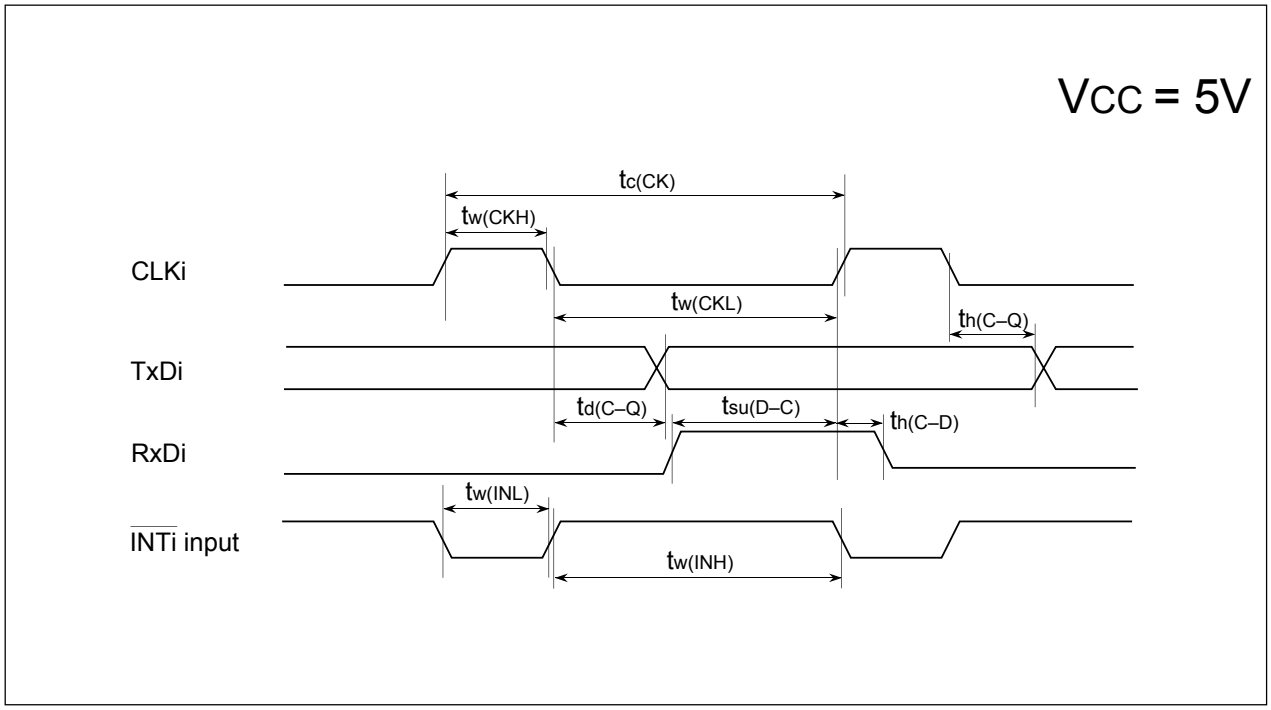


Figure 20.8 Timing Diagram (2)

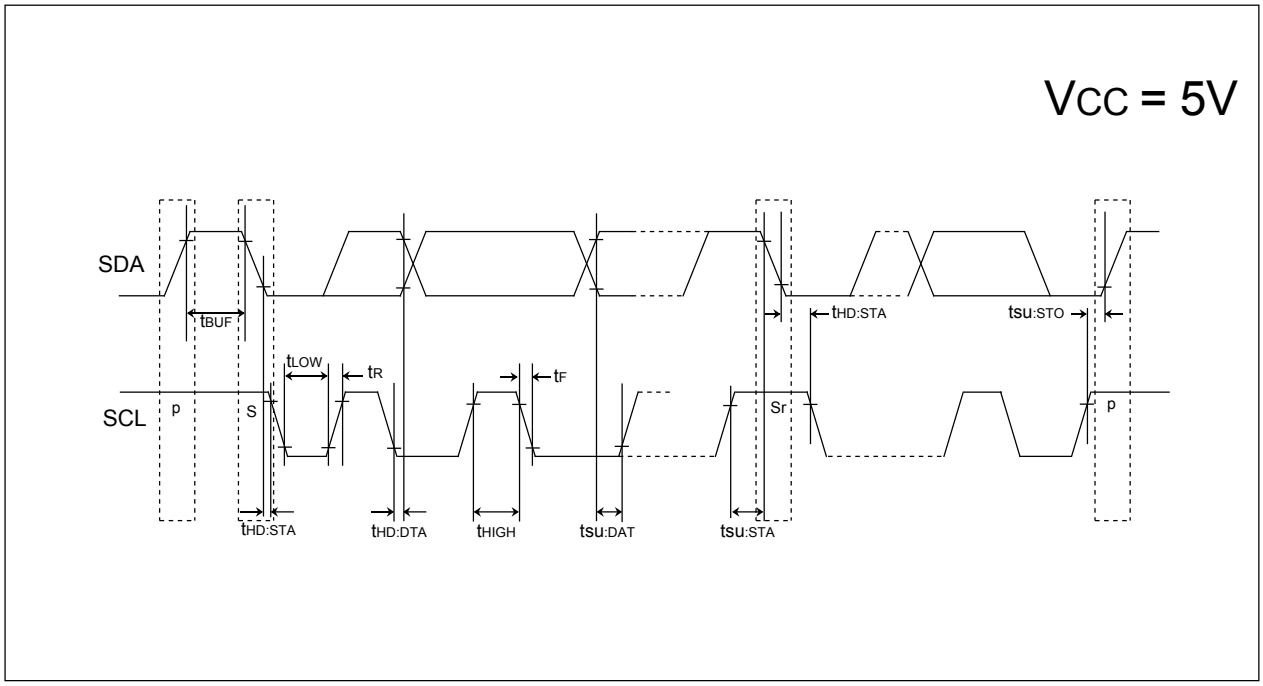


Figure 20.9 Timing Diagram (3)

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