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Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After Reset
≈			≈
01B016			
01B116			
01B216			
01B316	Flash memory control register 4 (2)	FMR4	010000002
01B416			
01B516	Flash memory control register 1 (2)	FMR1	000XXX0X2
01B616			
01B716	Flash memory control register 0 (2)	FMR0	000000012
01B816			
01B916			
≈			≈
021016	Low-power Consumption Control 0	LPCC0	X000000012
021116			
021216			
021316			
021416			
021516			
021616			
021716			
021816			
021916			
≈			≈
025016			
025116			
025216			
025316			
025416			
025516			
025616			
025716			
025816			
025916			
025A16	Three-phase protect control register	TPRC	0016
025B16			
025C16	On-chip oscillator control register	ROCR	X000010012
025D16	Pin assignment control register	PACR	0016
025E16	Peripheral clock select register	PCLKR	000000112
025F16	Low-power Consumption Control 1	LPCC1	0016
≈			≈
02E016	I2C0 data shift register	S00	XX16
02E116			
02E216	I2C0 address register	S0D0	0016
02E316	I2C0 control register 0	S1D0	0016
02E416	I2C0 clock control register	S20	0016
02E516	I2C0 start/stop condition control register	S2D0	000110102
02E616	I2C0 control register 1	S3D0	001100002
02E716	I2C0 control register 2	S4D0	0016
02E816	I2C0 status register	S10	0001000X2
02E916			
02EA16			
≈			≈
02FE16			
02FF16			

Note 1:The blank spaces are reserved. No access is allowed.
Note 2:This register is included in the flash memory version.

X : Undefined

5. Reset

Hardware reset 1, software reset, watchdog timer reset, and oscillation stop detection reset are implemented to reset the MCU.

5.1 Hardware Reset

5.1.1 Hardware Reset 1

Pins, CPU, and SFRs are reset by using the $\overline{\text{RESET}}$ pin. When a low-level (“L”) signal is applied to the $\overline{\text{RESET}}$ pin while the supply voltage meets the recommended operating condition, pins, CPU, and SFRs are reset (see **Table 5.1** Pin Status When $\overline{\text{RESET}}$ Pin Level is “L”). The oscillation circuit is also reset and the on-chip oscillator starts oscillating as the CPU clock. CPU and SFRs re reset when the signal applied to the $\overline{\text{RESET}}$ pin changes from “L” to high (“H”). The MCU executes a program beginning with the address indicated by the reset vector. The internal RAM is not reset. When an “L” signal is applied to the $\overline{\text{RESET}}$ pin while writing data to the internal RAM, the content of internal RAM is undefined.
Figure 5.1 shows an example of the reset circuit. **Figure 5.2** shows a reset sequence. **Table 5.1** shows status of the other pins while the $\overline{\text{RESET}}$ pin is held “L”. **Figure 5.3** shows CPU register states after reset. Refer to **4. Special Function Register (SFR)** about SFR states after reset.

1. Reset on a stable supply voltage
(1) Apply an “L” signal to the $\overline{\text{RESET}}$ pin
(2) Wait *td(ROC)* or more
(3) Apply an “H” signal to the $\overline{\text{RESET}}$ pin

2. Power-on reset
(1) Apply an “L” signal to the $\overline{\text{RESET}}$ pin
(2) Increase the supply voltage until it meets the the recommended performance condition
(3) Wait for *td(P-R)* or more to allow the internal power supply to stabilize
(4) Wait *td(ROC)* or more
(5) Apply an “H” signal to the $\overline{\text{RESET}}$ pin

6. Processor Mode

The MCU supports single-chip mode only. **Figures 6.1** and **6.2** show the associated registers.

Processor Mode Register 0 (1)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0		0	0	0

Symbol	Address	After Reset
PM0	0004$_{16}$	00$_{16}$

Bit Symbol	Bit Name	Function	RW
$\overline{(b2\text{-}b0)}$	Reserved bit	Set to 0	RW
PM03	Software reset bit	The MCU is reset when this bit is set to 1. When read, its content is 0.	RW
$\overline{(b7\text{-}b4)}$	Reserved bit	Set to 0	RW

NOTE:
1. Set the PM0 register after the PRC1 bit in the PRCR register is set to 1 (write enable).

Processor Mode Register 1 (1)

b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	1		0	

Symbol	Address	After Reset
PM1	0005$_{16}$	00001000$_2$

Bit Symbol	Bit Name	Function	RW
PM10	Flash data block access bit (2)	0: Disabled 1: Enabled (3)	RW
$\overline{(b1)}$	Reserved bit	Set to 0	RW
PM12	Watchdog timer function select bit	0 : Watchdog timer interrupt 1 : Watchdog timer reset (4)	RW
$\overline{(b3)}$	Reserved bit	Set to 1	RW
$\overline{(b6\text{-}b4)}$	Reserved bit	Set to 0	RW
PM17	Wait bit (5)	0 : No wait state 1 : Wait state (1 wait)	RW

NOTES:
1. Rewrite the PM1 register after the PRC1 bit in the PRCR register is set to 1 (write enable).
2. To access the two 2K-byte data spaces in data block A and data block B, set the PM10 bit to 1. The PM10 bit is not available in mask version.
3. When the FMR01 bit in the FMR0 register is set to 1 (enables CPU rewrite mode), the PM10 bit is automatically set to 1.
4. Set the PM12 bit to 1 by program. (Writing 0 by program has no effect)
5. When the PM17 bit is set to 1 (wait state), one wait is inserted when accessing the internal RAM or the internal ROM.

Figure 6.1 PM0 Register, PM1 Register

System Clock Control Register 1 (1)

b7	b6	b5	b4	b3	b2	b1	b0
			0	0	0		

Symbol	Address	After Reset
CM1	0007$_{16}$	00100000$_2$

Bit Symbol	Bit Name	Function	RW
CM10	All clock stop control bit (4, 6)	0 : Clock on 1 : All clocks off (stop mode)	RW
CM11	System clock select bit 1 (6, 7)	0 : Main clock 1 : PLL clock (5)	RW
$\overline{\text{(b4-b2)}}$	Reserved bit	Set to 0	RW
CM15	XIN-XOUT drive capacity select bit (2)	0 : LOW 1 : HIGH	RW
CM16	Main clock division select bits (3)	b7 b6 0 0 : No division mode 0 1 : Division by 2 mode 1 0 : Division by 4 mode 1 1 : Division by 16 mode	RW
CM17			RW

NOTES:
1. Write to this register after setting the PRC0 bit in the PRCR register to 1 (write enable).
2. When entering stop mode from high or middle speed mode, or when the CM05 bit is set to 1 (main clock turned off) in low speed mode, the CM15 bit is set to 1 (drive capability high).
3. Effective when the CM06 bit is 0 (bits CM16 and CM17 enable).
4. If the CM10 bit is 1 (stop mode), XOUT goes "H" and the internal feedback resistor is disconnected. The XCIN and XCOUT pins are placed in the high-impedance state. When the CM11 bit is set to 1 (PLL clock), or the CM20 bit in the CM2 register is set to 1 (oscillation stop, re-oscillation detection function enabled), do not set the CM10 bit to 1.
5. After setting the PLC07 bit in the PLC0 register to 1 (PLL operation), wait until tsu (PLL) elapses before setting the CM11 bit to 1 (PLL clock).
6. When the PM21 bit in the PM2 register is set to 1 (clock modification disable), writing to bits CM10, CM11 has no effect. When the PM22 bit in the PM2 register is set to 1 (watchdog timer count source is on-chip oscillator clock), writing to the CM10 bit has no effect.
7. Effective when CM07 bit is 0 and CM21 bit is 0 .

Figure 7.3 CM1 Register

On-chip Oscillator Control Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
X	0	0	0				

Symbol	Address	After Reset
ROCR	025C$_{16}$	X00001012

Bit Symbol	Bit Name	Function	RW
ROCR0	Frequency select bits	b1 b0 0 0: f1 (ROC) 0 1: f2 (ROC) 1 0: Do not set to this value 1 1: f3 (ROC)	RW
ROCR1			RW
ROCR2	Divider select bits	b3 b2 0 0: Do not set to this value 0 1: divide by 2 1 0: divide by 4 1 1: divide by 8	RW
ROCR3			RW
$\overline{\text{(b6-b4)}}$	Reserved bit	Set to 0	RW
$\overline{\text{(b7)}}$	Nothing is assigned. When write, set to 0. When read, the content is undefined		—

NOTE:
1. Write to this register after setting the PRC0 bit in the PRCR register to 1 (write enable).

Figure 7.4 ROCR Register

Table 11.1 DMAC Specifications

Item		Specification
No. of channels		2 (cycle steal method)
Transfer memory space		• From any address in the 1M bytes space to a fixed address • From a fixed address to any address in the 1M bytes space • From a fixed address to a fixed address
Maximum No. of bytes transferred		128K bytes (with 16-bit transfers) or 64K bytes (with 8-bit transfers)
DMA request factors (1, 2)		Falling edge of $\overline{INT0}$ or $\overline{INT1}$ Both edge of $\overline{INT0}$ or $\overline{INT1}$ Timer A0 to timer A4 interrupt requests Timer B0 to timer B2 interrupt requests UART0 transfer, UART0 reception interrupt requests UART1 transfer, UART1 reception interrupt requests UART2 transfer, UART2 reception interrupt requests SI/O3, SI/O4 interrupt requests A/D conversion interrupt requests Timer S(IC/OC) requests Software triggers
Channel priority		DMA0 > DMA1 (DMA0 takes precedence)
Transfer unit		8 bits or 16 bits
Transfer address direction		forward or fixed (The source and destination addresses cannot both be in the forward direction)
Transfer mode	Single transfer	Transfer is completed when the DMAi transfer counter (i = 0,1) underflows after reaching the terminal count
	Repeat transfer	When the DMAi transfer counter underflows, it is reloaded with the value of the DMAi transfer counter reload register and a DMA transfer is con tinued with it
DMA interrupt request generation timing		When the DMAi transfer counter underflowed
DMA startup the		Data transfer is initiated each time a DMA request is generated when DMAE bit in the DMAiCON register = 1 (enabled)
DMA shutdown	Single transfer	• When the DMAE bit is set to 0 (disabled) • After the DMAi transfer counter underflows
	Repeat transfer	When the DMAE bit is set to 0 (disabled)
Reload timing for forward address pointer and transfer counter		When a data transfer is started after setting the DMAE bit to 1 (en abled), the forward address pointer is reloaded with the value of the SARi or the DARi pointer whichever is specified to be in the forward direction and the DMAi transfer counter is reloaded with the value of the DMAi transfer counter reload register

NOTES:

1. DMA transfer is not effective to any interrupt. DMA transfer is affected neither by the I flag nor by the interrupt control register.
2. The selectable causes of DMA requests differ with each channel.
3. Make sure that no DMAC-related registers (addresses 0020_{16} to $003F_{16}$) are accessed by the DMAC.

14. Serial I/O

Note

The SI/O4 interrupt of peripheral function interrupt is not available in the 64-pin package.

Serial I/O is configured with five channels: UART0 to UART2, SI/O3 and SI/O4.

14.1 UARTi (i=0 to 2)

UARTi each have an exclusive timer to generate a transfer clock, so they operate independently of each other.

Figure 14.1 shows the block diagram of UARTi. **Figures 14.2** and **14.3** shows the block diagram of the UARTi transmit/receive.

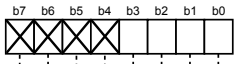
UARTi has the following modes:

- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode).
- Special mode 1 (I^2C bus mode): UART2
- Special mode 2: UART2
- Special mode 3 (Bus collision detection function, IEBus mode): UART2
- Special mode 4 (SIM mode): UART2

Figures 14.4 to **14.9** show the UARTi-associated registers.

Refer to **Tables 14.2, 14.6, 14.11, 14.12, 14.16, 14.17**, and **14.19** to set the registers in individual mode.

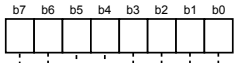
UARTi Transmit/receive Control Register 1 (i=0, 1)



Symbol: U0C1, U1C1 | Address: 03A5$_{16}$,03AD$_{16}$ | After Reset: 00000010$_2$

Bit Symbol	Bit Name	Function	RW
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	RW
TI	Transmit buffer empty flag	0 : Data present in UiTB register 1 : No data present in UiTB register	RO
RE	Receive enable bit	0 : Reception disabled 1 : Reception enabled	RW
RI	Receive complete flag	0 : No data present in UiRB register 1 : Data present in UiRB register	RO
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

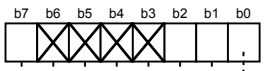
UART2 Transmit/receive Control Register 1



Symbol: U2C1 | Address: 037D$_{16}$ | After Reset: 00000010$_2$

Bit Symbol	Bit Name	Function	RW
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	RW
TI	Transmit buffer empty flag	0 : Data present in U2TB register 1 : No data present in U2TB register	RO
RE	Receive enable bit	0 : Reception disabled 1 : Reception enabled	RW
RI	Receive complete flag	0 : No data present in U2RB register 1 : Data present in U2RB register	RO
U2IRS	UART2 transmit interrupt cause select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmit is completed (TXEPT = 1)	RW
U2RRM	UART2 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enabled	RW
U2LCH	Data logic select bit	0 : No reverse 1 : Reverse	RW
U2ERE	Error signal output enable bit	0 : Output disabled 1 : Output enabled	RW

Pin Assignment Control Register (1)



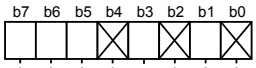
Symbpl: PACR | Address: 025D$_{16}$ | After Reset: 00$_{16}$

Bit Symbol	Bit Name	Function	RW
PACR0	Pin enabling bit	010 : 64 pin 011 : 80 pin All other values are reserved. Do not use.	RW
PACR1			RW
PACR2			RW
— (b6-b3)	Reserved bits	Nothing is assigned. If necessary, set to 0. When read, the content is 0	—
U1MAP	UART1 pin remapping bit	UART1 pins assigned to 0 : P67 to P6$_4$ 1 : P7$_3$ to P7$_0$	RW

NOTE:
1. Set the PACR register by the next instruction after setting the PRC2 bit in the PRCR register to 1(write enable).

Figure 14.7 U0C1 to U2C1 Register, and PACR Register

UART2 Special Mode Register 3

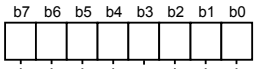


Symbol	Address	After Reset
U2SMR3	037516	$000X0X0X2$

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—
CKPH	Clock phase set bit	0 : Without clock delay 1 : With clock delay	RW
— (b2)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—
NODC	Clock output select bit	0 : CLK_2 is CMOS output 1 : CLK_2 is N-channel open drain output	RW
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined		—
DL0	SDA2 digital delay setup bit (1, 2)	b7 b6 b5 0 0 0 : Without delay 0 0 1 : 1 to 2 cycle(s) of U2BRG count source 0 1 0 : 2 to 3 cycles of U2BRG count source 0 1 1 : 3 to 4 cycles of U2BRG count source 1 0 0 : 4 to 5 cycles of U2BRG count source 1 0 1 : 5 to 6 cycles of U2BRG count source 1 1 0 : 6 to 7 cycles of U2BRG count source 1 1 1 : 7 to 8 cycles of U2BRG count source	RW
DL1			RW
DL2			RW

NOTES:
1. Bits DL2 to DL0 are used to generate a delay in SDA output by digital means during I^2C bus mode. In other than I^2C bus mode, set these bits to 000_2 (no delay).
2. The amount of delay varies with the load on pins SCL2 and SDA2. Also, when using an external clock, the amount of delay increases by about 100 ns.

UART2 Special Mode Register 4



Symbol	Address	After Reset
U2SMR4	037416	0016

Bit Symbol	Bit Name	Function	RW
STAREQ	Start condition generate bit (1)	0 : Clear 1 : Start	RW
RSTAREQ	Restart condition generate bit (1)	0 : Clear 1 : Start	RW
STPREQ	Stop condition generate bit (1)	0 : Clear 1 : Start	RW
STSPSEL	SCL_2,SDA_2 output select bit	0 : Start and stop conditions not output 1 : Start and stop conditions output	RW
ACKD	ACK data bit	0 : ACK 1 : NACK	RW
ACKC	ACK data output enable bit	0 : Serial I/O data output 1 : ACK data output	RW
SCLHI	SCL_2 output stop enable bit	0 : Disabled 1 : Enabled	RW
SWC9	SCL_2 wait bit 3	0 : SCL_2 “L” hold disabled 1 : SCL_2 “L” hold enabled	RW

NOTE:
1. Set to 0 when each condition is generated.

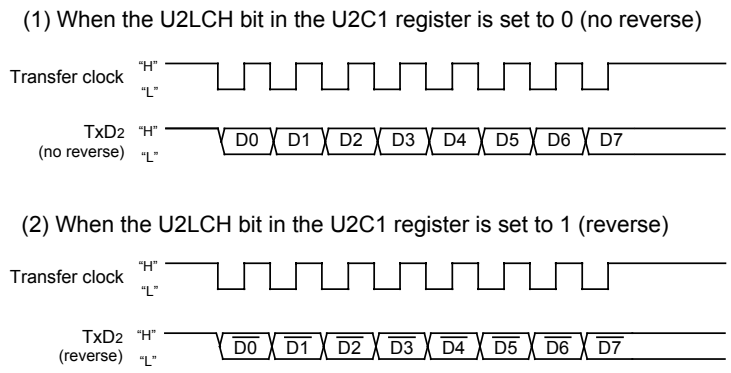
Figure 14.9 U2SMR3 and U2SMR4 Registers

14.1.1.4 Continuous receive mode

When the UiRRM bit (i=0 to 2) is set to 1 (continuous receive mode), the TI bit in the UiC1 register is set to “0” (data present in the UiTB register) by reading the UiRB register. In this case, i.e., UiRRM bit is set to 1, do not write dummy data to the UiTB register in a program. The U0RRM and U1RRM bits are the bit 2 and bit 3 in the UCON register, respectively, and the U2RRM bit is the bit 5 in the U2C1 register.

14.1.1.5 Serial data logic switch function (UART2)

When the U2LCH bit in the U2C1 register is set to 1 (reverse), the data written to the U2TB register has its logic reversed before being transmitted. Similarly, the received data has its logic reversed when read from the U2RB register. **Figure 14.13** shows serial data logic.

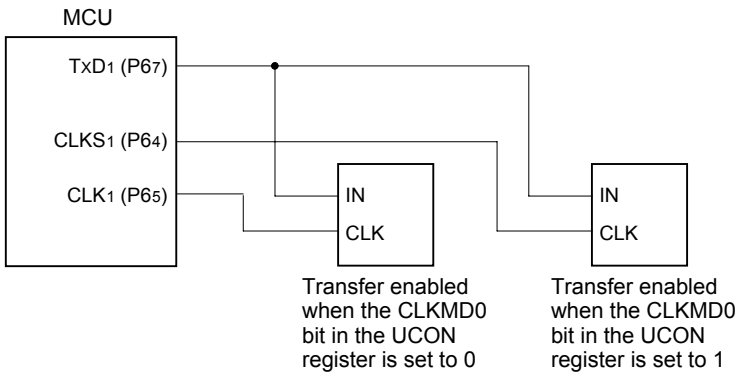


NOTE:
1. This applies to the case where the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and the receive data taken in at the rising edge of the transfer clock) and the UFORM bit is set to 0 (LSB first).

Figure 14.13 Serial data logic switch timing

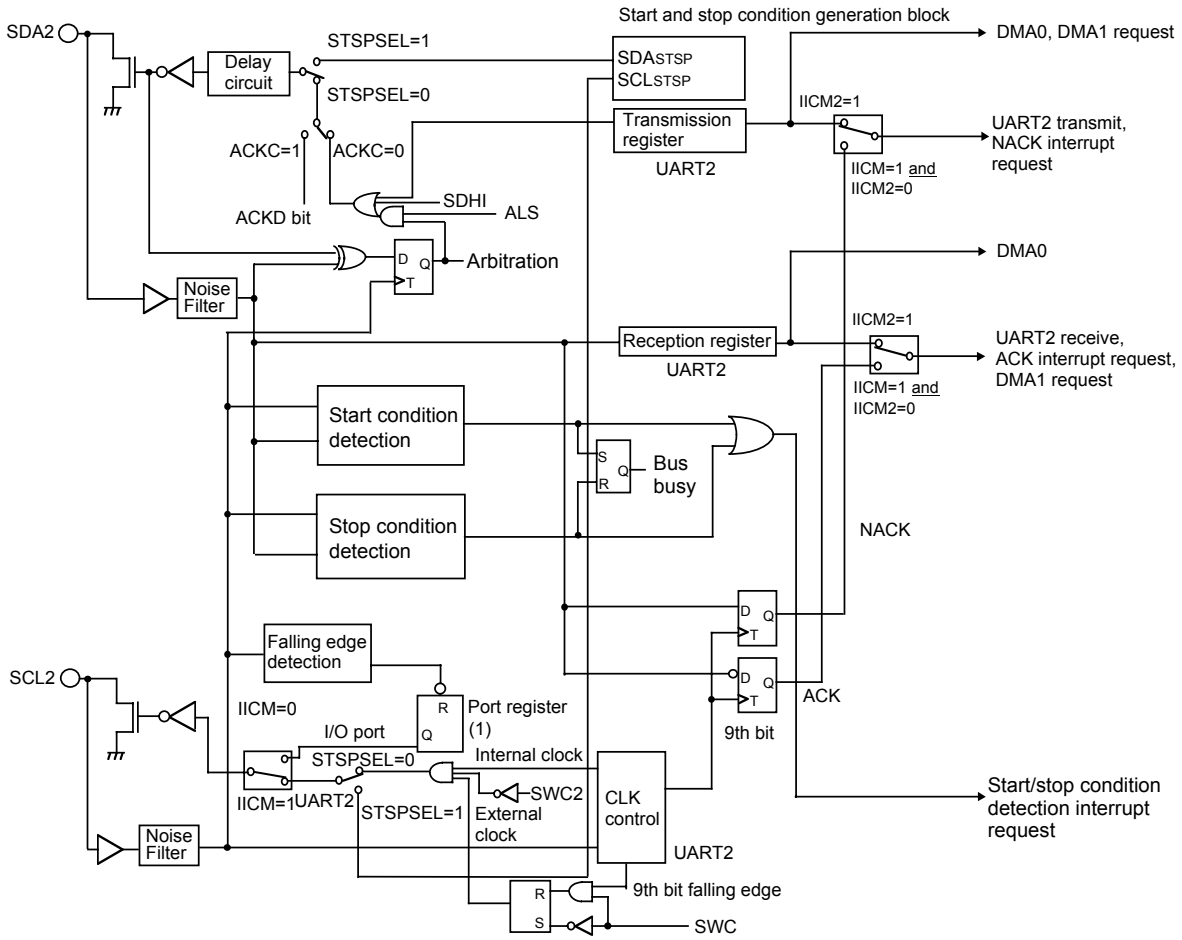
14.1.1.6 Transfer clock output from multiple pins function (UART1)

The CLKMD1 to CLKMD0 bits in the UCON register can choose one from two transfer clock output pins. (See **Figure 14.14**) This function is valid when the internal clock is selected for UART1.



NOTES:
1. This applies to the case where the CKDIR bit in the U1MRregister is set to 0 (internal clock) and the CLKMD1 bit in the UCON register is set to 1 (transfer clock output from multiple pins).
2. This applies to the case where U1MAP bit in PACR register is set to 0 (P67 to P64).

Figure 14.14 Transfer Clock Output From Multiple Pins



This diagram applies to the case where bits SMD2 to SMD0 in the U2MR register is set to 010$_2$ and the IICM bit in the U2SMR register is set to 1.

IICM: Bit in the U2SMR register
IICM2, SWC, ALS, SWC2, SDHI: Bits in the U2SMR2 register
STSPSEL, ACKD, ACKC: Bits in the U2SMR4 register

NOTE:
1. If the IICM bit is set to 1, the pin can be read even when the PD7_1 bit is set to 1 (output mode).

Figure 14.22 I^{2}C bus Mode Block Diagram

14.1.3.7 ACK and NACK

If the STSPSEL bit in the U2SMR4 register is set to 0 (start and stop conditions not generated) and the ACKC bit in the U2SMR4 register is set to 1 (ACK data output), the value of the ACKD bit in the U2SMR4 register is output from the SDA_2 pin.

If the IICM2 bit is set to 0, a NACK interrupt request is generated if the SDA_2 pin remains high at the rising edge of the 9th bit of transmit clock pulse. An ACK interrupt request is generated if the SDA_2 pin is low at the rising edge of the 9th bit of transmit clock pulse.

If ACK2 is selected for the cause of DMA1 request, a DMA transfer can be activated by detection of an acknowledge.

14.1.3.8 Initialization of Transmission/Reception

If a start condition is detected while the STAC bit is set to 1 (UART2 initialization enabled), the serial I/O operates as described below.

- The transmit shift register is initialized, and the content of the U2TB register is transferred to the transmit shift register. In this way, the serial I/O starts sending data synchronously with the next clock pulse applied. However, the UART2 output value does not change state and remains the same as when a start condition was detected until the first bit in the data is output synchronously with the input clock.
- The receive shift register is initialized, and the serial I/O starts receiving data synchronously with the next clock pulse applied.
- The SWC bit is set to 1 (SCL_2 wait output enabled). Consequently, the SCL_2 pin is pulled low at the falling edge of the ninth clock pulse.

Note that when UART2 transmission/reception is started using this function, the TI does not change state. Note also that when using this function, the selected transfer clock should be an external clock.

A/D Trigger Control Register (1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	0		1	1

Symbol	Address	After Reset
ADTRGCON	$03D2_{16}$	00_{16}

Bit Symbol	Bit Name	Function	RW
SSE	A/D operation mode select bit 2	1: Simultaneous sample sweep mode or delayed trigger mode 0, 1	RW
DTE	A/D operation mode select bit 3	0: Other than delayed trigger mode 0, 1	RW
HPTRG0	AN0 trigger select bit	See **Table 15.9**	RW
HPTRG1	AN1 trigger select bit	Set to 0 in simultaneous sample sweep mode	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0		—

NOTE:
1. If ADTRGCON is rewritten during A/D conversion, the conversion result will be undefined.

Figure 15.18 ADTRGCON Register in Simultaneous Sample Sweep Mode

Table 15.9 Trigger Select Bit Setting in Simultaneous Sample Sweep Mode

TRG	TRG1	HPTRG0	TRIGGER
0	-	-	Software trigger
1	-	1	Timer B0 underflow (1)
1	0	0	$\overline{\text{ADTRG}}$
1	1	0	Timer B2 or Timer B2 interrupt generation frequency setting counter underflow (2)

NOTES:
1. A count can be started for Timer B2, Timer B2 interrupt generation frequency setting counter underflow or the INT5 pin falling edge as count start conditions of Timer B0.
2. Select Timer B2 or Timer B2 interrupt generation frequency setting counter using the TB2SEL bit in the TB2SC register.

16. Multi-master I2C bus Interface

The multi-master I2C bus interface is a serial communication circuit based on Philips I2C bus data transfer format, equipped with arbitration lost detection and synchronous functions. **Figure 16.1** shows a block diagram of the multi-master I2C bus interface and **Table 16.1** lists the multi-master I2C bus interface functions.

The multi-master I2C bus interface consists of the S0D0 register, the S00 register, the S20 register, the S3D0 register, the S4D0 register, the S10 register, the S2D0 register and other control circuits.

Figures 16.2 to **16.8** show the registers associated with the multi-master I2C bus.

Table 16.1 Multi-master I2C bus interface functions

Item	Function
Format	Based on Philips I2C bus standard: 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	Based on Philips I2C bus standard: Master transmit Master receive Slave transmit Slave receive
SCL clock frequency	16.1kHz to 400kHz (at VIIC (1)= 4MHz)
I/O pin	Serial data line SDAMM(SDA) Serial clock line SDLMM(SCL)

NOTE:

1. VIIC=I2C system clock

16.5 I2C0 Status Register (S10 register)

The S10 register monitors the I2C bus interface status. When using the S10 register to check the status, use the 6 low-order bits for read only.

16.5.1 Bit 0: Last Receive Bit (LRB)

The LRB bit stores the last bit value of received data. It can also be used to confirm whether ACK is received. If the ACK-CLK bit in the S20 register is set to 1 (with ACK clock) and ACK is returned when the ACK clock is generated, the LRB bit is set to 0. If ACK is not returned, the LRB bit is set to 1. When the ACK-CLK bit is set to 0 (no ACK clock), the last bit value of received data is input. When writing data to the S00 register, the LRB bit is set to 0.

16.5.2 Bit 1: General Call Detection Flag (ADR0)

When the ALS bit in the S1D0 register is set to 0 (addressing format), this ADR0 flag is set to 1 by receiving the general calls(1),whose address data are all 0, in slave mode.
The ADR0 flag is set to 0 when STOP or START conditions is detected or when the IHR bit in the S1D0 register is set to 1 (reset).

NOTE:
1. General call: A master device transmits the general call address 00_{16} to all slaves. When the master device transmits the general call, all slave devices receive the controlled data after general call.

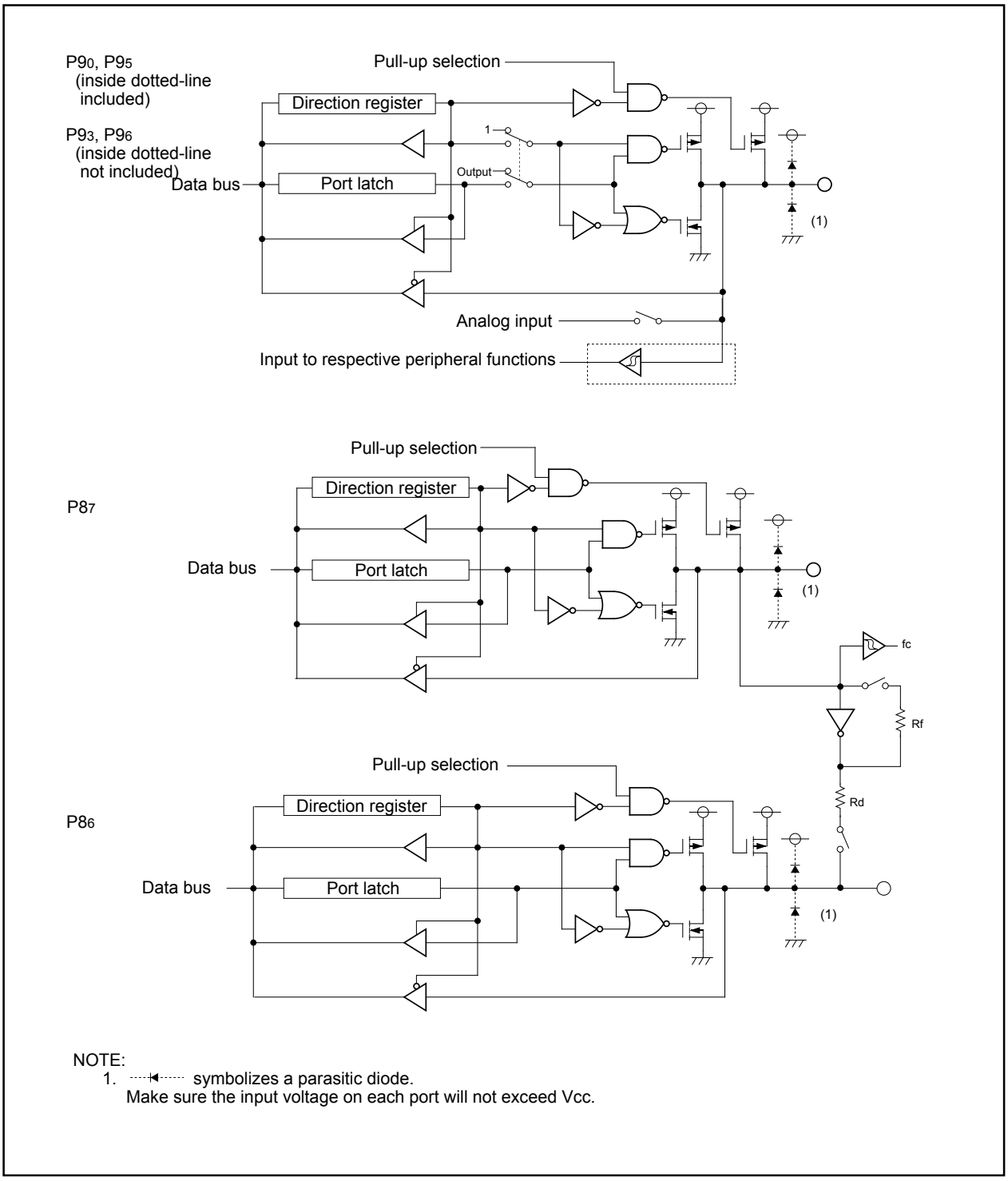
16.5.3 Bit 2: Slave Address Comparison Flag (AAS)

The AAS flag indicates a comparison result of the slave address data after enabled by setting the ALS bit in the S1D0 register to 0 (addressing format).
The AAS flag is set to 1 when the 7 bits of the address data are matched with the slave address stored into the S0D0 register, or when a general call is received, in slave receive mode. The AAS flag is set to 0 by writing data to the S00 register. When the ES0 bit in the S1D0 register is set to 0 (I2C bus interface disabled) or when the IHR bit in the S1D0 register is set to 1 (reset), the AAS flag is also set to 0.

16.5.4 Bit 3: Arbitration Lost Detection Flag (AL)(1)

In master transmit mode, if an "L" signal is applied to the SDA pin by other than the MCU, the AL flag is set to 1 by determining that the arbitration is los and the TRX bit in the S10 register is set to 0 (receive mode) at the same time. The MST bit in the S10 register is set to 0 (slave mode) after transferring the bytes which lost the arbitration.
The arbitration lost can be detected only in master transmit mode. When writing data to the S00 register, the AL flag is set to 0. When the ES0 bit in the S1D0 register is set to 0 (I2C bus interface disabled) or when the IHR bit in the S1D0 register is set to 1 (reset), the AL flag is set to 0.

NOTE:
1. Arbitration lost: communication disabled as a master

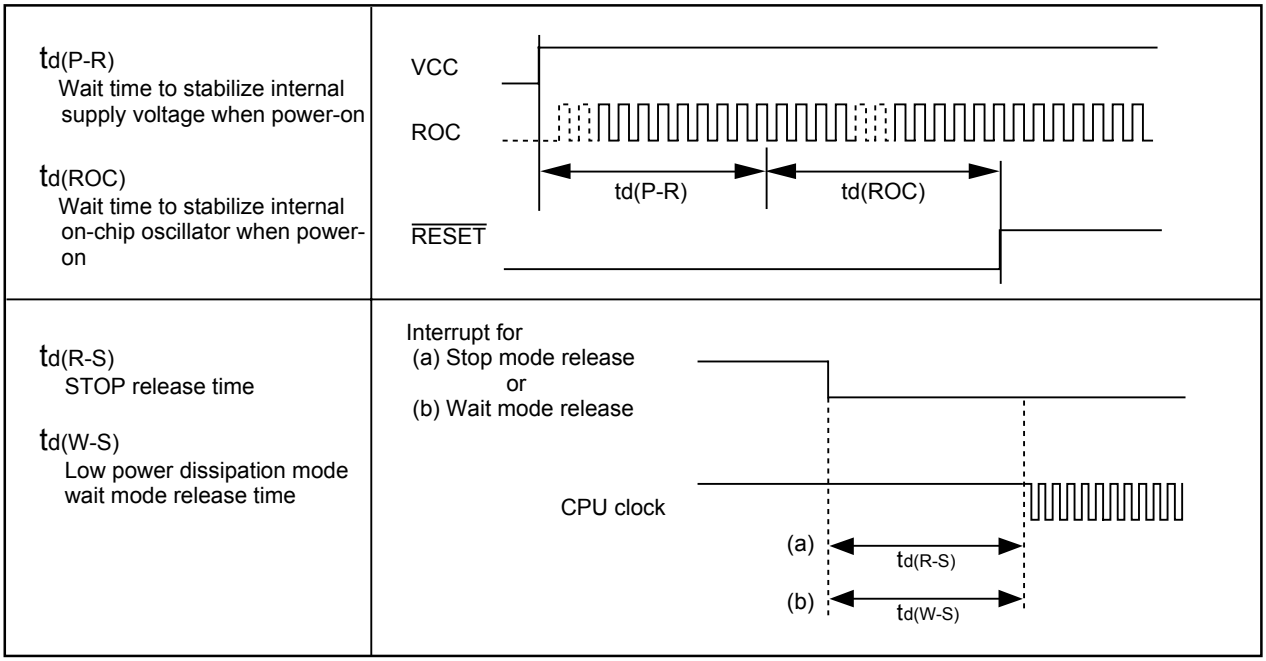


NOTE:
1. ⋯◂⋯ symbolizes a parasitic diode.
Make sure the input voltage on each port will not exceed Vcc.

Figure 18.4 I/O Ports (4)

Table 20.44 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	V_{CC}=4.2 to 5.5V			2	ms
td(ROC)	Wait Time to Stabilize Internal On-chip Oscillator when Power-on				40	µs
td(S-R)	STOP Release Time				150	µs
td(W-S)	Low Power Dissipation Mode Wait Mode Release Time				150	µs



21.6.1.3 Timer A (One-shot Timer Mode)

1. The timer remains idle after reset. Set the mode, count source, counter value, etc. using the TAiMR (i = 0 to 4) register, the TAi register, bits TA0TGL and TA0TGH in the ONSF register and the TRGSR register before setting the TAiS bit in the TABSR register to 1 (count starts).
   Always make sure bits TA0TGL and TA0TGH in the TAiMR register, the ONSF register, and the TRGSR register are modified while the TAiS bit remains 0 (count stops) regardless whether after reset or not.

2. When setting TAiS bit to 0 (count stop), the followings occur:
   • A counter stops counting and a content of reload register is reloaded.
   • TAiOUT pin outputs "L".
   • After one cycle of the CPU clock, the IR bit in TAiIC register is set to 1 (interrupt request).

3. Output in one-shot timer mode synchronizes with a count source internally generated. When the external trigger has been selected, a maximun delay of one cycle of the count source occurs between the trigger input to TAiIN pin and output in one-shot timer mode.

4. The IR bit is set to 1 when timer operation mode is set with any of the following procedures:
   • Select one-shot timer mode after reset.
   • Change an operation mode from timer mode to one-shot timer mode.
   • Change an operation mode from event counter mode to one-shot timer mode.
   To use the timer Ai interrupt (the IR bit), set the IR bit to 0 after the changes listed above have been made.

5. When a trigger occurs while the timer is counting, the counter reloads the reload register value, and continues counting after a second trigger is generated and the counter is decremented once. To generate a trigger while counting, space more than one cycle of the timer count source from the first trigger and generate again.

6. When selecting the external trigger for the count start conditions in timer A one-shot timer mode, do not generate an external trigger 300ns before the count value of timer A is set to 0000_{16}. The one-shot timer may stop counting.

7. If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is set to 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the TA1OUT, TA2OUT and TA4OUT pins go to a high-impedance state.

21.7.2 Rewrite the ICOCiIC Register

When the interrupt request to the ICOCiIC register is generated during the instruction process, the IR bit may not be set to 1 (interrupt requested) and the interrupt request may not be acknowledged. At that time, when the bit in the G1IR register is held to 1 (interrupt requested), the following IC/OC interrupt request will not be generated. When changing the ICOCiIC register settiing, use the following instruction.

Subject instructions: AND, OR, BCLR, BSET

When initializing Timer S, change the ICOCiIC register setting with the request again after setting the IOCiIC and G1IR registers to 00_{16}.

21.7.3 Waveform Generating Function

1. If the BTS bit in the G1BCR1 register is set to 0 (base timer is reset) when the waveform is generating and the base timer is stopped counting, the waveform output pin keeps the same output level. The output level will be changed when the base timer and the G1POj register match the setting value next time after the base timer starts counting again.
2. If the G1POCRj register is set when the waveform is generated, the same setting value of the IVL bit is applied to the waveform generating pin. Do not set the G1POCRj register when the waveform is generating.
3. When the RST1 bit in the G1BCR1 register is set to 1 (the base timer is reset by matching the G1PO0 register), the base timer is reset after two clock cycles of f_{BT1} when the base timer value matches the G1PO0 register value. A high-level ("H") signal is applied to the OUTC10 pin between the base timer value match to the base timer reset.

21.7.4 IC/OC Base Timer Interrupt

If the MCU is operated in the combination selected from Tabl e 1 for use when the RST4 bit in the G1BCR0 register is set to 1 (reset the base timer that matches the G1BTRR register) to reset the base timer, an IC/OC base timer interrupt request is generated twice.

Table 21.1 Uses of IT Bit in the G1BCR0 Register and G1BTRR Register

IT Bit in the G1BCR0 Register	G1BTRR Register
0 (bit 15 in the base timer overflows)	$07FFF_{16}$ to $0FFFE_{16}$
1 (bit 14 in the base timer overflows)	$03FFF_{16}$ to $0FFFE_{16}$ or $0BFFF_{16}$ to $0FFFE_{16}$

The second IC/OC base timer interrupt request is generated because the base timer overflow request is generated after one fBT1 clock cycle as soon as the base timer is reset.

One of the following conditions must be met in order not to generate the IC/OC base timer interrupt request twice:

1) When the RST4 bit is set to 1, set the G1BTRR register with a combination other than what is listed in **Table 21.1**.
2) Do not reset the base timer by matching the G1BTRR register. Reset the base timer by matching the G1P00 register. In other words, do not set the RST4 bit to 1 to reset the base timer. Set the RST1 bit in the G1BCR1 register to 1 (reset the base timer that matches the G1P00 register).

21.11 Programmable I/O Ports

1. If a low-level signal is applied to the $\overline{SD}$ pin when the IVPCR1 bit in the TB2SC register is set to 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the P7$_2$ to P7$_5$, P8$_0$ and P8$_1$ pins go to a high-impedance state.

2. The input threshold voltage of pins differs between programmable input/output ports and peripheral functions.
   Therefore, if any pin is shared by a programmable input/output port and a peripheral function and the input level at this pin is outside the range of recommended operating conditions V_{IH} and V_{IL} (neither “high” nor “low”), the input level may be determined differently depending on which side—the programmable input/output port or the peripheral function—is currently selected.

3. When the SM32 bit in the S3C register is set to 1, the P3$_2$ pin goes to high-impedance state. When the SM42 bit in the S4C register is set to 1, the P9$_6$ pin goes to high-imepdance state.

4. When the INV03 bit in the INVC0 register is 1(three-phase motor control timer output enabled), an "L" input on the P8$_5$ /$\overline{NMI}$/$\overline{SD}$ pin, has the following effect.

   - When the TB2SC register IVPCR1 bit is set to 1 (three-phase output forcible cutoff by input on $\overline{SD}$ pin enabled), the U/ $\overline{U}$/ V/ $\overline{V}$/ W/ $\overline{W}$ pins go to a high-impedance state.
   - When the TB2SC register IVPCR1 bit is set to 0 (three-phase output forcible cutoff by input on $\overline{SD}$ pin disabled), the U/ $\overline{U}$/ V/ $\overline{V}$/ W/ $\overline{W}$ pins go to a normal port.

   Therefore, the P8$_5$ pin can not be used as programmable I/O port when the INV03 bit is set to 1.
   When the $\overline{SD}$ function isn't used, set to 0 (Input) in PD8$_5$ and pullup to H in the P8$_5$ /$\overline{NMI}$/$\overline{SD}$ pin from outside.

21.14.9 Interrupts

EW Mode 0

- Any interrupt which has a vector in the variable vector table can be used providing that its vector is transferred into the RAM area.
- The $\overline{\text{NMI}}$ and watchdog timer interrupts can be used because the FMR0 register and FMR1 register are initialized when one of those interrupts occurs. The jump addresses for those interrupt service routines should be set in the fixed vector table.
  Because the rewrite operation is halted when a $\overline{\text{NMI}}$ or watchdog timer interrupt occurs, the rewrite program must be executed again after exiting the interrupt service routine.
- The address match interrupt cannot be used because the flash memory's internal data is referenced.

EW Mode 1

- Make sure that any interrupt which has a vector in the variable vector table or address match interrupt will not be accepted during the auto program period or auto erase period with erase-suspend function disabled.
- The $\overline{\text{NMI}}$ interrupt can be used because the FMR0 register and FMR1 register are initialized when this interrupt occurs. The jump address for the interrupt service routine should be set in the fixed vector table.
  Because the rewrite operation is halted when a $\overline{\text{NMI}}$ interrupt occurs, the rewrite program must be executed again after exiting the interrupt service routine.

21.14.10 How to Access

To set the FMR01, FMR02, FMR11 or FMR16 bit to 1, set the subject bit to 1 immediately after setting to 0. Do not generate an interrupt or a DMA transfer between the instruction to set the bit to 0 and the instruction to set the bit to 1. Set the bit when the PM24 bit is set to 1 ($\overline{\text{NMI}}$ funciton) and a high-level ("H") signal is applied to the $\overline{\text{NMI}}$ pin.

21.14.11 Writing in the User ROM Area

EW Mode 0

- If the power supply voltage drops while rewriting any block in which the rewrite control program is stored, a problem may occur that the rewrite control program is not correctly rewritten and, consequently, the flash memory becomes unable to be rewritten thereafter. In this case, standard serial I/O or parallel I/O mode should be used.

EW Mode 1

- Avoid rewriting any block in which the rewrite control program is stored.

21.14.12 DMA Transfer

In EW mode 1, make sure that no DMA transfers will occur while the FMR00 bit in the FMR0 register is set to 0(during the auto program or auto erase period).

21.14.13 Regarding Programming/Erasure Times and Execution Time

As the number of programming/erasure times increases, so does the execution time for software commands (program command and block erase command).
The software commands are aborted by hardware reset 1, $\overline{\text{NMI}}$ interrupt, and watchdog timer interrupt. If a software command is aborted by such reset or interrupt, the affected block must be erased before reexecuting the aborted command.