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Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Keyboard Controller
Core Processor	AVR
Program Memory Type	SRAM (16kB)
Controller Series	AT43USB
RAM Size	512 x 8
Interface	SPI, 3-Wire Serial
Number of I/O	42
Voltage - Supply	4.4V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at43usb325e-au

1.1 Pin Configuration

Figure 1-1. 64-lead LQFP AT43USB325E-AC

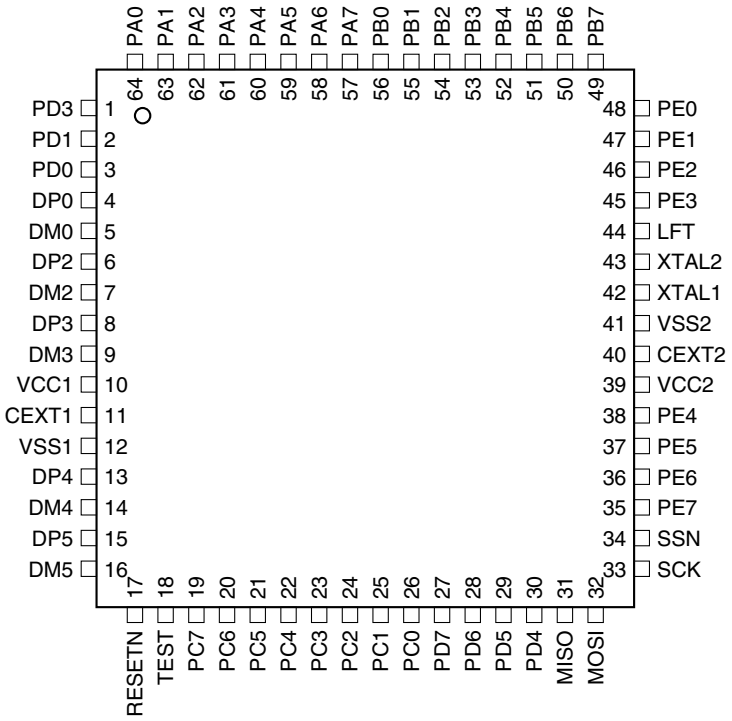
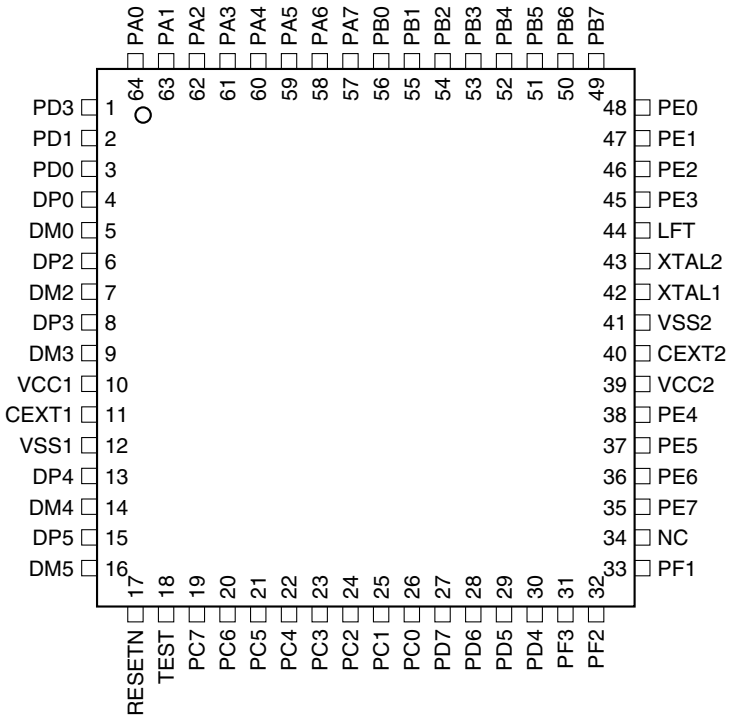


Figure 1-2. 64-lead LQFP AT43USB325M-AC



1.2 Pin Assignment

Pin#	Signal	Type
1	PD3	Bi-directional
2	PD1	Bi-directional
3	PD0	Bi-directional
4	DP0	Bi-directional
5	DM0	Bi-directional
6	DP2	Bi-directional
7	DM2	Bi-directional
8	DP3	Bi-directional
9	DM3	Bi-directional
10	VCC1	Power Supply/Ground
11	CEXT1	Output
12	VSS1	Power Supply/Ground
13	DP4	Bi-directional
14	DM4	Bi-directional
15	DP5	Bi-directional
16	DM5	Bi-directional
17	RESETN	Input
18	TEST	Input
19	PC7	Bi-directional
20	PC6	Bi-directional
21	PC5	Bi-directional
22	PC4	Bi-directional
23	PC3	Bi-directional
24	PC2	Bi-directional
25	PC1	Bi-directional
26	PC0	Bi-directional
27	PD7/INTD	Bi-directional
28	PD6/INTC	Bi-directional
29	PD5/INTB	Bi-directional
30	PD4/INTA	Bi-directional
31	PF3/SO/ICP	Bi-directional
32	PF2/SI/OC1B	Bi-directional

Pin#	Signal	Type
33	PF1/SCK/OC1A	Bi-directional
34	NC/SSN	Bi-directional
35	PE7	Bi-directional
36	PE6	Bi-directional
37	PE5	Bi-directional
38	PE4	Bi-directional
39	VCC2	Power Supply/Ground
40	CEXT2	Output
41	VSS2	Power Supply/Ground
42	XTAL1	Input
43	XTAL2	Output
44	LFT	Output
45	PE3	Bi-directional
46	PE2	Bi-directional
47	PE1	Bi-directional
48	PE0	Bi-directional
49	PB7	Bi-directional
50	PB6	Bi-directional
51	PB5	Bi-directional
52	PB4	Bi-directional
53	PB3	Bi-directional
54	PB2	Bi-directional
55	PB1	Bi-directional
56	PB0	Bi-directional
57	PA7	Bi-directional
58	PA6	Bi-directional
59	PA5	Bi-directional
60	PA4	Bi-directional
61	PA3	Bi-directional
62	PA2	Bi-directional
63	PA1	Bi-directional
64	PA0	Bi-directional

Table 3-2. SRAM Organization

Register File		Data Address Space
R0		$0000
R1		$0001
R30		$001E
R31		$001F

I/O Registers

$00		$0020
$01		$0021
$3E		$005E
$3F		$005F

Internal SRAM

$0060
$0061
$025E
$045F

USB Registers

$1F00
$1FFE
$1FFF

Table 3-4. USB Hub and Function Registers

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GLB_STATE	$1FFB	–	KB INT EN	–	SUSP FLG	RESUME FLG	RMWUPE	CONFG	HADD EN
SPRSR	$1FFA	INTD	INTC	INTB	INTA	-	FRWUP	RSM	GLB SUSP
SPRSIE	$1FF9	INTD EN	INTC EN	INTB EN	INTA EN	-	FRWUP IE	RSM IE	GLB SUSP IE
SPRSMSK	$1FF8	INTD MSK	INTC MSK	INTB MSK	INTA MSK	-	FRWUP MSK	RSM MSK	GLB SUSP MSK
UISR	$1FF7	SOF INT	EOF2 INT	-	FEP3 INT	HEP0 INT	FEP2 INT	FEP1 INT	FEP0 INT
UIMSKR	$1FF6	SOF MSK	SOF2 MSK	-	FEP3 MSK	HEP0 MSK	FEP2 MSK	FEP1 MSK	FEP0 MSK
UIAR	$1FF5	SOF INTACK	EOF2 INTACK	-	FEP3 INTACK	HEP0 INTACK	FEP2 INTACK	FEP1 INTACK	FEP0 INTACK
UIER	$1FF3	SOF IE	EOF2 IE	-	FEP3 IE	HEP0 IE	FEP2 IE	FEP1 IE	FEP0 IE
UOVCER	$1FF2	–	–	–	–	–	OVC	–	–
ISCR	$1FF1	ISC71	ISC70	ISC61	ISC60	ISC51	ISC50	ISC41	ISC40
HADDR	$1FEF	SAEN	HADD6	HADD5	HADD4	HADD3	HADD2	HADD1	HADD0
FADDR	$1FEE	FEN	FADD6	FADD5	FADD4	FADD3	FADD2	FADD1	FADD0
HENDP0_CNTR	$1FE7	EPEN	–	–	–	DTGLE	EPDIR	EPTYPE1	EPTYPE0
FENDP0_CNTR	$1FE5	EPEN	–	–	–	DTGLE	EPDIR	EPTYPE1	EPTYPE0
FENDP1_CNTR	$1FE4	EPEN	–	–	–	DTGLE	EPDIR	EPTYPE1	EPTYPE0
FENDP2_CNTR	$1FE3	EPEN	–	–	–	DTGLE	EPDIR	EPTYPE1	EPTYPE0
FENDP3_CNTR	$1FE2	EPEN	-	-	-	DTGLE	EPDIR	EPTYPE1	EPTYPE0
HCSR0	$1FDF	–	–	–	–	STALL SENT	RX SETUP	RX OUT PACKET	TX CEMPLETE
FCSR0	$1FDD	–	–	–	–	STALL SENT	RX SETUP	RX OUT PACKET	TX COMPLETE
FCSR1	$1FDC	–	–	–	–	STALL SENT	RX SETUP	RX OUT PACKET	TX COMPLETE
FCSR2	$1FDB	–	–	–	–	STALL SENT	RX SETUP	RX OUT PACKET	TX COMPLETE
FCSR3	$1FDA	-	-	-	-	STALL SENT	-	RX OUT PACKET	TX CMPLETE
HDR0	$1FD7	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
FDR0	$1FD5	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
FDR1	$1FD4	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
FDR2	$1FD3	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
FDR3	$1FD2	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
HBYTE_CNT0	$1FCF	–	–	BYTCT5	BYTCT4	BYTCT3	BYTCT2	BYTCT1	BYTCT0
FBYTE_CNT0	$1FCD	–	–	BYTCT5	BYTCT4	BYTCT3	BYTCT2	BYTCT1	BYTCT0
FBYTE_CNT1	$1FCC	–	–	BYTCT5	BYTCT4	BYTCT3	BYTCT2	BYTCT1	BYTCT0
FBYTE_CNT2	$1FCB	–	–	BYTCT5	BYTCT4	BYTCT3	BYTCT2	BYTCT1	BYTCT0
FBYTE_CNT3	$1FCA	-	-	-	BYTCT4	BYTCT3	BYTCT2	BYTCT1	BYTCT0
HSTR	$1FC7	–	–	–	–	OVLSC	LPSC	OVI	LPS
HPCON	$1FC5	–	HPCON2	HPCON1	HPCON0	–	HPADD2	HPADD1	HPADD0
HPSTAT5	$1FBC	-	LSP	PPSTAT	PRSTAT	POCI	PSSTAT	PESTAT	PCSTAT
HPSTAT4	$1FBB	-	LSP	PPSTAT	PRSTAT	POCI	PSSTAT	PESTAT	PCSTAT
HPSTAT3	$1FBA	–	LSP	PPSTAT	PRSTAT	POCI	PSSTAT	PESTAT	PCSTAT
HPSTAT2	$1FB9	–	LSP	PPSTAT	PRSTAT	POCI	PSSTAT	PESTAT	PCSTAT
HPSTAT1	$1FB8	–	LSP	PPSTAT	PRSTAT	POCI	PSSTAT	PESTAT	PCSTAT
HPSCR5	$1FB4	-	-	-	RSTSC	POCIC	PSSC	PESC	PCSC
HPSCR4	$1FB3	-	-	-	RSTSC	POCIC	PSSC	PESC	PCSC
HPSCR3	$1FB2	–	–	–	RSTSC	POCIC	PSSC	PESC	PCSC
HPSCR2	$1FB1	–	–	–	RSTSC	POCIC	PSSC	PESC	PCSC
HPSCR1	$1FB0	–	–	–	RSTSC	POCIC	PSSC	PESC	PCSC
PSTAT5	$1FAC	–	–	–	–	–	–	DPSTATE	DMSTATE
PSTAT4	$1FAB	–	–	–	–	–	–	DPSTATE	DMSTATE
PSTAT3	$1FAA	–	–	–	–	–	–	DPSTATE	DMSTATE
PSTAT2	$1FA9	–	–	–	–	–	–	DPSTATE	DMSTATE
HCAR0	$1FA7	CTL DIR	DATA END	FORCE STALL	TX PACKET READY	STALL_SENT-ACK	RX_SETUP_ACK	RX_OUT_PACKET_ACK	TX_COMPLETE-ACK
FCAR0	$1FA5	CTL DIR	DATA END	FORCE STALL	TX PACKET READY	STALL_SENT-ACK	RX_SETUP_ACK	RX_OUT_PACKET_ACK	TX_COMPLETE-ACK

from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

4.11.1 MCU Control Register – MCUCR

Bit	7	6	5	4	3	2	1	0	
$35 ($55)	–	–	SE	SM	ISC11	ISC10	–	–	MCUCR
Read/Write	R	R	R/W	R/W	R/W	R/W	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7, 6 – Res: Reserved Bits**

- **Bit 5 – SE: Sleep Enable**

The SE bit must be set (1) to make the MCU enter the sleep mode when the SLEEP instruction is executed. To avoid the MCU entering the sleep mode, unless it is the programmer's purpose, it is recommended to set the Sleep Enable SE bit just before the execution of the SLEEP instruction.

- **Bit 4 – SM: Sleep Mode**

This bit selects between the two available sleep modes. When SM is cleared (zero), Idle Mode is selected as Sleep Mode. When SM is set (1), Power Down mode is selected as sleep mode. The AT43USB325 does not support the Idle Mode and SM should always be set to one when entering the Sleep Mode.

- **Bit 3, 2 – ISC11, ISC10: Interrupt Sense Control 1 Bit 1 and Bit 0**

The External Interrupt 1 is activated by the external pin INT1 if the SREG I-flag and the corresponding interrupt mask in the GIMSK is set. The level and edges on the external INT1 pin that activate the interrupt are defined in the following table:

Table 4-2. INT1 Sense Control

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Reserved.
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

4.13.2 USB Interrupt Mask Register – UIMSKR

Bit	7	6	5	4	3	2	1	0	
$1FF6	SOF IMSK	EOF2 IMSK	–	FEP3 IMSK	HEP0 IMSK	FEP2 IMSK	FEP1 IMSK	FEP0 IMSK	UIMSKR
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – SOF IMSK: Enable Start of Frame Interrupt Mask**

When the SOF IMSK bit is set (1), the Start of Frame Interrupt is masked.

- **Bit 6 – EOF2 IMSK: Enable EOF2 Interrupt**

When the EOF2 IMSK bit is set (1), the EOF2 Interrupt is masked.

- **Bit 5 – Res: Reserved Bit**

This bit is reserved and always read as zero.

- **Bit 4 – FEP3 IMSK: Function End-point 3 Interrupt Mask**

When the FE3 IMSK bit is set (1), the Function End-point 3 Interrupt is masked.

- **Bit 3 – HEP0 IMSK: Enable Endpoint 0 Interrupt**

When the HEP0 IMSK bit is set (1), the Hub Endpoint 0 Interrupt is masked.

- **Bit 2 – FEP2 IMSK: Enable Endpoint 2 Interrupt**

When the FE2 IMSK bit is set (1), the Function Endpoint 2 Interrupt is masked.

- **Bit 1 – FEP1 IMSK: Enable Endpoint 1 Interrupt**

When the FE1 IMSK bit is set (1), the Function Endpoint 1 Interrupt is masked.

- **Bit 0 – FEP0 IMSK: Enable Endpoint 0 Interrupt**

When the FE0 IMSK bit is set (1), the Function Endpoint 0 Interrupt is masked.

6.2.1 Timer/Counter0 Control Register – TCCR0

Bit	7	6	5	4	3	2	1	0	
$33 ($53)	–	–	–	–	–	CS02	CS01	CS00	TCCR0
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7..3 – Res: Reserved Bits**

These bits are reserved bits in the AT43USB325 and always read as zero.

- **Bits 2, 1, 0 – CS02, CS01, CS00: Clock Select0, bit 2, 1 and 0**

The Clock Select0 bits 2, 1 and 0 define the prescaling source of Timer/Counter0.

Table 6-1. Clock 0 Prescale Select

CS02	CS01	CS00	Description
0	0	0	Stop, the Timer/Counter0 is stopped
0	0	1	CK
0	1	0	CK/8
0	1	1	CK/64
1	0	0	CK/256
1	0	1	CK/1024
1	1	0	External Pin T0, falling edge
1	1	1	External Pin T0, rising edge

The Stop condition provides a Timer Enable/Disable function. The CK down divided modes are scaled directly from the CK oscillator clock. If the external pin modes are used for Timer/Counter0, transitions on PB0/(T0) will clock the counter even if the pin is configured as an output. This feature can give the user SW control of the counting.

6.2.2 Timer/Counter0 – TCNT0

Bit	7	6	5	4	3	2	1	0	
$32 ($52)	MSB	–	–	–	–	–	–	LSB	TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Timer/Counter0 is realized as an up-counter with read and write access. If the Timer/Counter0 is written and a clock source is present, the Timer/Counter0 continues counting in the clock cycle following the write operation.

down-counting compare match is not interpreted to be reached before the next time the counter reaches the TOP value, making a one-period PWM pulse.

Table 6-7. PWM Outputs OCR1X = $0000 or Top

COM1X1	COM1X0	OCR1X	Output OC1X
1	0	$0000	L
1	0	TOP	H
1	1	$0000	H
1	1	TOP	L

Note: X = A or B

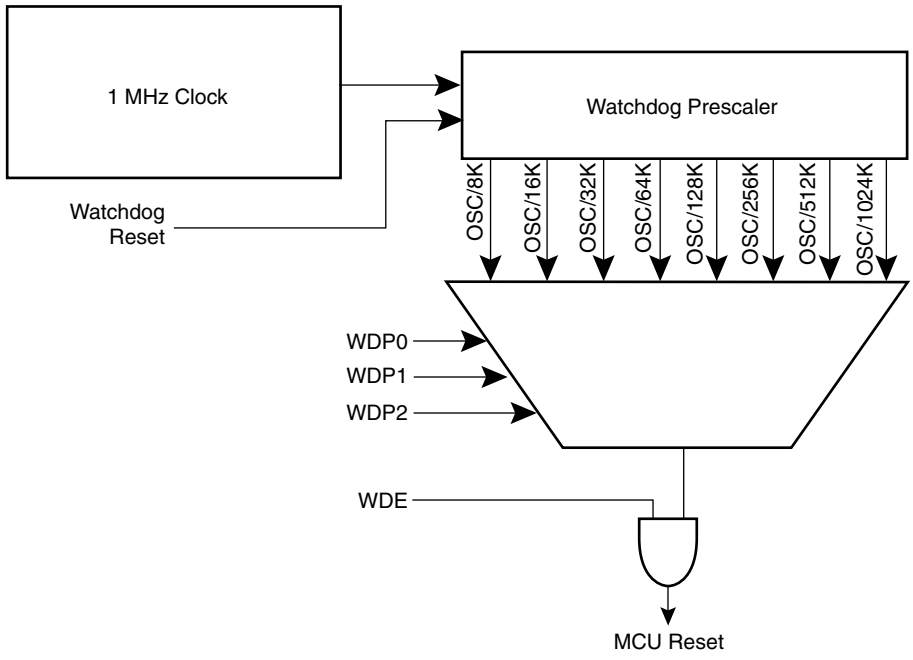
In PWM mode, the Timer Overflow Flag1, TOV1, is set when the counter advances from $0000. Timer Overflow Interrupt1 operates exactly as in normal Timer/Counter mode, i.e. it is executed when TOV1 is set provided that Timer Overflow Interrupt1 and global interrupts are enabled. This also applies to the Timer Output Compare1 flags and interrupts.

6.5 Watchdog Timer

The Watchdog Timer is clocked from a 1 MHz clock derived from the 6 MHz on chip oscillator. By controlling the Watchdog Timer prescaler, the Watchdog reset interval can be adjusted, see Table 6-8 for a detailed description. The WDR (Watchdog Reset) instruction resets the Watchdog Timer. Eight different clock cycle periods can be selected to determine the reset period. If the reset period expires without another Watchdog reset, the AT43USB325 resets and executes from the reset vector.

To prevent unintentional disabling of the watchdog, a special turn-off sequence must be followed when the watchdog is disabled. Refer to the description of the Watchdog Timer Control Register for details.

Figure 6-6. Watchdog Timer



7.3 Port C

Port C is an 8-bit bi-directional I/O port with an internal pull-up resistor at each pin. Port C is designed for use as the row inputs of a keyboard controller. Its output buffers can sink 4 mA.

Three I/O memory address locations are allocated for the Port C, one each for the Data Register - PORTC, $15($35), Data Direction Register - DDRC, $14($34) and the Port C Input Pins – PINC, $13($33). The Port C Input Pin's address is read only, while the Data Register and the Data Direction Register are read/write.

7.3.1 Port C Data Register – PORTC

Bit	7	6	5	4	3	2	1	0	
$15 ($35)	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	PORTC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

7.3.2 Port C Data Direction Register – DDRC

Bit	7	6	5	4	3	2	1	0	
$14 ($34)	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

7.3.3 Port C Input Pins Address – PINC

Bit	7	6	5	4	3	2	1	0	
$13 ($33)	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	PINC
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

The Port C Input Pins address (PINC) is not a register, and this address enables access to the physical value on each Port C pin. When reading PORTC, the Port C Data Latch is read, and when reading PINC, the logical values present on the pins are read.

7.4.4 Port D as General Digital I/O

PDn, General I/O Pin: The DDDn bit in the DDRD register selects the direction of this pin. If DDDn is set (one), PDn is con-figured as an output pin. If DDDn is cleared (zero), PDn is configured as an input pin. The value of PORTDn has no meaning in this mode. The Port D pins are tri-stated when a reset condition becomes active.

Table 7-3. DDDn Bits on Port D Pins

DDDn	PORTDn	I/O	Comment
0	0	Input	Tri-state (Hi-Z)
0	1	Input	Tri-state (Hi-Z)
1	0	Output	Push-pull Zero Output
1	1	Output	Push-pull One Output

Note: n: 7,6,5,4,3,1,0, pin number

7.4.5 Alternate Functions of Port D

INT1, External Interrupt Source 1: The PD3 pin can serve as an external interrupt source to the MCU. See the interrupt description for further details, and how to enable the source.

7.5 Port E

Port E[0:3] each is a bi-directional I/O port with open drain outputs and controlled slew rate and is designed for use as the column drivers in a keyboard controller. The Port E[0:3] output buffers can sink 4 mA. Port E[4:7] are bi-directional I/O with outputs capable of driving LEDs directly. Each pin of Port E[4:7] has a series resistor to limit the LEDs current.

Three I/O memory address locations are allocated for the Port E, one each for the Data Register - PORTE, $03($23), Data Direction Register - DDRE, $02($22) and the Port E Input Pins - PINE, $01($21). The Port E Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

7.5.1 Port E Data Register – PORTE

Bit	7	6	5	4	3	2	1	0	
$03($23)	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0	PORTE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

7.5.2 Port E Data Direction Register – DDRE

Bit	7	6	5	4	3	2	1	0	
$02 ($22)	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0	DDRE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

7.6.1 Port F Data Register – PORTF

Bit	7	6	5	4	3	2	1	0	
$06($26)	-	-	-	-	PORTF3	PORTF2	PORTF1	-	PORTF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

7.6.2 Port F Data Direction Register – DDRF

Bit	7	6	5	4	3	2	1	0	
$05($25)	-	-	-	-	DDF3	DDF2	DDF1	-	DDRF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

7.6.3 Port F Input Pin Address – PINF

Bit	7	6	5	4	3	2	1	0	
$04($24)	-	-	-	-	PINF3	PINF2	PINF1	-	PINF
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

The Port F Input Pins address - PINF - is not a register, and this address enables access to the physical value on each Port F pin. When reading PORTF, the Port F Data Latch is read, and when reading PINF, the logical values present on the pins are read.

7.6.4 Port F as General Digital I/O

PFn, General I/O Pin: After firmware downloading, the DDFn bit in the DDRF register selects the direction of this pin. If DDFn is set (one), PFn is con-figured as an output pin. If DDFn is cleared (zero), PFn is configured as an input pin. The value of PORTFn has no meaning in this mode. The Port F pins are tri-stated when a reset condition becomes active.

Table 7-6. DDFn Bits on Port F Pins

DDFn	PORTFn	I/O	Comment
0	0	Input	Tri-state (Hi-Z)
0	1	Input	Tri-state (Hi-Z)
1	0	Output	Push-pull Zero Output
1	1	Output	Push-pull One Output

Note: n: 3,2,1, pin number

8.1.3 Setup Response State

The Function Interface Unit (FIU) receives a SETUP token with 8 bytes of data from the Host. The FIU stores the data in the FIFO, sends an ACK back to the host and asserts an RX_SETUP interrupt.

Hardware

1. SETUP token, DATA from Host
2. ACK to Host
3. Store data in FIFO
4. Set RX SETUP → INT

Firmware

5. Read UISR
6. Read CSR0
7. Read Byte Count
8. Read FIFO
9. Parse command data
10. Write to H/FCAR0:
11. If Control Read: set DIR, clear RX SETUP, fill FIFO, set TX Packet Ready in CAR0
12. If Control Write: clear DIR in CAR0
13. If no Data Stage: set Data End, clear DIR, set Force STALL in CAR0
14. Set UIAR[EP0 INTACK] to clear the interrupt source

8.3 Endpoint Registers

8.3.1 Hub Endpoint 0 Control Register – HENDP0_CR

8.3.2 Function Endpoint 0 Control Register – FENDP0_CR

Bit	7	6	5	4	3	2	1	0	
$1FE7	**EPEN**	**–**	**–**	**–**	**DTGLE**	**EPDIR**	**EPTYPE1**	**EPTYPE0**	**HENDP0_CR**
$24 ($44)	**EPEN**	**–**	**–**	**–**	**DTGLE**	**EPDIR**	**EPTYPE1**	**EPTYPE0**	**FENDP0_CR**
Read/Write	R/W	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – EPEN: Endpoint Enable**

0 = Disable endpoint

1 = Enable endpoint

- **Bit 6..4 – Reserved**

These bits are reserved in the AT43USB325 and will read as zero.

- **Bit 3 – DTGLE: Data Toggle**

Identifies DATA0 or DATA1 packets. This bit will automatically toggle and requires clearing by the firmware only in certain special circumstances.

- **Bit 2 – EPDIR: Endpoint Direction**

0 = Out

1 = In

- **Bit 1, 0 – EPTYPE: Endpoint Type**

These bits must be programmed as 0, 0.

8.3.3 Function Endpoint 1-3 Control Register – FENDP1-3_CR

Bit	7	6	5	4	3	2	1	0	
$1FE4	**EPEN**	**–**	**–**	**–**	**DTGLE**	**EPDIR**	**EPTYPE1**	**EPTYPE0**	**FENDP1_CR**
$1FE3	**EPEN**	**–**	**–**	**–**	**DTGLE**	**EPDIR**	**EPTYPE1**	**EPTYPE0**	**FENDP2_CR**
$1FE2	**EPEN**	**–**	**–**	**–**	**DTGLE**	**EPDIR**	**EPTYPE1**	**EPTYPE0**	**FENDP3_CR**
Read/Write	R/W	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – EPEN: Endpoint Enable**

0 = Disable endpoint

1 = Enable endpoint

- **Bit 6..4 – Reserved**

These bits are reserved in the AT43USB325 and will read as zero.

- **Bit 3 – DTGLE: Data Toggle**

Identifies DATA0 or DATA1 packets. This bit will automatically toggle and requires clearing by the firmware only in certain special circumstances.

- **Bit 2 – EPDIR: Endpoint Direction**

0 = Out

1 = In

- **Bit 1, 0 – EPTYPE: Endpoint Type**

These bits program the type of endpoint.

Bit1	Bit0	Type
0	1	Isochronous
1	0	Bulk
1	1	Interrupt

The microcontroller should write into the FIFO only if this bit is cleared. After it has completed writing the data, it should set this bit. This data can be of zero length.

Hardware clears this bit after it receives an ACK. If the interrupt is enabled and if the TX Complete bit is set, clearing the TX Packet Ready bit by the hardware causes an interrupt to the microcontroller.

- **Bit 3 – STALL_SENT_ACK: Acknowledge Stall Sent Interrupt**

Firmware sets this bit to clear STALL SENT, CSR bit 3. The 1 written in the CSRACK3 bit is not actually stored and thus does not have to be cleared.

- **Bit 2 – RX_SETUP_ACK: Acknowledge RX SETUP Interrupt**

Firmware sets this bit to clear RX SETUP, CSR bit2. The 1 written in the CSRACK2 bit is not actually stored and thus does not have to be cleared.

- **Bit 1 – RX_OUT_PACKET_ACK: Acknowledge RX OUT PACKET Interrupt**

Firmware sets this bit to clear RX OUT PACKET, CSR bit1. The 1 written in the CSRACK1 bit is not actually stored and thus does not have to be cleared.

- **Bit 0 – TX_COMPLETE_ACK: Acknowledge TX COMPLETE Interrupt**

Firmware sets this bit to clear TX COMPLETE, CSR bit0. The 1 written in the CSRACK0 bit is not actually stored and thus does not have to be cleared.

8.4.2 Hub Status Register

In the AT43USB325 overcurrent detection and port power switch control output processing is done in firmware. The hardware is designed so that various types of hubs are possible just through firmware modifications.

1. Hub local power status, bits 0 and 2, are optional features and apply to hubs that report on a global basis. If this feature is not used, both these bits should be programmed to 0. To use this feature, the firmware needs to know the status of the local power supply, which requires an input pin and extra internal or external circuitry.
2. Hub overcurrent status, bits 1 and 3, apply to self powered hubs with bus powered SIE only, or hubs that are programmable as self/bus powered. The firmware should clear these two bits to 0.

The firmware uses bits 1 and 3 to generate bit 0 of the Hub and Port Status Change Bitmap which is transmitted through the Hub Endpoint1 Data Register. Bit 0 of this register is a 1 whenever bit 1 or 3 of HSTATR is a 1.

8.4.2.1 Hub Status Register – HSTR

Bit	7	6	5	4	3	2	1	0	
$1FC7	–	–	–	–	OVLSC	LPSC	OVI	LPS	HSTR
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7..4 – Reserved**

These bits are reserved in the AT43USB325 and will read as zero.

- **Bit 3 – OVLSC: Overcurrent Status Change**

0 = No change has occurred on Overcurrent Indicator

1 = Overcurrent Indicator has changed

- **Bit 2 – LPSC: Hub Local Power Status Change**

0 = No change has occurred on Local Power Status

1 = Local Power Status has changed

- **Bit 1 – OVI: Overcurrent Indicator**

0 = All power operations normal

1 = An overcurrent exist on a hub wide basis

- **Bit 0 – LPS: Hub Local Power Status**

0 = Local power supply is good

1 = Local power supply is lost (inactive)

8.4.4.3 Hub Port State Register – HPSTAT2...5

Bit	7	6	5	4	3	2	1	0	
Port2 $1FA9	–	–	–	–	–	–	DPSTATE	DMSTATE	PSTATE2
Port3 $1FAA	–	–	–	–	–	–	DPSTATE	DMSTATE	PSTATE3
Port4 $1FAB	–	–	–	–	–	–	DPSTATE	DMSTATE	PSTATE4
Port5 $1FAC	–	–	–	–	–	–	DPSTATE	DMSTATE	PSTATE5
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

These registers contain the state of the ports' DP and DM pins, which will be sent to the host upon receipt of a GetBusState request.

- **Bit 7..2 – Reserved**

These bits are reserved in the AT43USB325 and will read as zero.

- **Bit 1 – DPSTATE: DPlus State**

Value of DP at last EOF. Set and cleared by hardware at EOF2.

Set to 1 for Port 1.

- **Bit 0 – DMSTATE: DMinus State**

Value of DM at last EOF. Set and cleared by hardware at EOF2.

Set to 0 for Port 1.

8.4.4.4 Hub Port Status Change Register – PSCR1..5

Bit	7	6	5	4	3	2	1	0	
Port1 $1FB0	–	–	–	RSTSC	POCIC	PSSC	PESC	PCSC	PSCR1
Port2 $1FB1	–	–	–	RSTSC	POCIC	PSSC	PESC	PCSC	PSCR2
Port3 $1FB2	–	–	–	RSTSC	POCIC	PSSC	PESC	PCSC	PSCR3
Port4 $1FB3	–	–	–	RSTSC	POCIC	PSSC	PESC	PCSC	PSCR4
Port5 $1FB4	–	–	–	RSTSC	POCIC	PSSC	PESC	PCSC	PSCR5
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

The microcontroller firmware uses the bits in this register to monitor when a port status change has occurred, which then gets reported to the host through the Port Change Field *wPortChange*.

Except for bit 3, the Port Overcurrent Indicator Change, the bits in this register are set by the USB hardware. Otherwise, the firmware should only clear these bits.

- **Bit 7..5 – Reserved**

These bits are reserved in the AT43USB325 and will read as zero.

- **Bit 4 – RSTSC: Port Reset Status Change**

0 = No change

8.5.4 Suspend and Resume Process

8.5.4.1 Global Suspend

The Host stops sending packets, the hardware detects this as global suspend signaling and stops all downstream signaling. Finally, the hardware asserts the GLB_SUSP interrupt.

Hardware	Firmware
1. Host stops sending packets	
2. Global suspend signaling detected	
3. Stop downstream signaling	
4. Set GBL SUS bit → interrupt	
	5. Shut down any peripheral activity
	6. Set Sleep Enable and Sleep Mode bits of MCUCR
	7. Set GPIO to low power state if required
	8. Set UOVCER bit 2
	9. Execute SLEEP instruction
10. SLEEP bit detected	
11. Shut off oscillator	

8.5.4.2 Global Resume

The Host resumes signaling, the hardware detects this as global resume and propagates this signaling to all downstream ports. Finally, the hardware enables the oscillator and asserts the RSM interrupt.

Hardware	Firmware
1. Host resumes signaling	
2. Resume signaling detected	
3. Propagate signaling downstream	
4. Enable oscillator	
5. Set RSM bit → interrupt	
	6. Reset RSM and GBL SUSP bits
	7. Restore GPIO states if required
	8. Clear UOVCER bit 2
	9. Enable peripheral activity

8.5.4.6 Selective Suspend, Embedded Function

Hardware	Firmware
	1. Set Port Feature PORT_SUSPEND decoded 2. Disable Port 1's endpoints 3. Set GPIO to low power state if required

8.5.4.7 Selective Resume, Embedded Function

Hardware	Firmware
	1. Clear Port Feature PORT_SUSPEND decoded 2. Clear Port 1 suspend status bit 3. Restore GPIO states if required 4. Wait 23 ms, then set enable status bit and suspend change bit 5. Enable Port 1 endpoints
6. Send updated port status at next IN to endpoint1	

Table 9-4. PA, PB, PC, PD, PE, PF

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL2}	Output Low Level, PA, PB, PE[0:3]	IOL = 4 mA		0.5	V
RPU	PC Pull-up resistor current	V = 0	90	280	µA
V_{IL3}	Input Low Level, PC			0.3 VCEXT	V
V_{IH3}	Input High Level, PC		0.7 VCEXT		V
V_{IL4}	Input Low Level, PD[0,1]			0.3 VCEXT	V
V_{IH4}	Input High Level, PD[0,1]		0.7 VCEXT		V
V_{OL4}	Output Low Level, PD[0,1]	IOL = 4 mA		0.3 VCEXT	V
V_{OH4}	Output High Level, PD[0,1]	IOH = 4 mA	0.7 VCEXT		V
C	Input/Output capacitance	1 MHz		10	pF

Note: VCEXT is the voltage at CEXT1, CEXT2.

Table 9-5. Oscillator Signals: XTAL1, XTAL2

Symbol	Parameter	Condition	Min	Max	Unit
V_{LH}	OSC1 switching level		0.47	1.20	V
V_{HL}	OSC1 switching level		0.67	1.44	V
CX1	Input capacitance, XTAL1			10	pF
CX2	Output capacitance, XTAL2			10	pF
C12	OSC1/2 capacitance			5	pF
t_{SU}	Start-up time	6 MHz, fundamental		2	ms
DL	Drive level			50	µW

Note: XTAL2 must not be used to drive other circuitry.

9.2.1 AC Characteristics

Table 9-6. SEEPROM SPI Timing

Symbol	Parameter	Condition	Min	Max	Unit
f_{SCK}	SCK Clock Frequency 50% duty cycle		333	333	ns
t_{RO}, t_{FO}	Output Rise Time, Fall Time		10	10	ns
			-5	5	ns
t_{CSS}	SSN Setup Time		0	20	ns
t_{CSH}	SSN Hold Time		0	20	ns
t_{SU}	Data IN Setup Time		10		ns
t_H	Data In Hold Time		2		ns
t_{HO}	Output Hold Time		0		ns
t_V	Output Valid			10	ns