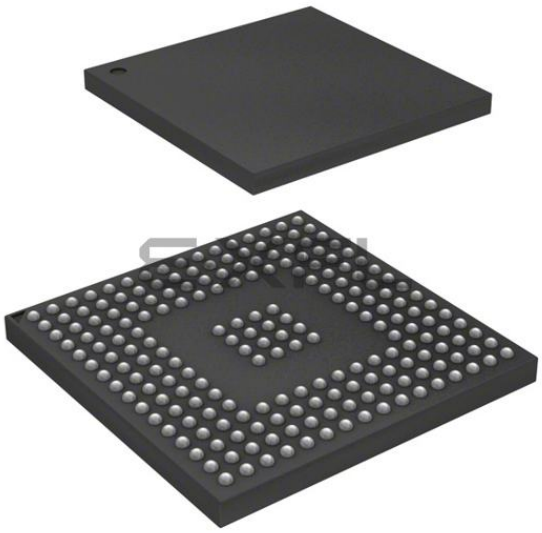
Infineon Technologies - SAF-TC1115-L100EB BB Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, FIFO, I²C, IrDA, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	144K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LBGA
Supplier Device Package	P-LBGA-208-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-tc1115-l100eb-bb

2 General Device Information

2.1 Block Diagram

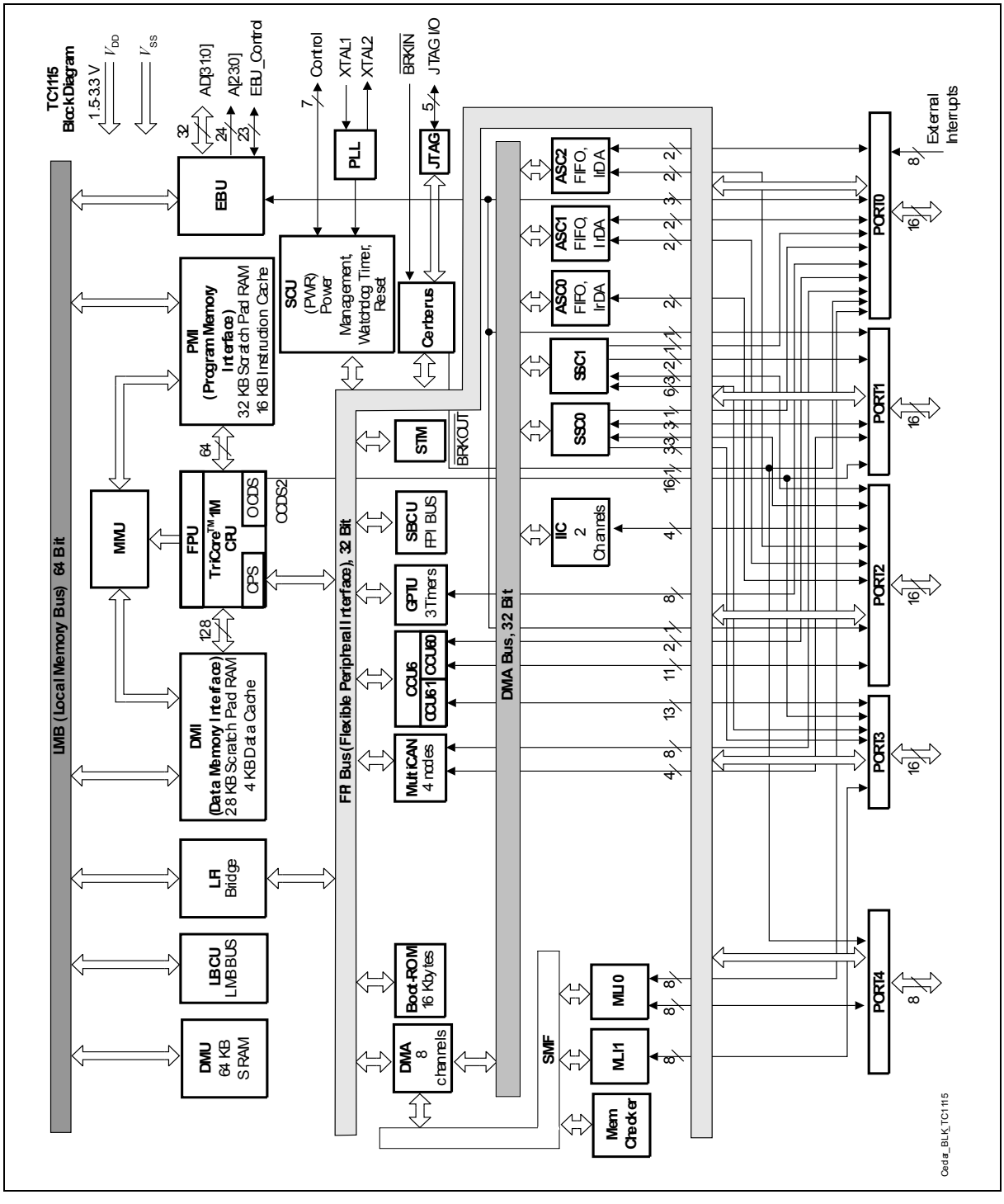


Figure 2-1 TC1115 Block Diagram

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P1.7	B13	I	PUC	SWCFG7	Software configuration 7
		O		OCDSA_7	OCDS L2 Debug Line A7
P1.8	A13	I	PUC	SWCFG8	Software configuration 8
		O		OCDSA_8	OCDS L2 Debug Line A8
P1.9	A14	I	PUC	SWCFG9	Software configuration 9
		O		OCDSA_9	OCDS L2 Debug Line A9
P1.10	B14	I	PUC	SWCFG10	Software configuration 10
		O		OCDSA_10	OCDS L2 Debug Line A10
P1.11	C14	I	PUC	SWCFG11	Software configuration 11
		O		OCDSA_11	OCDS L2 Debug Line A1
		O		SLSO0_1	SSC0 Slave Select output 1
P1.12	F13	I	PUC	SWCFG12	Software configuration 12
		O		OCDSA_12	OCDS L2 Debug Line A12
		O		SLSO1_1	SSC1 Slave Select output 1
P1.13	E14	I	PUC	SWCFG13	Software configuration 13
		O		OCDSA_13	OCDS L2 Debug Line A13
		O		SLSO0_2	SSC0 Slave Select output 2
P1.14	D14	O	PUC	SLSO1_2	SSC1 Slave Select output 2
		I		SWCFG14	Software configuration 14
		O		OCDSA_14	OCDS L2 Debug Line A14
P1.15	F14	I	PUC	SLSI0	SSC0 Slave Select Input
		O		RMW	EBU Read Modify Write
		I		SWCFG15	Software configuration 15
		O		OCDSA_15	OCDS L2 Debug Line A15

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P2		I/O		**Port 2** Port 2 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for ASC0/1/2, SSC0/1, CCU60, IIC, EBU and SCU.	
P2.0	P12	I/O	PUC	RXD0	ASC0 receiver input/output line
		O		CSEMU	EBU Chip Select Output for Emulator Region
P2.1	P11	O	PUC	TXD0	ASC0 transmitter output line
		I		TESTMODE	Test Mode Select Input
P2.2	P13	I/O	PUC	MRST0	SSC0 master receive/slave transmit input/output
P2.3	P14	I/O	PUC	MTSR0	SSC0 master transmit/slave receive input/output
P2.4	N15	I/O	PUC	SCLK0	SSC0 clock input/output line
P2.5	N14	O	PUC	COUT60_3	CCU60 compare channel 3 output
		I/O		MRST1A	SSC1 master receive/slave transmit input/output A
P2.6	N12	I/O	PUC	CC60_0	CCU60 input/output of capture/ compare channel 0
		I/O		MTSR1A	SSC1 master transmit/slave receive input/output A
P2.7	K16	O	PUC	COUT60_0	CCU60 output of capture/compare channel 0
		I/O		SCLK1A	SSC1 clock input/output line A
P2.8	J16	I/O	PUC	CC60_1	CCU60 input/output of capture/ compare channel 1
		I/O		RXD1A	ASC1 receiver input/output line A
P2.9	H16	O	PUC	COUT60_1	CCU60 output of capture/compare channel 1
		O		TXD1A	ASC1 transmitter output line A
P2.10	L13	I/O	PUC	CC60_2	CCU60 input/output of capture/ compare channel 2
		I/O		RXD2A	ASC2 receiver input/output line A
P2.11	G16	O	PUC	COUT60_2	CCU60 output of capture/compare channel 2
		O		TXD2A	ASC2 transmitter output line A
P2.12	K15	I/O	—	SDA0	IIC Serial Data line 0
		I		CTRAP0	CCU60 trap input
		O		SLSO0_3	SSC0 Slave Select output 3

3.2 Address Map

Table 3-1 defines the specific segment oriented address blocks of the TC1115 with its address range, size, and PMI/DMI access view. Table 3-2 shows the block address map of the Segment 15 which includes on-chip peripheral units and ports.

Table 3-1 TC1115 Block Address Map

Segment	Address Range	Size	Description	DMI Acc.	PMI Acc.	
0 – 7	0000 0000$_H$ – 7FFF FFFF$_H$	2 GB	MMU Space	via FPI	via FPI	cached
8	8000 0000$_H$ – 8FFF FFFF$_H$	256 MB	External Memory Space mapped from Segment 10	via LMB	via LMB	
9	9000 0000$_H$ – 9FDF FFFF$_H$	256 MB	Reserved	via FPI	via FPI	
10	A000 0000$_H$ – AFBF FFFF$_H$	252 MB	External Memory Space	via LMB	via LMB	non-cached
	AFC0 0000$_H$ – AFC0 FFFF$_H$	64 KB	DMU Space			
	AFC1 0000$_H$ – AFFF FFFF$_H$	~4 MB	Reserved			
11	B000 0000$_H$ – BFFF FFFF$_H$	256 MB	Reserved	via FPI	via FPI	
12	C000 0000$_H$ – C000 FFFF$_H$	64 KB	DMU	via LMB	via LMB	cached
	C001 0000$_H$ – CFFF FFFF$_H$	~ 256 MB	Reserved			

3.7 Interrupt System

An interrupt request can be serviced by the CPU, which is called “Service Provider”. Interrupt requests are referred to as “Service Requests” in this document.

Each peripheral in the TC1115 can generate service requests. Additionally, the Bus Control Unit, the Debug Unit, the DMA Controller and even the CPU itself can generate service requests to the Service Provider. As shown in **Figure 3-3**, each unit that can generate service requests is connected to one or multiple Service Request Nodes (SRN). Each SRN contains a Service Request Control Register mod_SRC, where “mod” is the identifier of the unit requesting service. The SRNs are connected to the Interrupt Control Unit (ICU) via the CPU Interrupt Arbitration Bus. The ICU arbitrates service requests for the CPU and administers the Interrupt Arbitration Bus.

Units that can generate service requests are:

- Asynchronous/Synchronous Serial Interfaces (ASC0, ASC1 and ASC2) with 4 SRNs each
- High-Speed Synchronous Serial Interfaces (SSC0 and SSC1) with 3 SRNs each
- Inter IC Interface (IIC) with 3 SRNs
- Micro Link Interface MLI0 with 4 SRNs and MLI1 with 2 SRNs
- General Purpose Timer Unit (GPTU) with 8 SRNs
- Capture/Compare Unit (CCU60 and CCU61) with 4 SRNs each
- MultiCAN (CAN) with 16 SRNs
- External Interrupts with 4 SRNs
- Direct Memory Access Controller (DMA) with 4 SRNs
- DMA Bus with 1 SRN
- System Timer (STM) with 2 SRNs
- Bus Control Units (SBCU and LBCU) with 1 SRN each
- Central Processing Unit (CPU) with 4 SRNs
- Floating Point Unit (FPU) with 1 SRN
- Debug Unit (OCDS) with 1 SRN

The CPU can make service requests directly to itself (via the ICU). The CPU Service Request Nodes are activated through software.

- Evaluation of the device address in slave mode
- Bus access arbitration in multimaster mode

Features:

- Extended buffer allows up to 4 send/receive data bytes to be stored
- Selectable baud rate generation
- Support of standard 100 kBaud and extended 400 kBaud data rates
- Operation in 7-bit addressing mode or 10-bit addressing mode
- Flexible control via interrupt service routines or by polling
- Dynamic access to up to 2 physical IIC buses

3.12 MultiCAN

Figure 3-8 shows a global view of the functional blocks of the MultiCAN module.

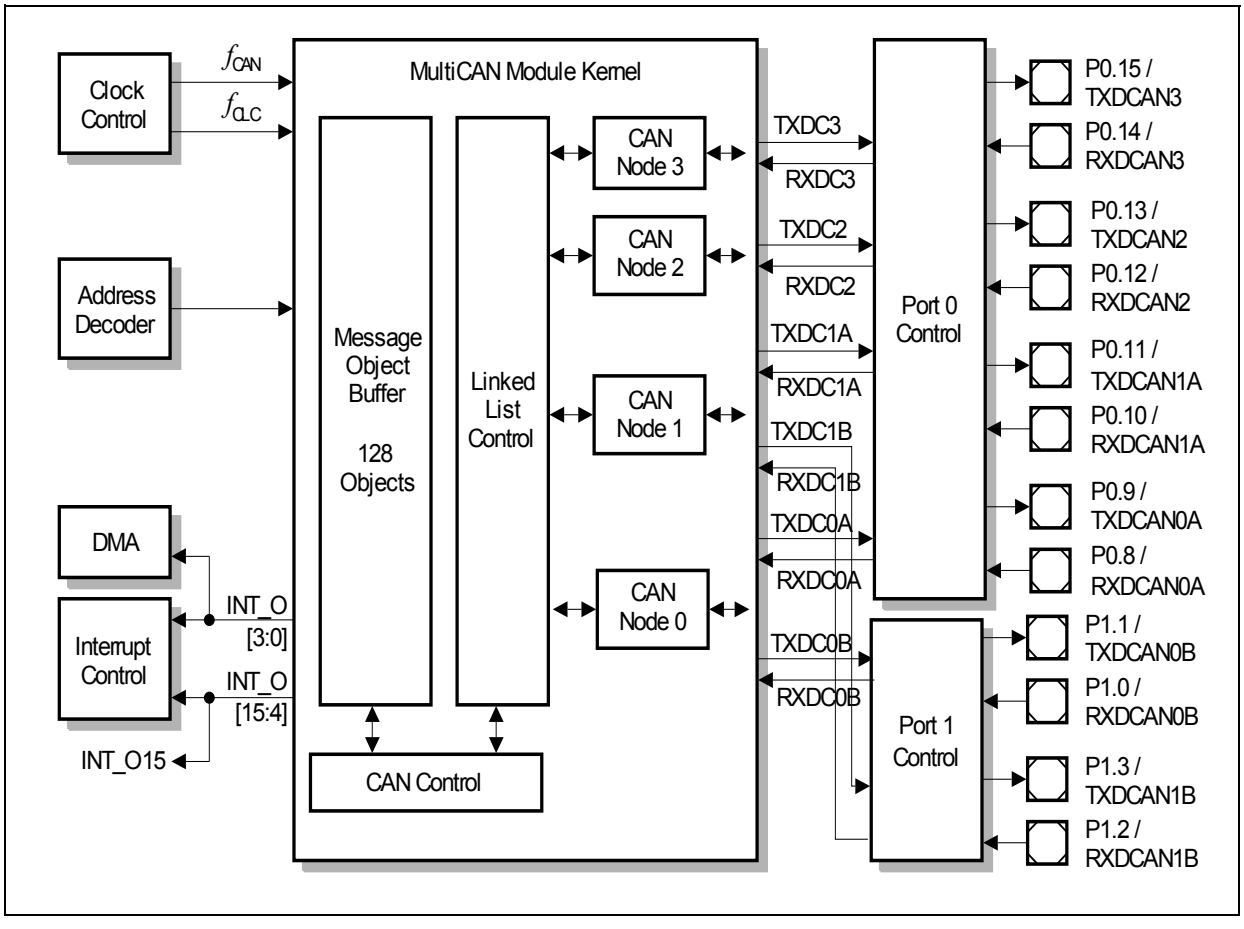


Figure 3-8 General Block Diagram of the MultiCAN Interface

The MultiCAN module contains 4 Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects, where each message object may be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects may be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double chained lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to the list of the CAN node. It only transmits messages from objects of this list.

A powerful, command driven list controller performs all list operations.

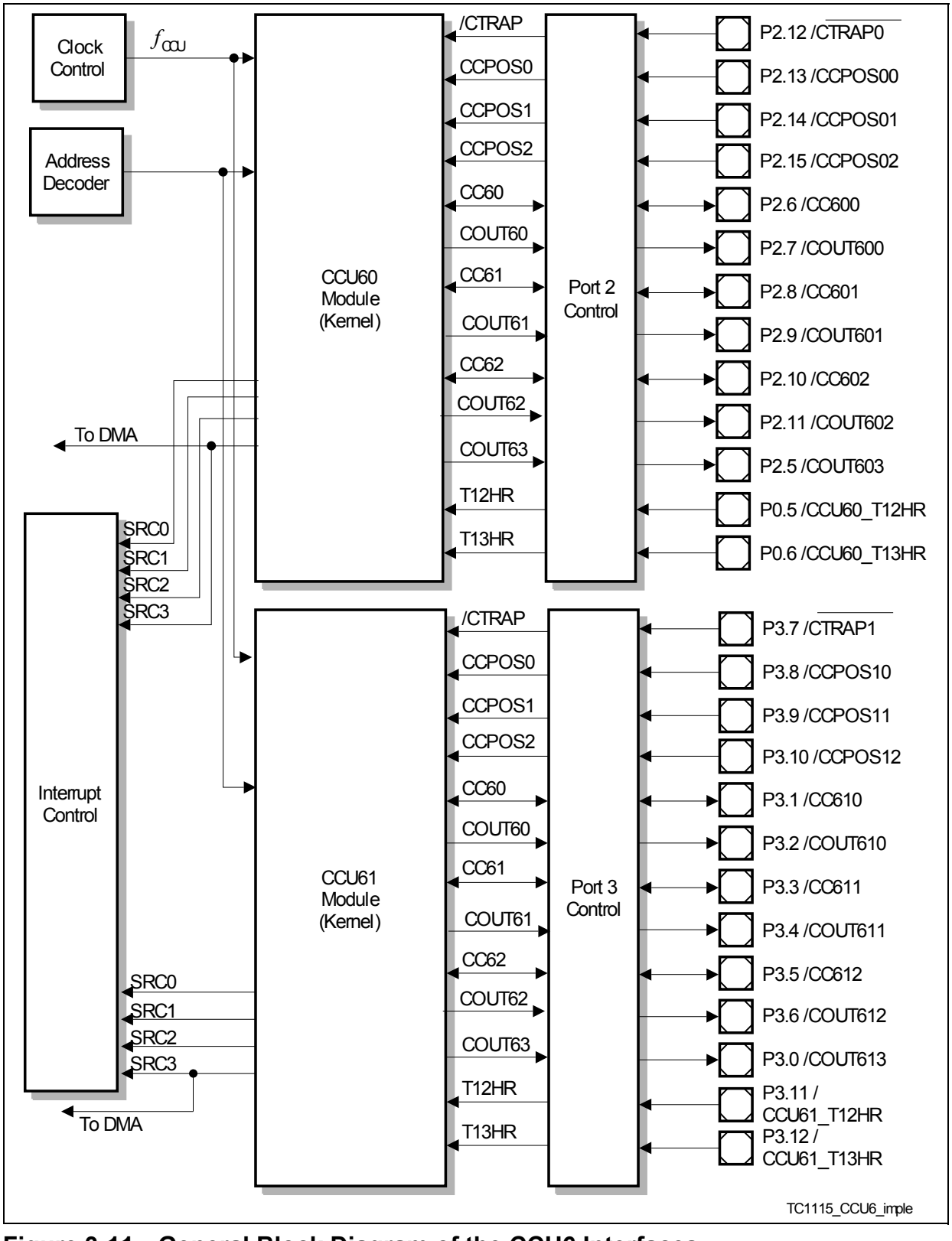


Figure 3-11 General Block Diagram of the CCU6 Interfaces

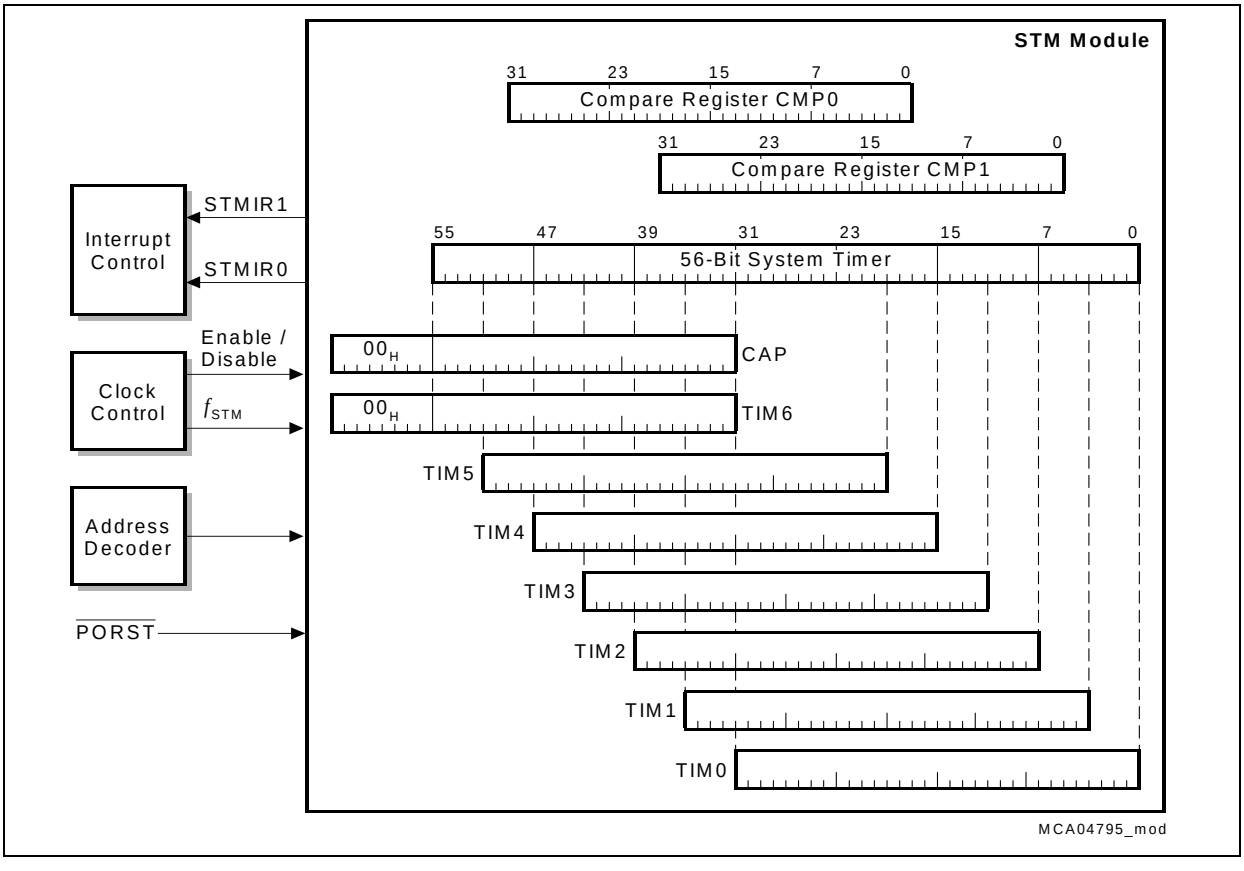


Figure 3-12 Block Diagram of the STM Module

3.17 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the TC1115 in a user-specified time period. When enabled, the WDT will cause the TC1115 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC1115 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

In addition to this standard “Watchdog” function, the WDT incorporates the ENDINIT feature and monitors its modifications. A system-wide line is connected to the ENDINIT bit implemented in a WDT control register, serving as an additional write-protection for critical registers (besides supervisor mode protection). Registers protected via this line can be modified only when supervisor mode is active and bit ENDINIT = 0.

A further enhancement in the TC1115’s Watchdog Timer is its reset prewarning operation. Instead of immediately resetting the device upon detection of an error, the WDT first issues a Non-Maskable Interrupt (NMI) to the CPU before finally resetting the device at a specified time period later. This gives the CPU a chance to save system state to memory for later examination of the cause of the malfunction, thus providing an important aid in debugging.

Features:

- 16-bit Watchdog counter
- Selectable input frequency: $f_{SYS}/256$ or $f_{SYS}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for time-out and prewarning modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated password access mechanism with fixed and user-definable password fields
- Proper access always requires two write accesses. The time between the two accesses is monitored by the WDT.
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation.
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation.
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled.
- Double Reset Detection: If a Watchdog induced reset occurs twice without a proper access to its control register in between, a severe system malfunction is assumed and the TC1115 is held in reset until a power-on reset. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed.

3.19 Boot Options

The TC1115 booting schemes provides a number of different boot options for the start of code execution. **Table 3-3** shows the boot options available in the TC1115.

Table 3-3 Boot Selections

$\overline{\text{BRKIN}}$[1]	$\overline{\text{TM}}$[1]	HWCFG [2:0]	Type of Boot	PC Start Value (User Entry)
1	1	000	**Bootstrap Loader** Serial boot from ASC to PMI scratch pad, run loaded program	DFFF FFFC$_H$[2] (D400 0000$_H$)
		001	**Bootstrap Loader** Serial boot from CAN to PMI scratch pad, run loaded program	
		010	**Bootstrap Loader** Serial boot from SSC to PMI scratch pad, run loaded program	
		011	External memory, EBU as master	DFFF FFFC$_H$[2] (A000 0000$_H$)
		100	External memory, EBU as slave	DFFF FFFC$_H$[2] (A000 0000$_H$)
		101	Reserved (STOP)	----
		110	PMI scratch pad	D400 0000$_H$
		111	Reserved (STOP)	DFFF FFFC$_H$[2]
1	0	000-111	Reserved (STOP)	DFFF FFFC$_H$[2]
0	1	000	Tristate chip	----
		001	Go to external emulator space	DFFF FFFC$_H$[2] (DE00 0000$_H$)
		010	Reserved (STOP)	----
		011	OSC and PLL Bypass	----
		100-111	Reserved (STOP)	DFFFFFFC$_H$[2]
0	0	000-111	Reserved (STOP)	DFFFFFFC$_H$[2]

1) This input signal is active low.

2) This is the BootROM entry address; the start address of user program in parentheses.

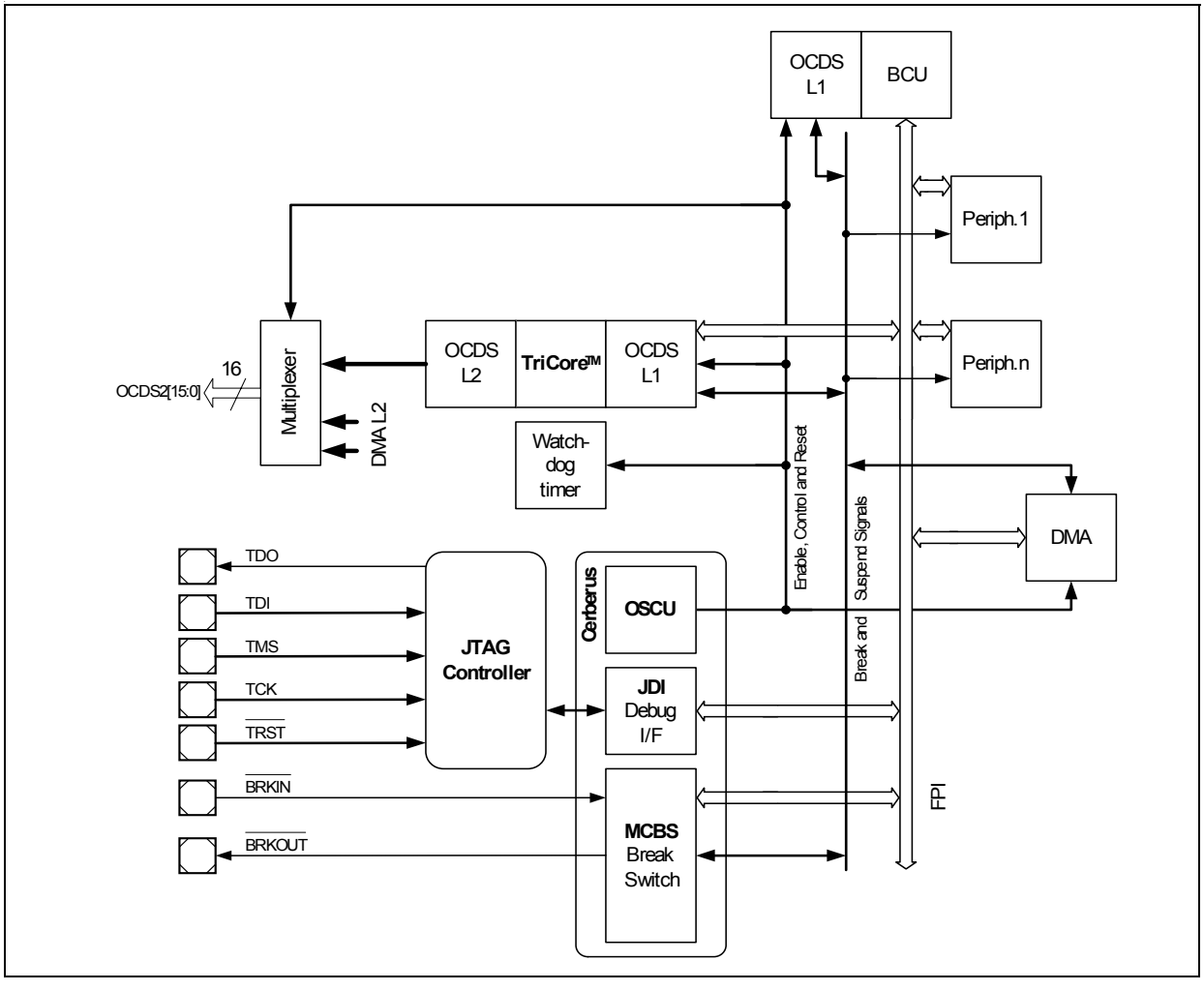


Figure 3-13 OCDS Support Basic Block Diagram

Table 3-5 Load Capacitors Select (cont'd)

Fundamental Mode Crystal Frequency (approx., MHz)	Load Capacitors C1, C2 (pF)
20	10
24	10

A block capacitor between V_{DDOSC3} and V_{SSOSC}, V_{DDOSC} and V_{SSOSC} is recommended, too.

4.2.3 IIC Characteristics

Each IIC Pin is an open drain output pin with different characteristics than other pins. The related characteristics are given in the following table.

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Output low voltage	V_{OL}	CC	–	0.4 0.6	V	3 mA sink current 6 mA sink current
Input high voltage[1)]	V_{IH}	SR	$0.7V_{DDP}$	$V_{DDP}+0.5$	V	–
Input low voltage[1)]	V_{IL}	SR	-0.5	$0.3V_{DDP}$	V	–

1) Not subject to production test, verified by design/characterization.

Note: No 5 V IIC interface is supported with these pads. Only voltages lower than 3.63 V must be applied to these pads.

Note: IIC pins have no pull-up and pull-down devices.

4.2.4 Power Supply Current

Parameter	Symbol	Limit Values		Unit	Test Conditions
		typ. [1]	max.		
Active mode supply current	I_{DD}	314	679	mA	Sum of I_{DDS} [2]
		153	345	mA	I_{DD} at V_{DD} [3]
		156	322	mA	I_{DD} at V_{DDP}
Idle mode supply current	I_{ID}	74	154	mA	Sum of I_{DDS} [2][4]
		66	130	mA	I_{DD} at V_{DD} [3][4]
		6	15	mA	I_{DD} at V_{DDP} [4]
Deep sleep mode supply current	I_{DS}	2	19	mA	Sum of I_{DDS} [2][5]
		2	19	mA	I_{DD} at V_{DD} [3][5]
		3.6	58	µA	I_{DD} at V_{DDP} [5]

1) Typical values are measured at 25°C, CPU clock at 150 MHz, and nominal supply voltage that is 3.3 V for V_{DDP}, V_{DDOSC3} and 1.5 V for V_{DD}, V_{DDOSC}. These currents are measured using a typical application pattern. The power consumption of modules can increase or decrease using other application programs.

2) These power supply currents are defined as the sum of all currents at the V_{DD} power supply lines: V_{DD} + V_{DDP} + V_{DDOSC3} + V_{DDOSC}

3) This measurement includes the TriCore™ and Logic power supply lines.

4) CPU is in idle state, input clocks to all peripherals are enabled.

5) Clock generation is disabled at the source.

4.3.6 Timing for JTAG Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
TCK clock period	t_{TCK}	SR	50	–	ns
TCK high time	t_1	SR	10	–	ns
TCK low time	t_2	SR	29	–	ns
TCK clock rise time	t_3	SR	–	0.4	ns
TCK clock fall time	t_4	SR	–	0.4	ns

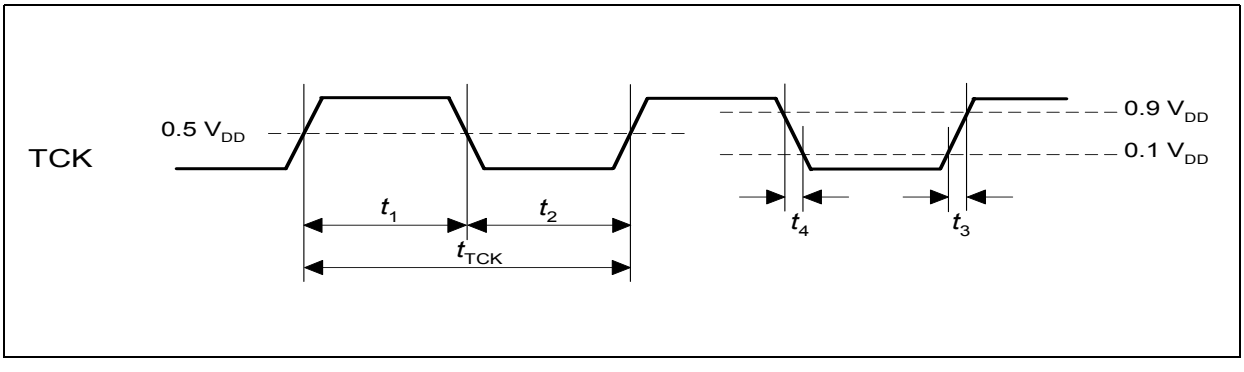


Figure 4-6 TCK Clock Timing

4.3.8 EBU Timings

4.3.8.1 SDCLKO Output Clock Timing

(Operating Conditions apply; CL = 50 pF)

Parameter	Symbol		Limits[1]		Limits[2]		Unit
			min	max	min	max	
SDCLKO period	t_1	CC	10	–	8.3	–	ns
SDCLKO high time	t_2	CC	3	–	2.5	–	ns
SDCLKO low time	t_3	CC	3	–	2.5	–	ns
SDCLKO rise time	t_4	CC	–	2.5	–	2.5	ns
SDCLKO fall time	t_5	CC	–	2.5	–	2.5	ns

1) The parameters are applicable for PC100 SDRAM access and the maximum SDCLKO is up to 100 MHz.

2) The parameters are applicable for PC133 SDRAM access and the maximum SDCLKO is up to 120 MHz.

4.3.8.2 BFCLKO Output Clock Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit [1]		Limit [2]		Unit
			min	max	min	max	
Clock period	t_1	CC	20	–	16.7	–	ns
BFCLKO high time	t_2	CC	6.6	–	7.5	–	ns
BFCLKO low time	t_3	CC	6.6	–	7.5	–	ns
BFCLKO rise time	t_4	CC	–	3.5	–	3.5	ns
BFCLKO fall time	t_5	CC	–	2.5	–	2.5	ns

1) The CPU runs at 150 MHz and the Burst Flash runs at divided by 3 clock.

2) The CPU runs at 120 MHz and the Burst Flash runs at divided by 2 clock.

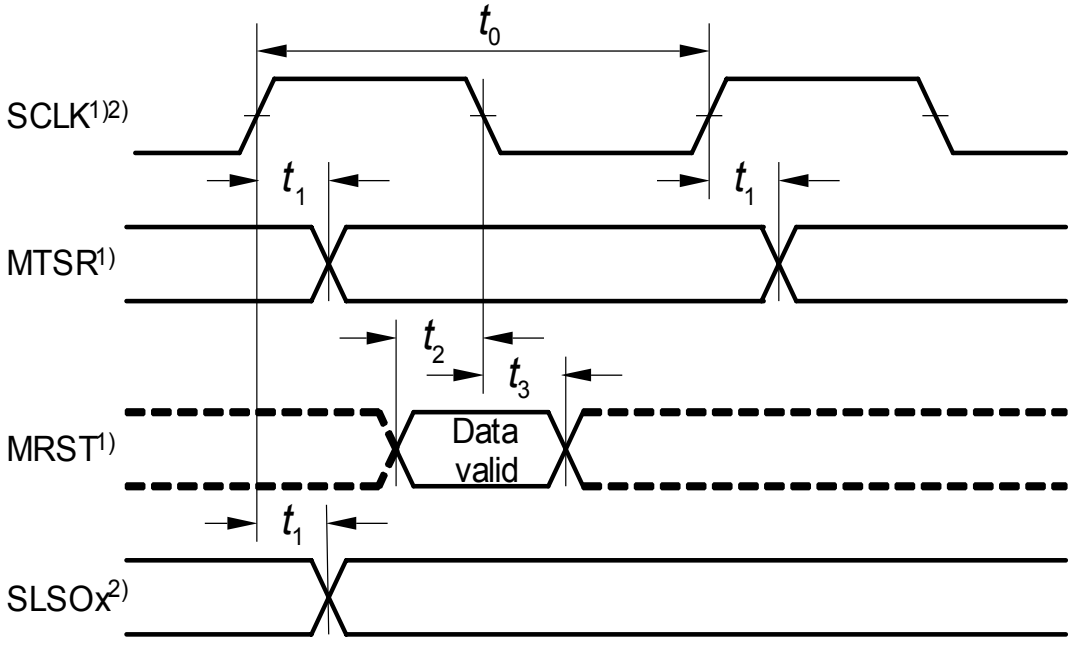
4.3.9 Peripheral Timings

4.3.9.1 SSC Master Mode Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit Values		Unit
			min.	max.	
SCLK clock period	t_0	CC	2*T_{SSC} [1]	–	ns
MTSR/SLSOx delay from SCLK ↓	t_1	CC	0	8	ns
MRST setup to SCLK ↓	t_2	SR	10	–	ns
MRST hold from SCLK ↓	t_3	SR	5	–	ns

1) $T_{SSCmin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 120MHz, t_0 = 16.7ns



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

2) The transition at SLSOx is based on the following setup: SSOTC.TRAIL = 0 and the first SCLK high pulse is in the first one of a transmission.

SSC_Tmg1

Figure 4-14 SSC Master Mode Timing

4.3.9.2 MLI Interface Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit Values		Unit
			min.	max.	
TCLK/RCLK clock period	t_0	CC/SR	2*T_{MLI} [1]	–	ns
MLI outputs delay from TCLK ↓	t_5	CC	0	8	ns
MLI inputs setup to RCLK ↓	t_6	SR	4	–	ns
MLI inputs hold to RCLK ↓	t_7	SR	4	–	ns
RREADY output delay from TCLK ↓	t_8	CC	0	8	ns

[1] $T_{MLImin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 120MHz, t_0 = 16.7ns

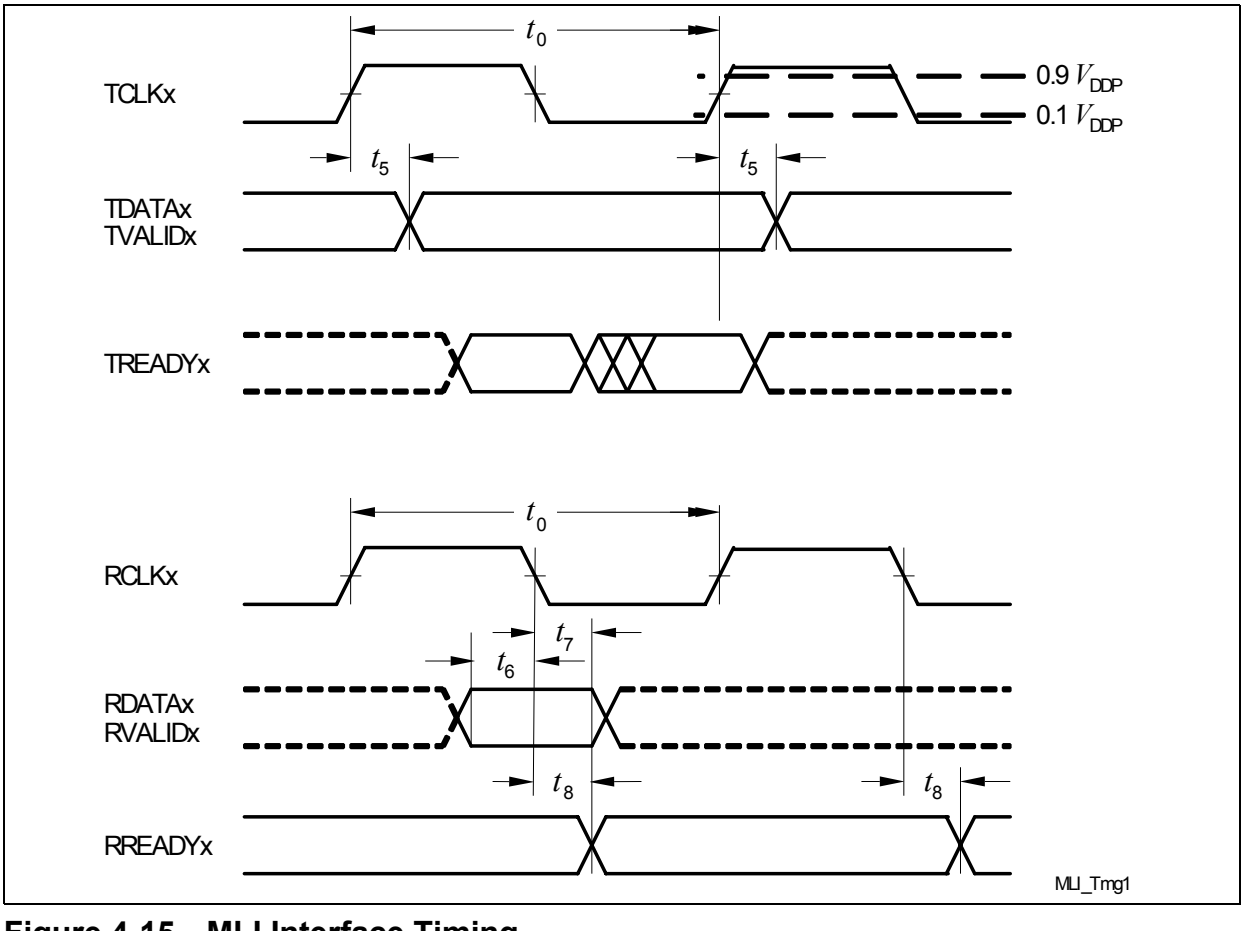


Figure 4-15 MLI Interface Timing

Note: The generation of RREADYx is in the input clock domain of the receiver. The reception of TREADYx is asynchronous to TCLKx.

5 Package Outline

Plastic Package, P-LBGA-208-2 (SMD)
(Low Profile Ball

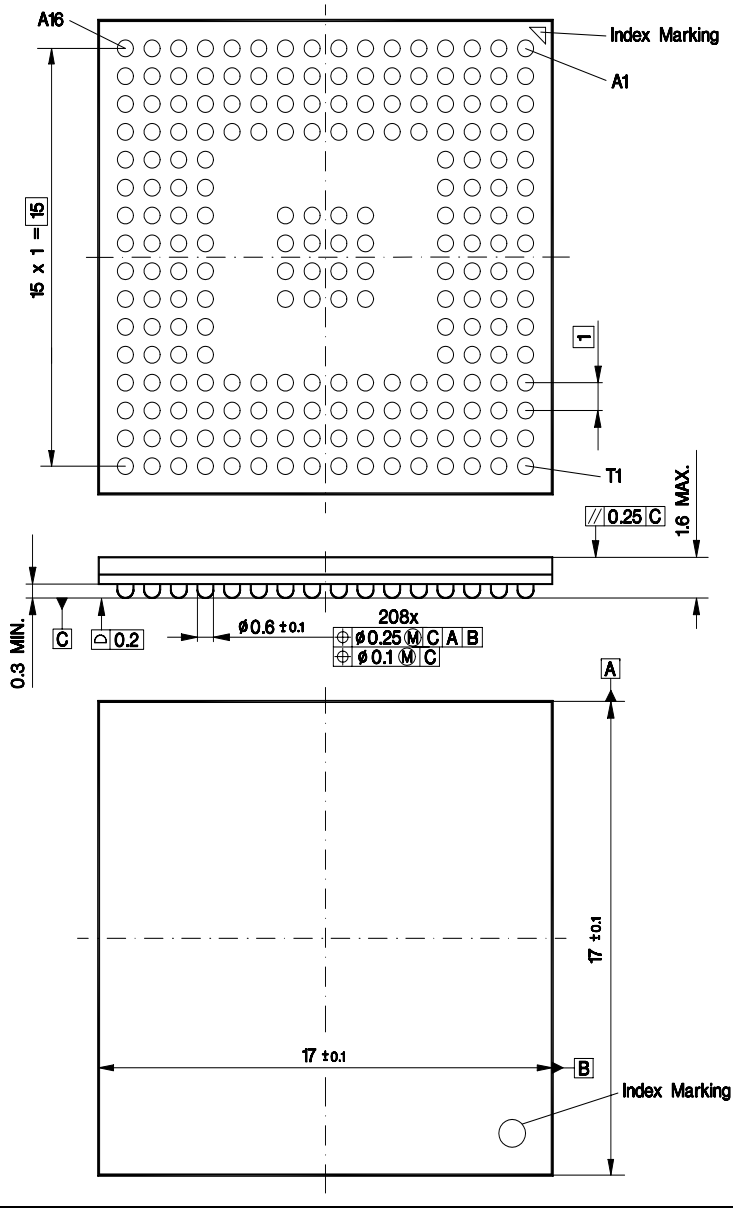


Figure 5-1 P-LBGA-208-2 Package

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm