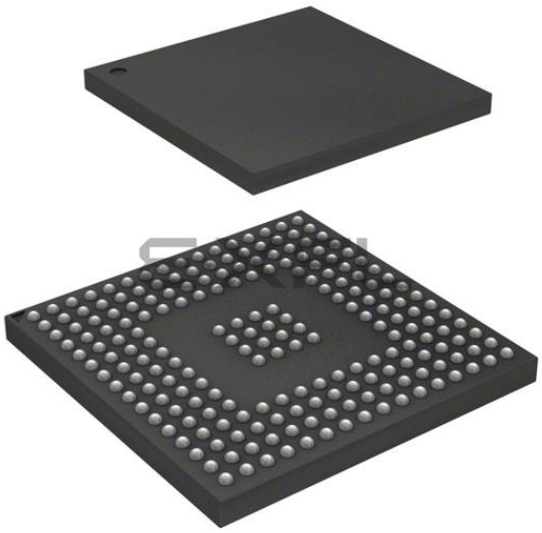
Infineon Technologies - SAF-TC1115-L100EB-G BB Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, FIFO, I²C, IrDA, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	144K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LBGA
Supplier Device Package	P-LBGA-208-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-tc1115-l100eb-g-bb

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In/ Out	PU/ PD[1]	Alternate Function	Function
P1.7	B13	I	PUC	SWCFG7	Software configuration 7
		O		OCDSA_7	OCDS L2 Debug Line A7
P1.8	A13	I	PUC	SWCFG8	Software configuration 8
		O		OCDSA_8	OCDS L2 Debug Line A8
P1.9	A14	I	PUC	SWCFG9	Software configuration 9
		O		OCDSA_9	OCDS L2 Debug Line A9
P1.10	B14	I	PUC	SWCFG10	Software configuration 10
		O		OCDSA_10	OCDS L2 Debug Line A10
P1.11	C14	I	PUC	SWCFG11	Software configuration 11
		O		OCDSA_11	OCDS L2 Debug Line A1
		O		SLSO0_1	SSC0 Slave Select output 1
P1.12	F13	I	PUC	SWCFG12	Software configuration 12
		O		OCDSA_12	OCDS L2 Debug Line A12
		O		SLSO1_1	SSC1 Slave Select output 1
P1.13	E14	I	PUC	SWCFG13	Software configuration 13
		O		OCDSA_13	OCDS L2 Debug Line A13
		O		SLSO0_2	SSC0 Slave Select output 2
P1.14	D14	O	PUC	SLSO1_2	SSC1 Slave Select output 2
		I		SWCFG14	Software configuration 14
		O		OCDSA_14	OCDS L2 Debug Line A14
P1.15	F14	I	PUC	SLSI0	SSC0 Slave Select Input
		O		RMW	EBU Read Modify Write
		I		SWCFG15	Software configuration 15
		O		OCDSA_15	OCDS L2 Debug Line A15

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In	Out	PU/PD[1]	Function	
P3			I/O		Port 3	
					Port 3 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for MLI1, CCU61, SSC0/1 and OCDS Level 2 debug lines.	
P3.0	A15		O	PUC	OCDSB_0	OCDS L2 Debug Line B0
			O		COUT61_3	CCU61 compare channel 3 output
P3.1	B15		O	PUC	OCDSB_1	OCDS L2 Debug Line B1
			I/O		CC61_0	CCU61 input/output of capture/ compare channel 0
P3.2	D15		O	PUC	OCDSB_2	OCDS L2 Debug Line B2
			O		COUT61_0	CCU61 output of capture/compare channel 0
P3.3	E15		O	PUC	OCDSB_3	OCDS L2 Debug Line B3
			I/O		CC61_1	CCU61 input/output of capture/ compare channel 1
P3.4	G14		O	PUC	OCDSB_4	OCDS L2 Debug Line B4
			O		COUT61_1	CCU61 output of capture/compare channel 1
P3.5	G15		O	PUC	OCDSB_5	OCDS L2 Debug Line B5
			I/O		CC61_2	CCU61 input/output of capture/ compare channel 2
P3.6	F15		O	PUC	OCDSB_6	OCDS L2 Debug Line B6
			O		COUT61_2	CCU61 output of capture/compare channel 2
P3.7	H14		O	PUC	OCDSB_7	OCDS L2 Debug Line B7
			I		CTRAP1	CCU61 trap input
			O		SLSO0_5	SSC0 Slave Select output 5
P3.8	C15		O	PUC	OCDSB_8	OCDS L2 Debug Line B8
			I		CCPOS1_0	CCU61 Hall input signal 0
			O		TCLK1	MLI1 transmit channel clock output
			O		SLSO1_5	SSC1 Slave Select output 5
P3.9	H15		O	PUC	OCDSB_9	OCDS L2 Debug Line B9
			I		CCPOS1_1	CCU61 Hall input signal 1
			I		TREADY1	MLI1 transmit channel ready input
			O		SLSO0_6	SSC0 Slave Select output 6
P3.10	B16		O	PUC	OCDSB_10	OCDS L2 Debug Line B10
			I		CCPOS1_2	CCU61 Hall input signal 2
			O		TVALID1	MLI1 transmit channel valid output
			O		SLSO1_6	SSC1 Slave Select output 6

Pin Definitions and Functions

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In	Out	PU/ PD[1]	Function
V_{SSOSC}	L15	—	—		Main Oscillator Ground
V_{DD}	G7 G8 G9 G10 G13 K7,K8 K9 K10	—	—		Core Logic Power Supply (1.5 V)
V_{DDP}	D4 D13 H4 J13 M4 N13	—	—		Pad Power Supply (3.3 V)
V_{SS}	E4 E13 H7 H8 H9 H10 H13 J4,J7 J8,J9 J10 M13 N4 R2,T2	—	—		Ground
N.C.	A1 A16 T1,R1 T14 T15 T16	—	—		Not Connected These pins must not be connected.

1) Refers to internal pull-up or pull-down device connected and corresponding type. The notation '—' indicates that the internal pull-up or pull-down device is not enabled.

Note: P2.12 to P2.15 are always configured as open drain.

3.2 Address Map

Table 3-1 defines the specific segment oriented address blocks of the TC1115 with its address range, size, and PMI/DMI access view. Table 3-2 shows the block address map of the Segment 15 which includes on-chip peripheral units and ports.

Table 3-1 TC1115 Block Address Map

Segment	Address Range	Size	Description	DMI Access	PMI Access	
0 – 7	0000 0000$_H$ – 7FFF FFFF$_H$	2 GB	MMU Space	via FPI	via FPI	cached
8	8000 0000$_H$ – 8FFF FFFF$_H$	256 MB	External Memory Space mapped from Segment 10	via LMB	via LMB	
9	9000 0000$_H$ – 9FDF FFFF$_H$	256 MB	Reserved	via FPI	via FPI	
10	A000 0000$_H$ – AFBF FFFF$_H$	252 MB	External Memory Space	via LMB	via LMB	non-cached
	AFC0 0000$_H$ – AFC0 FFFF$_H$	64 KB	DMU Space			
	AFC1 0000$_H$ – AFFF FFFF$_H$	~4 MB	Reserved			
11	B000 0000$_H$ – BFFF FFFF$_H$	256 MB	Reserved	via FPI	via FPI	
12	C000 0000$_H$ – C000 FFFF$_H$	64 KB	DMU	via LMB	via LMB	cached
	C001 0000$_H$ – CFFF FFFF$_H$	~ 256 MB	Reserved			

3.5 LMB External Bus Unit

The LMB External Bus Control Unit (EBU) of the TC1115 is the interface between external resources, like memories and peripheral units, and the internal resources connected to on-chip buses if enabled. The basic structure and external interconnections of the EBU are shown in Figure 3-1.

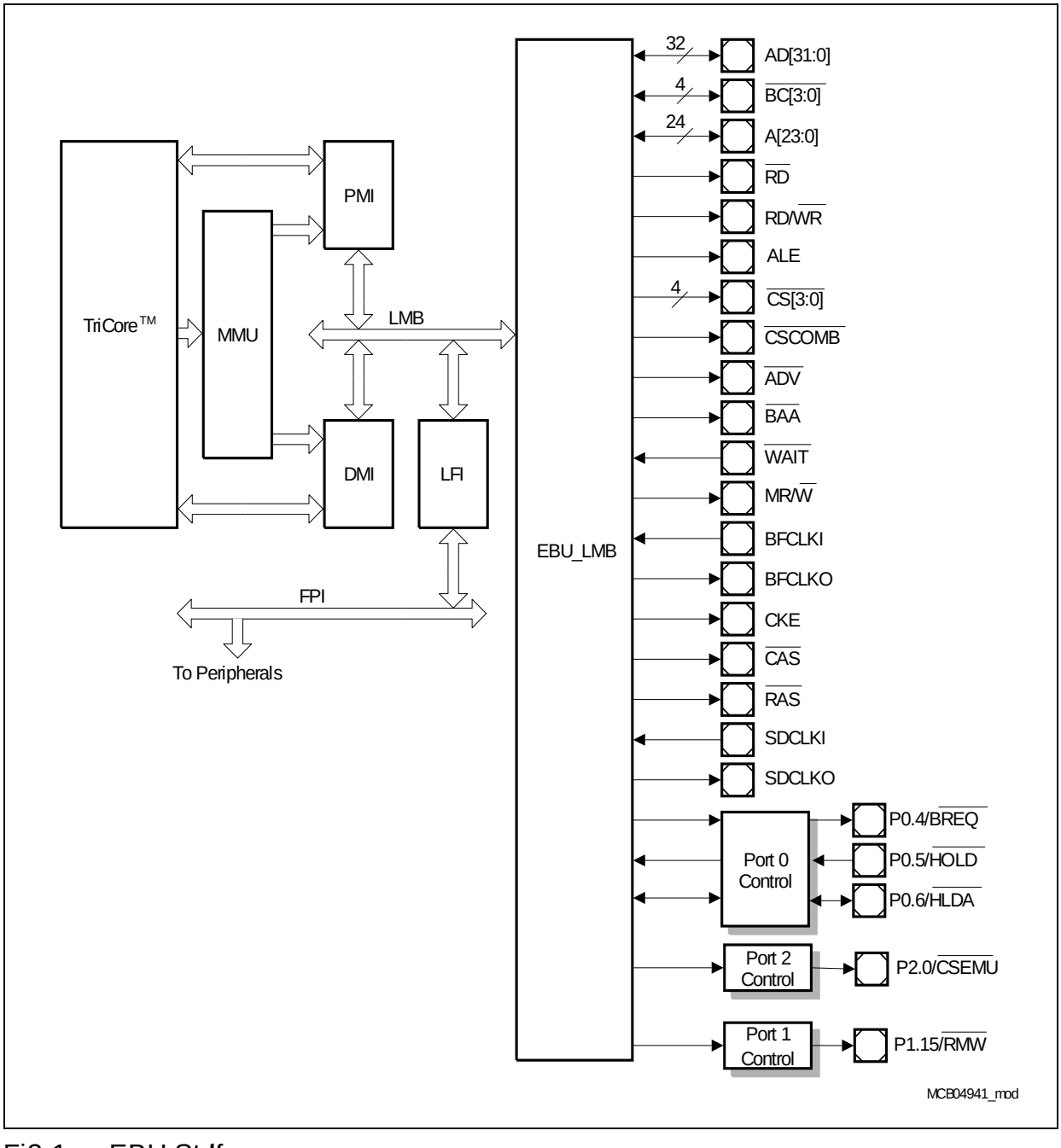

Figure 3-1 EBU Structure

Functional Description

3.9 Asynchronous/Synchronous Serial Interface (ASC)

Figure 3-5 shows a global view of the functional blocks of three Asynchronous/ Synchronous Serial interfaces (ASC0, ASC1 and ASC2).

Each ASC module (ASC0/ASC1/ASC2) communicates with the external world via one pair of I/O lines. The RXD line is the receive data input signal (in synchronous mode also output). TXD is the transmit output signal. Clock control, address decoding, and interrupt service request control are managed outside the ASC module kernel.

The Asynchronous/Synchronous Serial interfaces provide serial communication between the TC1115 and other microcontrollers, microprocessors or external peripherals.

Each ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In synchronous mode, data is transmitted or received synchronous to a shift clock which is generated by the ASC internally. In asynchronous mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud-rate generator provides the ASC with a separate serial clock signal that can be accurately adjusted by a prescaler implemented as a fractional divider.

Audio Functional Description

3.10 High-Speed Synchronous Serial Interface (SSC)

Figure 3-6 shows a global view of the functional blocks of two High-Speed Synchronous Serial interfaces (SSC0 and SSC1).

Each SSC supports full-duplex and half-duplex serial synchronous communication up to 37.5 MBaud (@ 75 MHz module clock) with receive and transmit FIFO support. The serial clock signal can be generated by the SSC itself (master mode) or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. Eight slave select inputs are available for slave mode operation. Eight programmable slave select outputs (chip selects) are supported in master mode.

Features

- Master and slave mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Baud rate generation minimum at 572.2 Baud (@ 75 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)
- Four-pin interface
- Flexible SSC pin configuration
- Up to eight slave select inputs in slave mode
- Up to eight programmable slave select outputs SLSO in master mode
  - Automatic SLSO generation with programmable timing
  - Programmable active level and enable control
- 4-stage receive FIFO (RXFIFO) and 4-stage transmit FIFO (TXFIFO)
  - Independent control of RXFIFO and TXFIFO
  - 2- to 16-bit FIFO data width
  - Programmable receive/transmit interrupt trigger level
  - Receive and transmit FIFO filling level indication
  - Overrun error generation
  - Underflow error generation

Auto

- Evaluation of the device address in slave mode
- Bus access arbitration in multimaster mode

Fea

- Extended buffer allows up to 4 send/receive data bytes to be stored
- Selectable baud rate generation
- Support of standard 100 kBaud and extended 400 kBaud data rates
- Operation in 7-bit addressing mode or 10-bit addressing mode
- Flexible control via interrupt service routines or by polling
- Dynamic access to up to 2 physical IIC buses

Micro Link Serial Bus Interface

The Micro Link Serial Bus Interface is dedicated to the serial communication between the other Infineon 32-bit controllers with MLI. The communication is intended to be fast due to an address translation system, and it is not necessary to have any special program in the second controller.

Features

- Serial communication from the MLI transmitter to MLI receiver of another controller
- Module supports connection of each MLI with up to four MLI from other controllers
- Fully transparent read/write access supported (= remote programming)
- Complete address range of target controller available
- Special protocol to transfer data, address offset, or address offset and data
- Error control using a parity bit
- 32-bit, 16-bit, and 8-bit data transfers
- Address offset width: from 1- to 16-bit
- Baud rate: f_{MLI} / 2 (symmetric shift clock approach),
  baud rate definition by the corresponding fractional divider

Architecture Functional Description

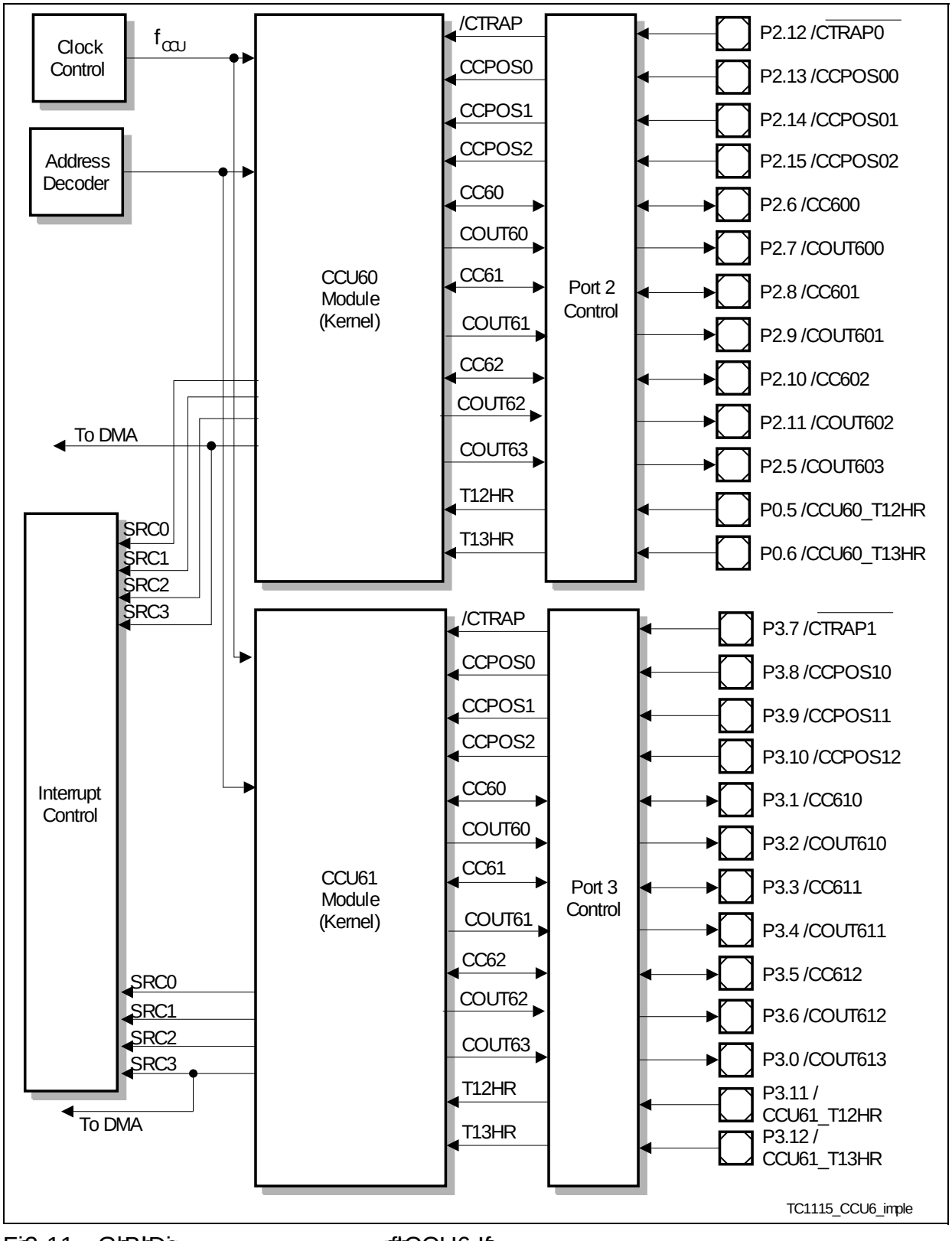

Figure 3-11 Block Diagram of CCU6 Interface

Audio Functional Description

The oscillator circuit, which is designed to work with an external crystal oscillator or an external stable clock source, consists of an inverting amplifier with XTAL1 as input and XTAL2 as output.

Figure 8-15 shows the recommended external oscillator circuitries for both operating modes, i.e. external crystal mode and external input clock mode.

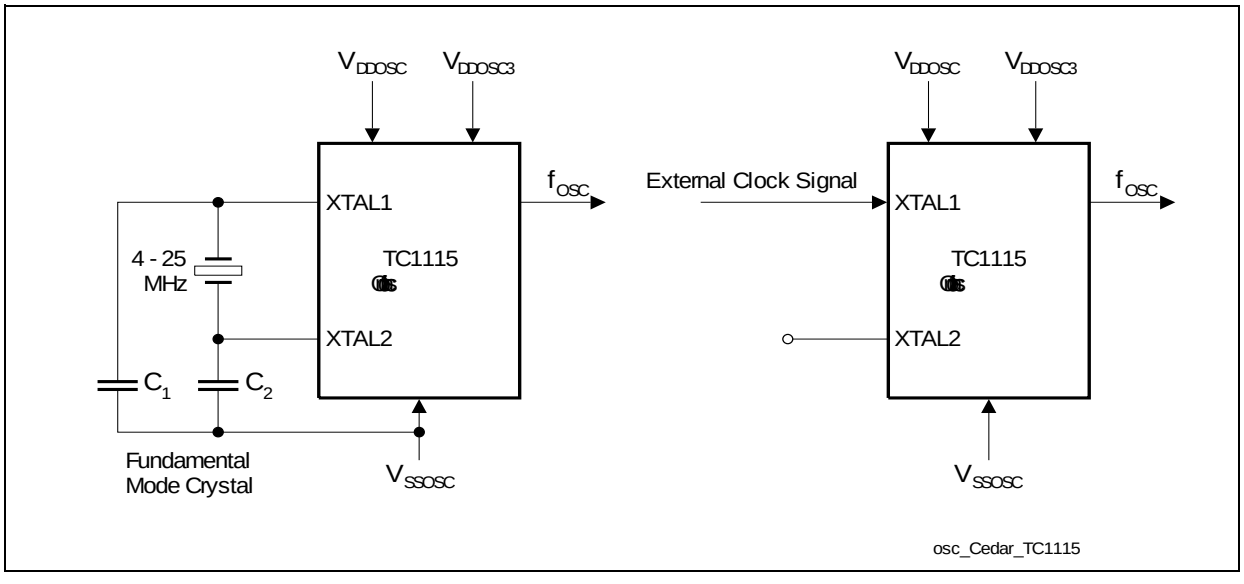

Figure 8-15 Oscillator Circuitry

When using an external clock signal, it must be connected to XTAL1 and XTAL2 is left open (unconnected). When supplying the clock signal directly, not using a crystal and the oscillator, the input frequency can be in the range of 0 - 40 MHz if the PLL is not used, 4 - 40 MHz in case the PLL is used.

When using a crystal, its frequency can be within the range of 4 MHz to 25 MHz. An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. It consists normally of the two load capacitances, C1 and C2. For some crystals, a series damp resistor may be necessary. The exact values and related operating range are dependant on the crystal and have to be determined and optimized together with the crystal vendor using the negative resistance method. As starting point for the evaluation and for non-productive systems, the following load capacitor values might be used.

Table 8-5 Load Capacitor Selection

Fundamental Mode Crystal Frequency (in MHz)	Load Capacitance C1, C2 (in pF)
4	33
8	18
12	12
16	10

Electrical Parameters

4.1.2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Note / Test Condition
		min.	max.		
Ambient temperature	T_A	-40	85	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	–
Junction temperature	T_J	-40	125	°C	under bias
Voltage at 1.5 V power supply pins with respect to V_{SS} [1]	V_{DD}	-0.5	1.7	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS} [2]	V_{DDP}	-0.5	4.0	V	–
Voltage on any pin with respect to V_{SS} [2]	V_{IN}	-0.5	4.0	V	–
Input current on any pin during overload condition	I_{IN}	-10	10	mA	–
Absolute sum of all input currents during overload condition	ΣI_{IN}	–	|100|	mA	–
CPU & LMB Bus Frequency	f_{SYS}	–	150	MHz	–
FPI Bus Frequency	f_{FPI}	–	100	MHz	–

1) Applicable for V_{DD} and V_{DDOSC}.

2) Applicable for V_{DDP} and V_{DDOSC3}. The maximum voltage difference must not exceed 4.0 V in any case (i.e. Supply Voltage = 4.0 V and Input Voltage = -0.5 V is not allowed).

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Electrical Parameters

4.2 DC Parameters

4.2.1 Input/Output Characteristics

V_{SS} = 0 V; T_A = -40°C to +125°C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
GPIO ports, DMU ports, EBU ports					
Input low voltage	V_{IL} SR	-0.3	0.8	V	LvTTL
Input high voltage	V_{IH} SR	2.0	V_{DDP} + 0.3	V	LvTTL
Output low voltage	V_{OL} CC	–	0.4	V	I_{OL} = 2mA
Output high voltage	V_{OH} CC	2.4	–	V	I_{OH} = -2mA
Pull-up current [1]	$\|I_{PUA}\|$ CC	–	149	µA	V_{IN} = 0V
	$\|I_{PUC}\|$ CC	–	7.2	µA	V_{IN} = 0V
Pull-down current [2]	$\|I_{PDA}\|$ CC	–	156	µA	V_{IN} = V_{DDP}
	$\|I_{PDC}\|$ CC	–	15.7	µA	V_{IN} = V_{DDP}
Input leakage current [3]	I_{OZ1} CC	–	±350	nA	0 < V_{IN} < V_{DDP}
Pin Capacitance [4]	C_{IO} CC	–	10	pF	f = 1 MHz T_A = 25 °C

1) The current is applicable to the pins, for which a pull-up has been specified. Refer to Table 2-1 . I_{PUx} refers to the pull-up current for type *x in absolute values*.

2) The current is applicable to the pins, for which a pull-down has been specified. Refer to Table 2-1 . I_{PDx} refers to the pull-down current for type *x in absolute values*.

3) Excluded following pins: $\overline{\text{NMI}}$, $\overline{\text{TRST}}$, TCK, TDI, TMS, ALE, P2.1, HWCFG0, HWCFG1, HWCFG2, BRKIN, PORST, HDRST.

4) Not subject to production test, verified by design/characterization

Advanced Electrical Parameters

4.3 AC Parameters

4.3.1 Power, Pad and Reset Timing

Parameter	Symbol	Limit Values		Unit	
		min.	max.		
Min. V_{DDP} voltage to ensure defined pad states[1]	V_{DDPPA}	CC	0.6	–	V
Oscillator start-up time[2]	t_{OSCS}	CC	–	30	ms
Minimum $\overline{\text{PORST}}$ active time after power supplies are stable at operating levels	t_{POA}	CC	50	–	ms
$\overline{\text{HDRST}}$ pulse width	t_{HD}	CC	1024 cycles[3]		f_{SYS}
Ports inactive after any reset active[2]	t_{PI}	CC	–	30	ns

1) This parameter is valid under assumption that PORST signal is constantly at low level during the power-up/ power-down of the V_{DDP}.

2) Not subject to production test, verified by design/characterization.

3) Any $\overline{\text{HDRST}}$ activation is internally prolonged to 1024 FPI bus clock cycles.

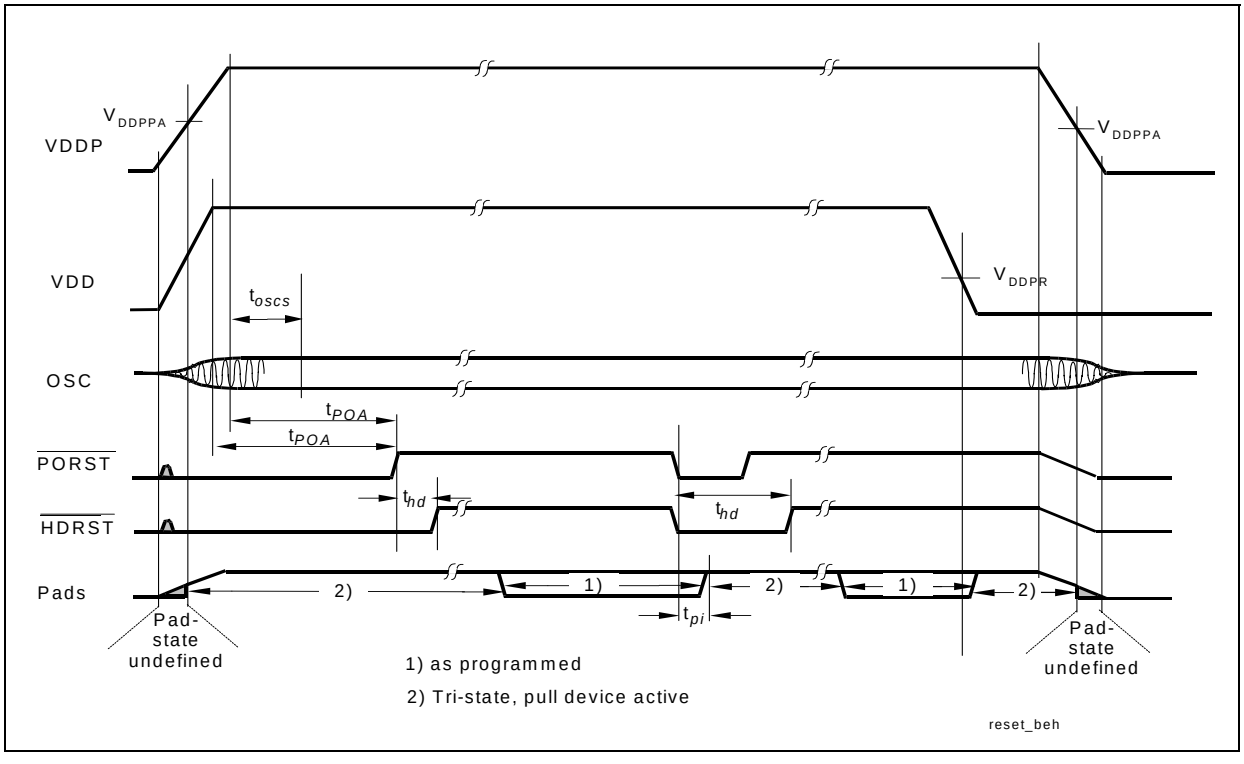

Fig 4-1 Pad Reset Timing

Au... Ele...

4.3.4 Input Clock Timing

(Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit
		min.	max.		
Oscillator clock frequency	with PLL	f_{OSC}	4	25	MHz
Input clock frequency driving at XTAL1	with PLL	f_{OSCDD}	-	40	MHz
Input Clock Duty Cycle (t_1 /t_2)			45	55	%

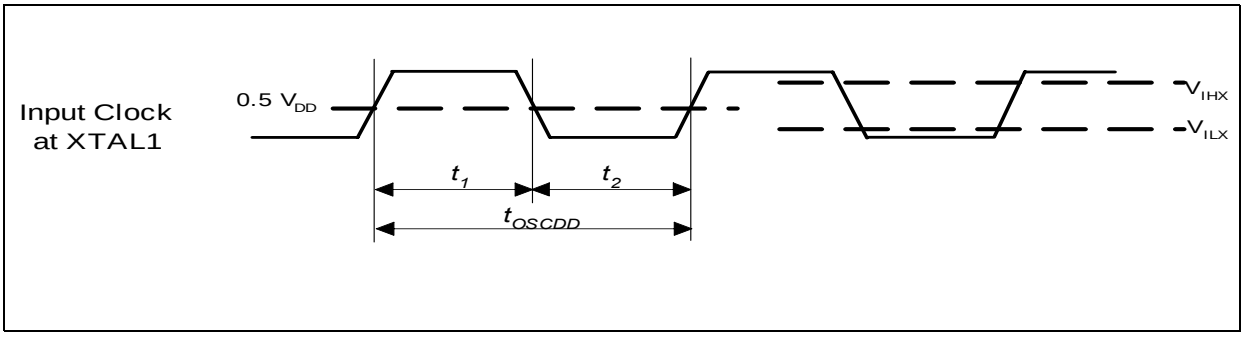

Fig... Input Clock Timing

4.3.5 PtoTign

(Operating Conditions apply; C_L = 50 pF)

Ptan	Sbyn		Lsn Uh		
			im	xan	
Port data valid from TRCLK [1] up to 120 MHz[2]	t_1	CC	–	13	ns

[1] Port data is output with respect to the FPI clock. The TRCLK is used as a reference here since the FPI clock is not available as an external pin and TRCLK is same frequency as CPU clock. Port lines maintain their states for at least 2 CPU clocks.

[2] 120 MHz is verified by design/characterization.

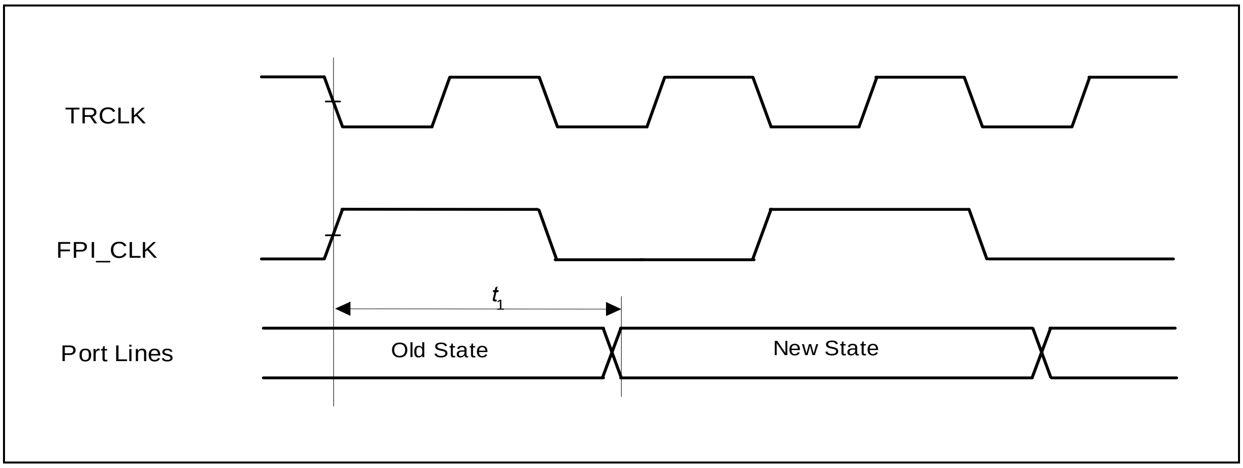

Fig4-5 PtoTign

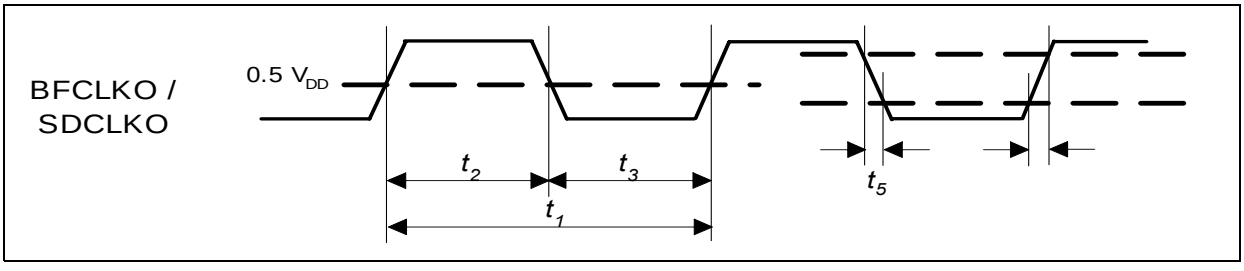

Figure 4-9 EBU Clock Output Timing

4.3.8.3 Timing for SDRAM Access

(Operating Conditions apply; C_L = 50 pF[1])

Parameter	Symbol	Limit Values				Unit
			[2]		[3]	
		min.	max.	min.	max.	
SDCLKO period	t_1 CC	10	–	8.3	–	ns
CKE output valid time from SDCLKO ↑	t_1 CC	–	8.0	–	6.8	ns
CKE output hold time from SDCLKO ↑	t_2 CC	0	–	0.8	–	ns
Address output valid time from SDCLKO ↑	t_3 CC	–	8.0	–	6.8	ns
Address output hold time from SDCLKO ↑	t_4 CC	1.0	–	0.8	–	ns
$\overline{CS}$x, $\overline{RAS}$, $\overline{CAS}$, RD/$\overline{WR}$, $\overline{BC(3:0)}$ output valid time from SDCLKO ↑	t_5 CC	–	8.0	–	6.8	ns
$\overline{CS}$x, $\overline{RAS}$, $\overline{CAS}$, RD/$\overline{WR}$, $\overline{BC(3:0)}$ output hold time from SDCLKO ↑	t_6 CC	1.0	–	0.8	–	ns
AD(31:0) output valid time from SDCLKO ↑	t_7 CC	–	8.0	–	6.8	ns
AD(31:0) output hold time from SDCLKO ↑	t_8 CC	1.0	–	0.8	–	ns
AD(31:0) input setup time to SDCLKO ↑	t_9 SR	4.0	–	2.9	–	ns
AD(31:0) input hold time from SDCLKO ↑	t_{10} SR	3.0	–	3.0	–	ns

1) If application conditions other than 50 pf capacitive load are used, then the proper correlation factor should be used for your specific application condition. For design team, the load should be set according to the system requirement.

2) The parameters are applicable for PC100 SDRAM access and the maximum SDCLKO is up to 100 MHz.

3) The parameters are applicable for PC133 SDRAM access and the maximum SDCLKO is up to 120 MHz.

5 Package Outlines

P-LBGA-208-2 (SMD)
(Low Profile Ball Grid Array Package)

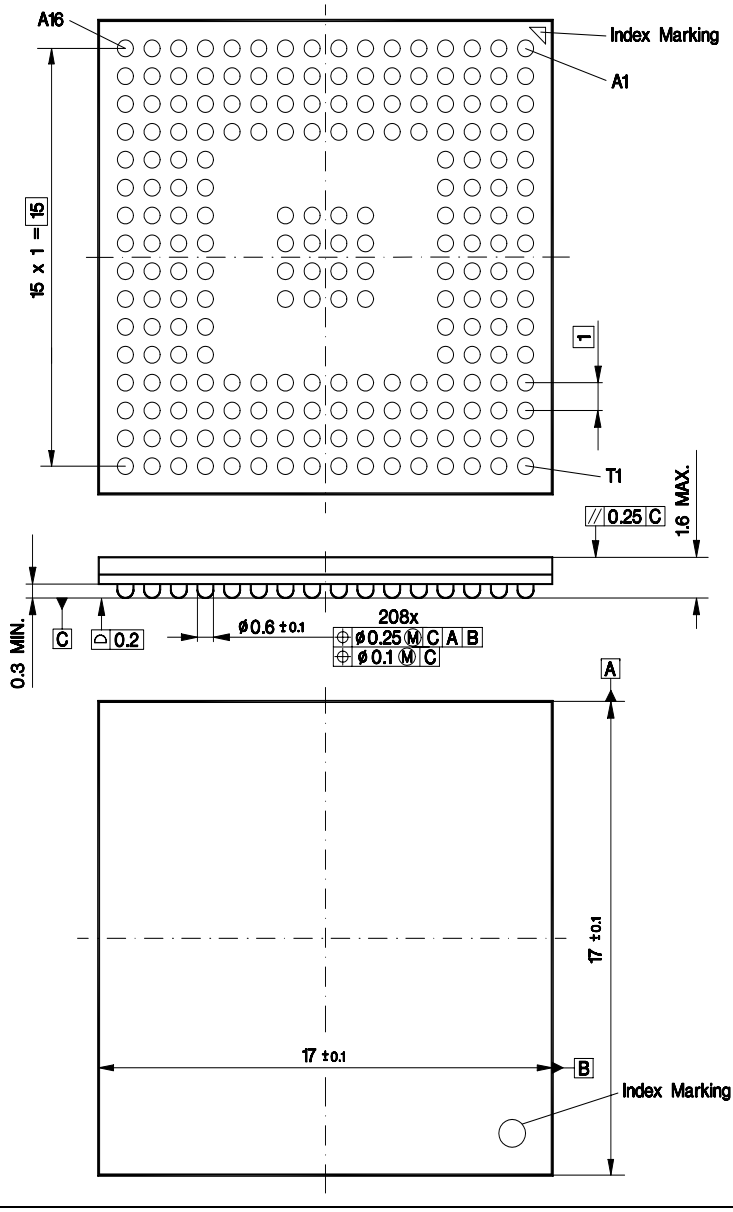

Fig 5-1 P-LBGA-208-2 Package

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm