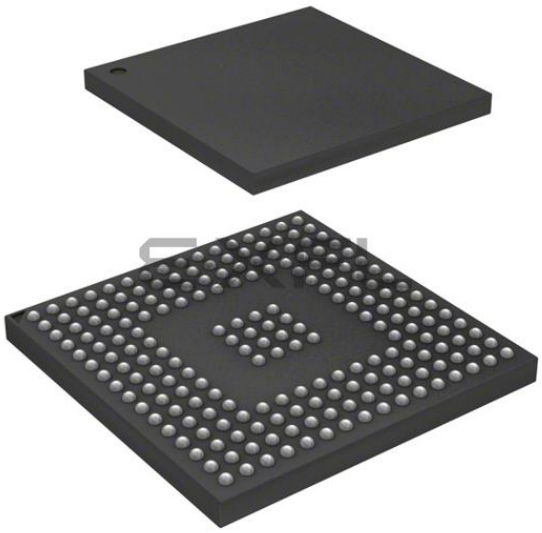
Infineon Technologies - SAF-TC1115-L150EB BB Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, FIFO, I²C, IrDA, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	144K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LBGA
Supplier Device Package	P-LBGA-208-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-tc1115-l150eb-bb

TC1115

32-Bit Single-Chip Microcontroller

Advance Information

Microcontrollers

Never stop thinking.

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
$\overline{CS0}$ **$\overline{CS1}$** **$\overline{CS2}$** **$\overline{CS3}$**	D9 D8 C9 B8	O O O O	PUC PUC PUC PUC	**EBU Chip Select Output Line 0** **EBU Chip Select Output Line 1** **EBU Chip Select Output Line 2** **EBU Chip Select Output Line 3** Each corresponds to a programmable region. Only one can be active at one time.
$\overline{CSCOMB}$	N3	O	PUC	**EBU Chip Select Output for combination function (Overlay Memory and Global)**
SDCLKI	J1	I	—	**SDRAM Clock Input (Clock Feedback)**
SDCLKO	H1	O	—	**SDRAM Clock Output** Accesses to SDRAM devices are synchronized to this clock.
$\overline{RAS}$	D6	O	PUC	**EBU SDRAM Row Address Strobe Output**
$\overline{CAS}$	D5	O	PUC	**EBU SDRAM Column Address Strobe Output**
CKE	L4	O	PUC	**EBU SDRAM Clock Enable Output**
BFCLKI	D1	I	—	**Burst Flash Clock Input (Clock Feedback)**
BFCLKO	E1	O	—	**Burst Flash Clock Output** Accesses to Burst Flash devices are synchronized to this clock.
$\overline{RD}$	P2	O	PUC	**EBU Read Control Line** Output in master mode Input in slave mode
RD/$\overline{WR}$	T3	O	PUC	**EBU Write Control Line** Output in master mode Input in slave mode
$\overline{WAIT}$	B9	I	PUC	**EBU Wait Control Line**
ALE	R3	O	PDC	**EBU Address Latch Enable Output**
MR/$\overline{W}$	P3	O	PUC	**EBU Motorola-style Read/Write Output**
$\overline{BAA}$	A11	O	PUC	**EBU Burst Address Advance Output** For advancing address in a Burst Flash access
$\overline{ADV}$	B11	O	PUC	**EBU Burst Flash Address Valid Output**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
				EBU Address Bus Input/Output Lines
A0	K1	O	PUC	EBU Address Bus Line 0
A1	L1	O	PUC	EBU Address Bus Line 1
A2	M1	O	PUC	EBU Address Bus Line 2
A3	N1	O	PUC	EBU Address Bus Line 3
A4	P1	O	PUC	EBU Address Bus Line 4
A5	J2	O	PUC	EBU Address Bus Line 5
A6	K2	O	PUC	EBU Address Bus Line 6
A7	L2	O	PUC	EBU Address Bus Line 7
A8	M2	O	PUC	EBU Address Bus Line 8
A9	N2	O	PUC	EBU Address Bus Line 9
A10	J3	O	PUC	EBU Address Bus Line 10
A11	K3	O	PUC	EBU Address Bus Line 11
A12	L3	O	PUC	EBU Address Bus Line 12
A13	M3	O	PUC	EBU Address Bus Line 13
A14	K4	O	PUC	EBU Address Bus Line 14
A15	A8	O	PUC	EBU Address Bus Line 15
A16	A9	O	PUC	EBU Address Bus Line 16
A17	A10	O	PUC	EBU Address Bus Line 17
A18	B10	O	PUC	EBU Address Bus Line 18
A19	C10	O	PUC	EBU Address Bus Line 19
A20	D10	O	PUC	EBU Address Bus Line 20
A21	T4	O	PUC	EBU Address Bus Line 21
A22	R4	O	PUC	EBU Address Bus Line 22
A23	P4	O	PUC	EBU Address Bus Line 23
XTAL1	M16	I	—	**Oscillator/PLL/Clock Generator Input/Output Pins**
XTAL2	N16	O	—	XTAL1 is the input to the main oscillator amplifier and input to the internal clock generator. XTAL2 is the output of the main oscillator amplifier circuit. For clocking of the device from an external source, XTAL1 is driven with the clock signal while XTAL2 is left unconnected. For crystal oscillator operation, XTAL1 and XTAL2 are connected to the crystal with the appropriate recommended oscillator circuitry.
V_{DDOSC3}	P16	—	—	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC3}	R16	—	—	**Main Oscillator Ground**
V_{DDOSC}	L16	—	—	**Main Oscillator Power Supply (1.5 V)**

Table 3-2 Block Address Map of Segment 15 (cont'd)

Symbol	Description	Address Range	Size
–	Reserved	F010 0700$_H$ - F010 BFFF$_H$	–
MLI0	Micro Link Interface 0	F010 C000$_H$ - F010 C0FF$_H$	256 Bytes
MLI1	Micro Link Interface 1	F010 C100$_H$ - F010 C1FF$_H$	256 Bytes
MCHK	Memory Checker	F010 C200$_H$ - F010 C2FF$_H$	256 Bytes
–	Reserved	F010 C300$_H$ - F01D FFFF$_H$	–
MLI0_ SP0	MLI0 Small Transfer Window 0	F01E 0000$_H$ - F01E 1FFF$_H$	8 Kbytes
MLI0_ SP1	MLI0 Small Transfer Window 1	F01E 2000$_H$ - F01E 3FFF$_H$	8 Kbytes
MLI0_ SP2	MLI0 Small Transfer Window 2	F01E 4000$_H$ - F01E 5FFF$_H$	8 Kbytes
MLI0_ SP3	MLI0 Small Transfer Window 3	F01E 6000$_H$ - F01E 7FFF$_H$	8 Kbytes
MLI1_ SP0	MLI1 Small Transfer Window 0	F01E 8000$_H$ - F01E 9FFF$_H$	8 Kbytes
MLI1_ SP1	MLI1 Small Transfer Window 1	F01E A000$_H$ - F01E BFFF$_H$	8 Kbytes
MLI1_ SP2	MLI1 Small Transfer Window 2	F01E C000$_H$- F01E DFFF$_H$	8 Kbytes
MLI1_ SP3	MLI1 Small Transfer Window 3	F01E E000$_H$ - F01E FFFF$_H$	8 Kbytes
–	Reserved	F01F 0000$_H$ - F01F FFFF$_H$	–
MLI0_ LP0	MLI0 Large Transfer Window 0	F020 0000$_H$ - F020 FFFF$_H$	64 Kbytes
MLI0_ LP1	MLI0 Large Transfer Window 1	F021 0000$_H$ - F021 FFFF$_H$	64 Kbytes
MLI0_ LP2	MLI0 Large Transfer Window 2	F022 0000$_H$ - F022 FFFF$_H$	64 Kbytes
MLI0_ LP3	MLI0 Large Transfer Window 3	F023 0000$_H$ - F023 FFFF$_H$	64 Kbytes
MLI1_ LP0	MLI1 Large Transfer Window 0	F024 0000$_H$ - F024 FFFF$_H$	64 Kbytes
MLI1_ LP1	MLI1 Large Transfer Window 1	F025 0000$_H$ - F025 FFFF$_H$	64 Kbytes

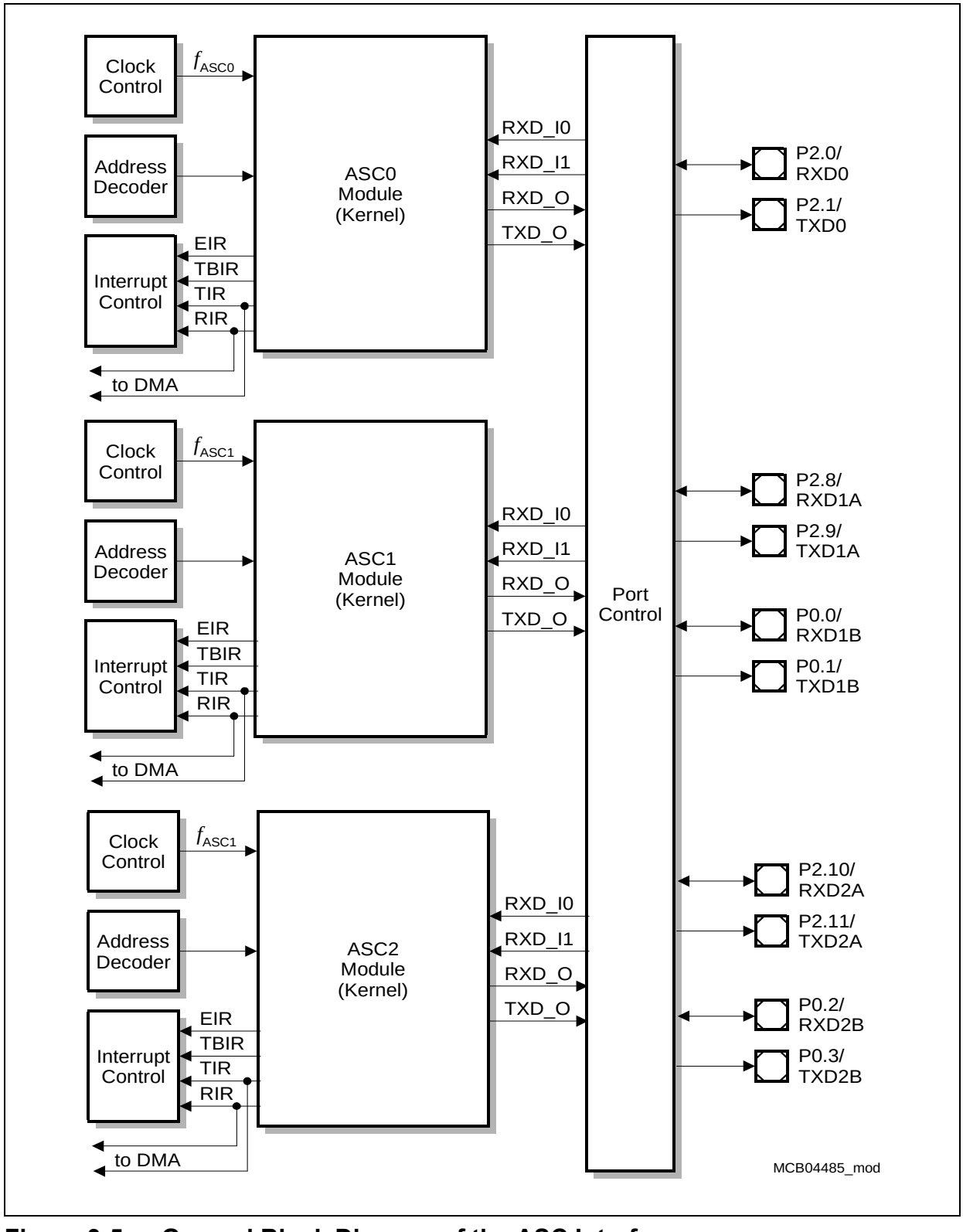


Figure 3-5 General Block Diagram of the ASC Interfaces

Features:

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baud rate from 4.6875 MBaud to 1.1 Baud (@ 75 MHz clock)
- Multiprocessor mode for automatic address/data byte detection
- Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 9.375 MBaud to 762.9 Baud (@ 75 MHz clock)
- Support for IrDA data transmission up to 115.2 kBaud maximum
- Double buffered transmitter/receiver
- Interrupt generation
  - On a transmitter buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receiver buffer full condition
  - On an error condition (frame, parity, overrun error)
- FIFO
  - 8-byte receive FIFO (RXFIFO)
  - 8-byte transmit FIFO (TXFIFO)
  - Independent control of RXFIFO and TXFIFO
  - 9-bit FIFO data width
  - Programmable Receive/Transmit Interrupt Trigger Level
  - Receive and Transmit FIFO filling level indication
  - Overrun error generation
  - Underflow error generation

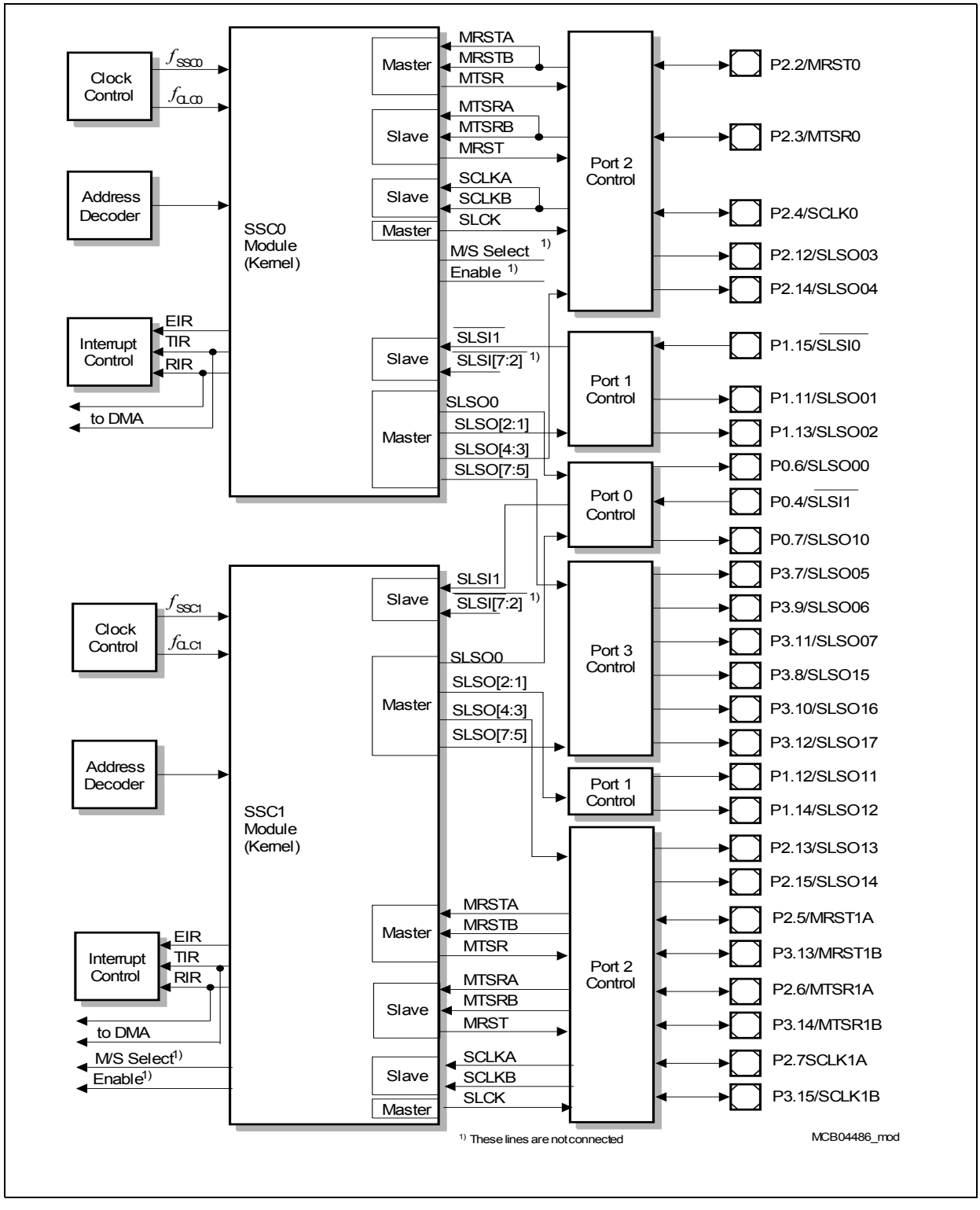


Figure 3-6 General Block Diagram of the SSC Interfaces

  - Static Allocation Commands offer compatibility with TwinCAN applications, which are not list based.
- Advanced Interrupt Handling:
  - Up to 16 interrupt output lines are available. Most interrupt requests can be individually routed to one of the 16 interrupt output lines.
  - Message postprocessing notifications can be flexibly aggregated into a dedicated register field of 256 notification bits.

3.15 Capture/Compare Unit 6 (CCU6)

Figure 3-11 shows a global view of the functional blocks of two Capture/Compare Units (CCU60 and CCU61).

Both of the CCU6 modules are further supplied by clock control, interrupt control, address decoding, and port control logic. One DMA request can be generated by each CCU6 module.

Each CCU6 provides two independent timers (T12, T13), which can be used for PWM generation, especially for AC-motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features:

- Three capture/compare channels, each channel can be used either as capture or as compare channel.
- Generation of a three-phase PWM supported (six outputs, individual signals for highside and lowside switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode

Timer 13 Features:

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported

Additional Features:

- Block commutation for Brushless DC-drives implemented
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

3.20 Power Management System

The TC1115 power management system allows software to configure the various processing units to adjust automatically in order to draw the minimum necessary power for the application.

There are four power management modes:

- Run Mode
- Idle Mode
- Sleep Mode
- Deep Sleep Mode

Table 3-4 describes the features of the power management modes.

Table 3-4 Power Management Mode Summary

Mode	Description
Run	The system is fully operational. All clocks and peripherals are enabled, as determined by software.
Idle	The CPU clock is disabled, waiting for a condition to return it to run mode. Idle mode can be entered by software when the processor has no active tasks to perform. All peripherals remain powered and clocked. Processor memory is accessible to peripherals. A reset, Watchdog Timer event, a falling edge on the $\overline{\text{NMI}}$ pin, or any enabled interrupt event will return the system to run mode.
Sleep	The system clock continues to be distributed only to those peripherals programmed to operate in sleep mode. The other peripheral modules will be shut down by the suspend signal. Interrupts from operating peripherals, the Watchdog Timer, a falling edge on the $\overline{\text{NMI}}$ pin, or a reset event will return the system to run mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.
Deep Sleep	The system clock is shut off; only an external signal will restart the system. Entering this state requires an orderly shut-down controlled by the Power Management State Machine (PMSM).

Besides these explicit software-controlled power-saving modes, special attention has been paid in the TC1115 to automatic power-saving in operating units that are currently not required or idle. In this case, they are shut off automatically until their operation is required again.

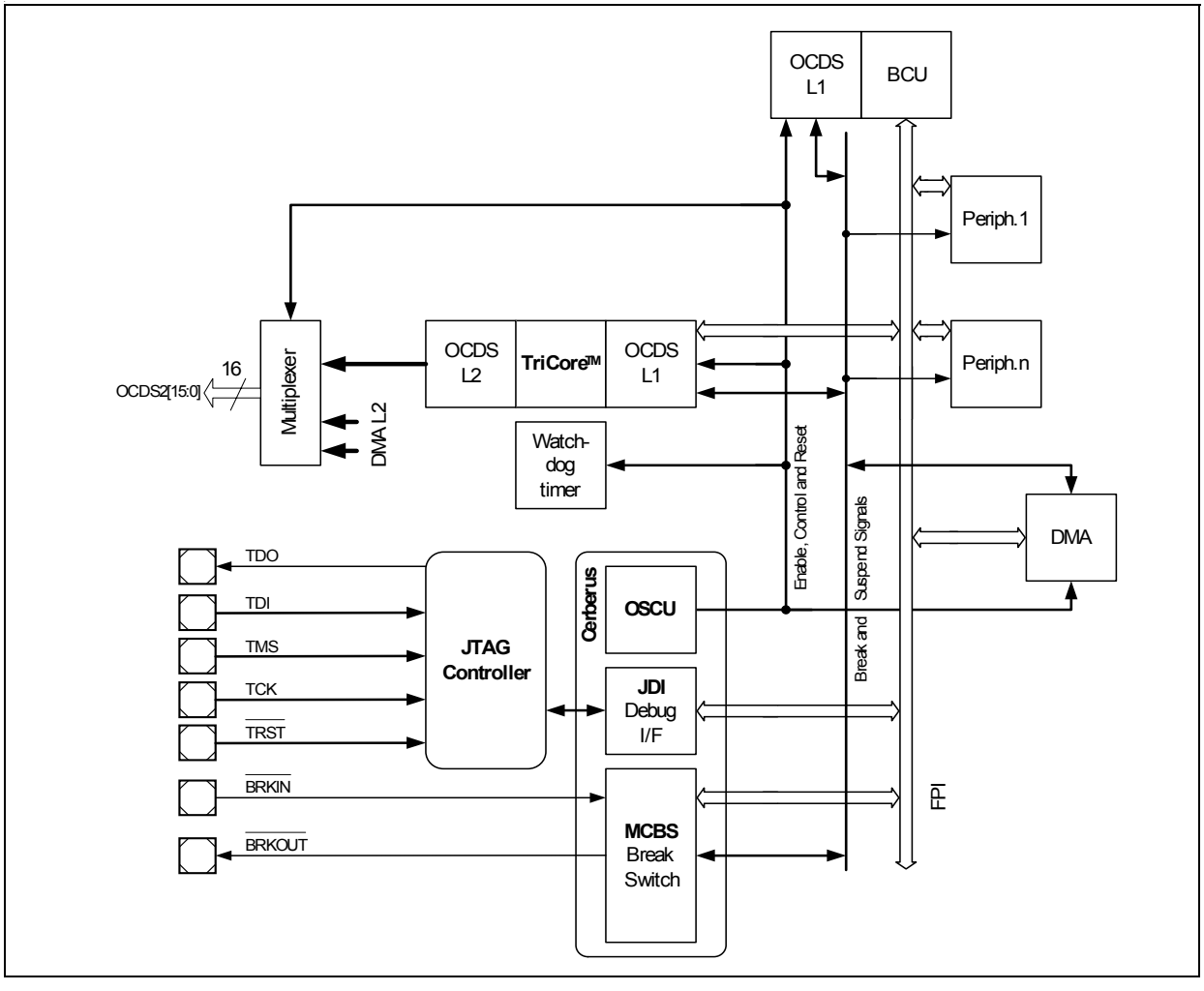


Figure 3-13 OCDS Support Basic Block Diagram

3.23 Power Supply

The TC1115 provides an ingenious power supply concept in order to improve the EMI behavior as well as to minimize the crosstalk within on-chip modules.

Figure 3-16 shows the TC1115's power supply concept, where certain logic modules are individually supplied with power. This concept improves the EMI behavior by reduction of the noise cross coupling.

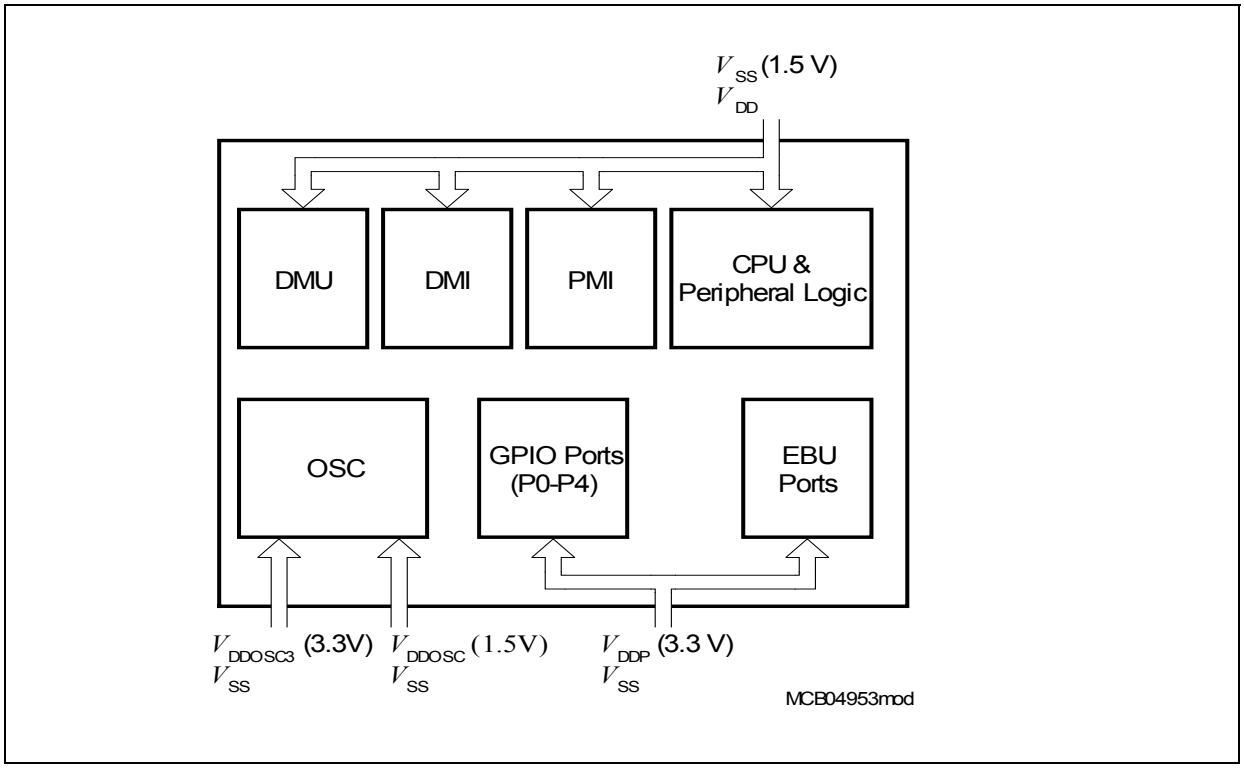


Figure 3-16 TC1115 Power Supply Concept

4 Electrical Parameters

4.1 General Parameters

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the TC1115 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for design purposes, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the TC1115 and must be considered for system design.
- **SR**
  These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the TC1115 is included.

4.3.2 PLL Parameters

When PLL operation is configured (*PLL_CLC.LOCK = 1*), the on-chip phase locked loop is enabled and provides the master clock. The PLL multiplies the input frequency by the factor **F** ($f_{MC} = f_{OSC} \times$ **F**) which results from the input divider, the multiplication factor (N Factor), and the output divider (**F** = *NDIV+1 / (PDIV+1* $\times$ *KDIV+1)*). The PLL circuit synchronizes the master clock to the input clock. This synchronization is done smoothly, i.e. the master clock frequency does not change abruptly.

Due to this adaptation to the input clock, the frequency of f_{MC} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{MC} which also affects the duration of individual TCMs.

The timing listed in the AC Characteristics refers to TCPs. Because f_{CPU} is derived from f_{MC}, the timing must be calculated using the minimum TCP possible under the respective circumstances.
The actual minimum value for TCP depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency in order to correspond to the applied input frequency (crystal or oscillator), the relative deviation for periods of more than one TCP is lower than for one single TCP (see formula and **Figure 4-2**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baud rates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler (K = *KDIV*+1) to generate the master clock signal f_{MC}. Therefore, the number of VCO cycles can be represented as K $\times$ N, where N is the number of consecutive f_{MC} cycles (TCM).

For a period of N $\times$ TCM, the accumulated PLL jitter is defined by the corresponding deviation D_N:

D_N [ns] = $\pm(1.5 + 6.32 \times N / f_{MC})$; f_{MC} in [MHz], N = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: $D_3 = \pm(1.5 + 6.32 \times 3 / 20) = 2.448$ ns.

This formula is applicable for K $\times$ N < 95. For longer periods, the K$\times N$=95 value can be used. This steady value can be approximated by: D_{Nmax} [ns] = $\pm(1.5 + 600 / (K \times f_{MC}))$.

4.3.5 Port Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol	Limits		Unit
		min	max	
Port data valid from TRCLK [1] up to 120 MHz[2]	t_1 CC	–	13	ns

[1] Port data is output with respect to the FPI clock. The TRCLK is used as a reference here since the FPI clock is not available as an external pin and TRCLK is same frequency as CPU clock. Port lines maintain their states for at least 2 CPU clocks.

[2] 120 MHz is verified by design/characterization.

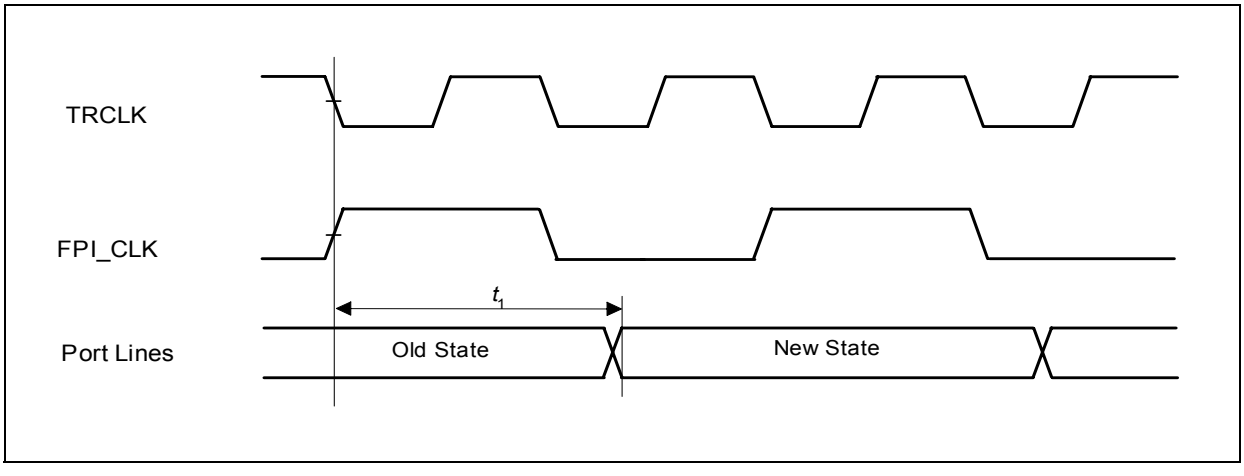


Figure 4-5 Port Timing

4.3.6 Timing for JTAG Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
TCK clock period	t_{TCK}	SR	50	–	ns
TCK high time	t_1	SR	10	–	ns
TCK low time	t_2	SR	29	–	ns
TCK clock rise time	t_3	SR	–	0.4	ns
TCK clock fall time	t_4	SR	–	0.4	ns

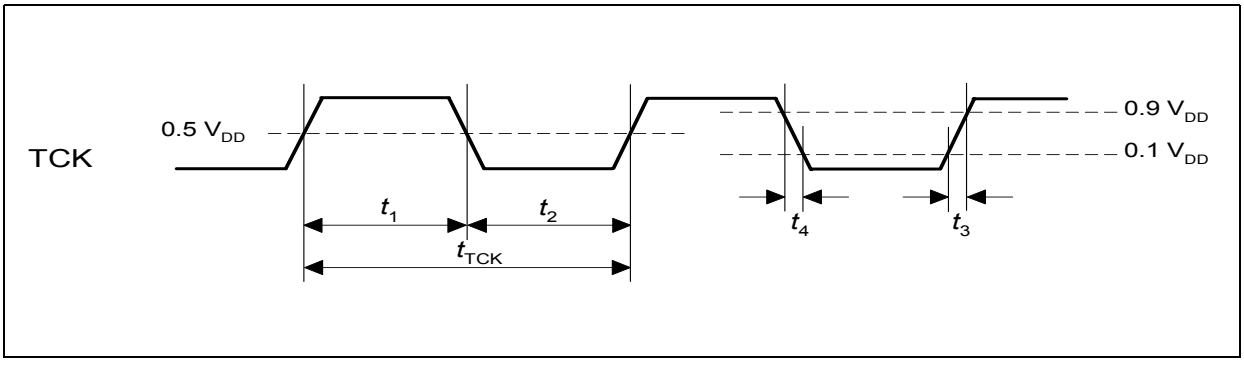
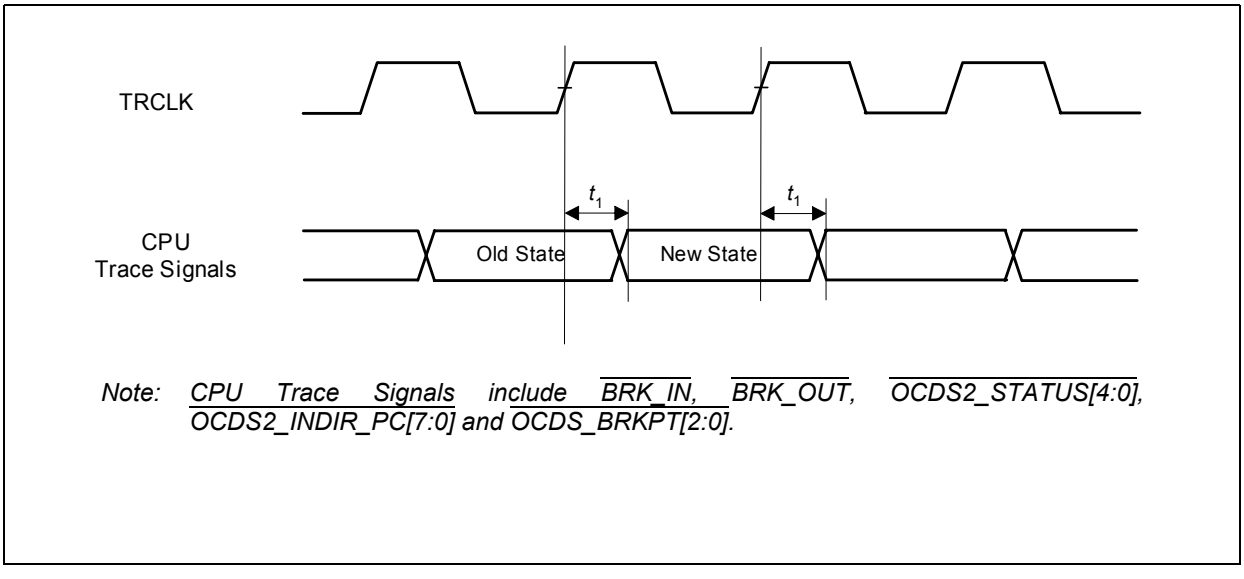


Figure 4-6 TCK Clock Timing

4.3.7 Timing for OCDS Trace and Breakpoint Signals

(Operating Conditions apply; C_L(TRCLK) = 25 pF, C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
$\overline{\text{BRK\_OUT}}$ valid from TRCLK ↓	t_1	CC	–	5.2	ns
$\overline{\text{OCDS2\_STATUS[4:0]}}$ valid from TRCLK ↓	t_1	CC	0	5	ns
$\overline{\text{OCDS2\_INDIR\_PC[7:0]}}$ valid from TRCLK ↓	t_1	CC	0	5	ns
$\overline{\text{OCDS2\_BRKPT[2:0]}}$ valid from TRCLK ↓	t_1	CC	0	5	ns



Note: CPU Trace Signals include $\overline{\text{BRK\_IN}}$, $\overline{\text{BRK\_OUT}}$, $\overline{\text{OCDS2\_STATUS[4:0]}}$, $\overline{\text{OCDS2\_INDIR\_PC[7:0]}}$ and $\overline{\text{OCDS\_BRKPT[2:0]}}$.

Figure 4-8 OCDS Trace Signals Timing

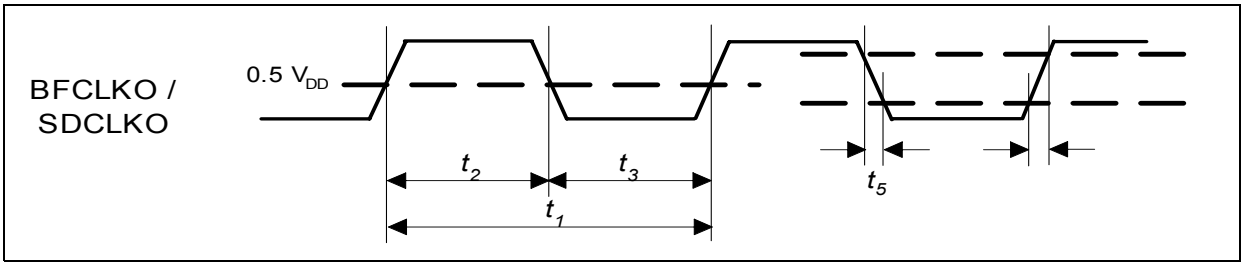


Figure 4-9 EBU Clock Output Timing

4.3.8.3 Timing for SDRAM Access Signals

(Operating Conditions apply; C_L = 50 pF[1])

Parameter	Symbol		Limits[2]		Limits[3]		Unit
			min	max	min	max	
SDCLKO period	t_1	CC	10	–	8.3	–	ns
CKE output valid time from SDCLKO	t_1	CC	–	8.0	–	6.8	ns
CKE output hold time from SDCLKO	t_2	CC	0	–	0.8	–	ns
Address output valid time from SDCLKO	t_3	CC	–	8.0	–	6.8	ns
Address output hold time from SDCLKO	t_4	CC	1.0	–	0.8	–	ns
$\overline{CS}$x, $\overline{RAS}$, $\overline{CAS}$, RD/$\overline{WR}$, $\overline{BC}$(3:0) output valid time from SDCLKO	t_5	CC	–	8.0	–	6.8	ns
$\overline{CS}$x, $\overline{RAS}$, $\overline{CAS}$, RD/$\overline{WR}$, $\overline{BC}$(3:0) output hold time from SDCLKO	t_6	CC	1.0	–	0.8	–	ns
AD(31:0) output valid time from SDCLKO	t_7	CC	–	8.0	–	6.8	ns
AD(31:0) output hold time from SDCLKO	t_8	CC	1.0	–	0.8	–	ns
AD(31:0) input setup time to SDCLKO	t_9	SR	4.0	–	2.9	–	ns
AD(31:0) input hold time from SDCLKO	t_{10}	SR	3.0	–	3.0	–	ns

1) If application conditions other than 50 pf capacitive load are used, then the proper correlation factor should be used for your specific application condition. For design team, the load should be set according to the system requirement.

2) The parameters are applicable for PC100 SDRAM access and the maximum SDCLKO is up to 100 MHz.

3) The parameters are applicable for PC133 SDRAM access and the maximum SDCLKO is up to 120 MHz.

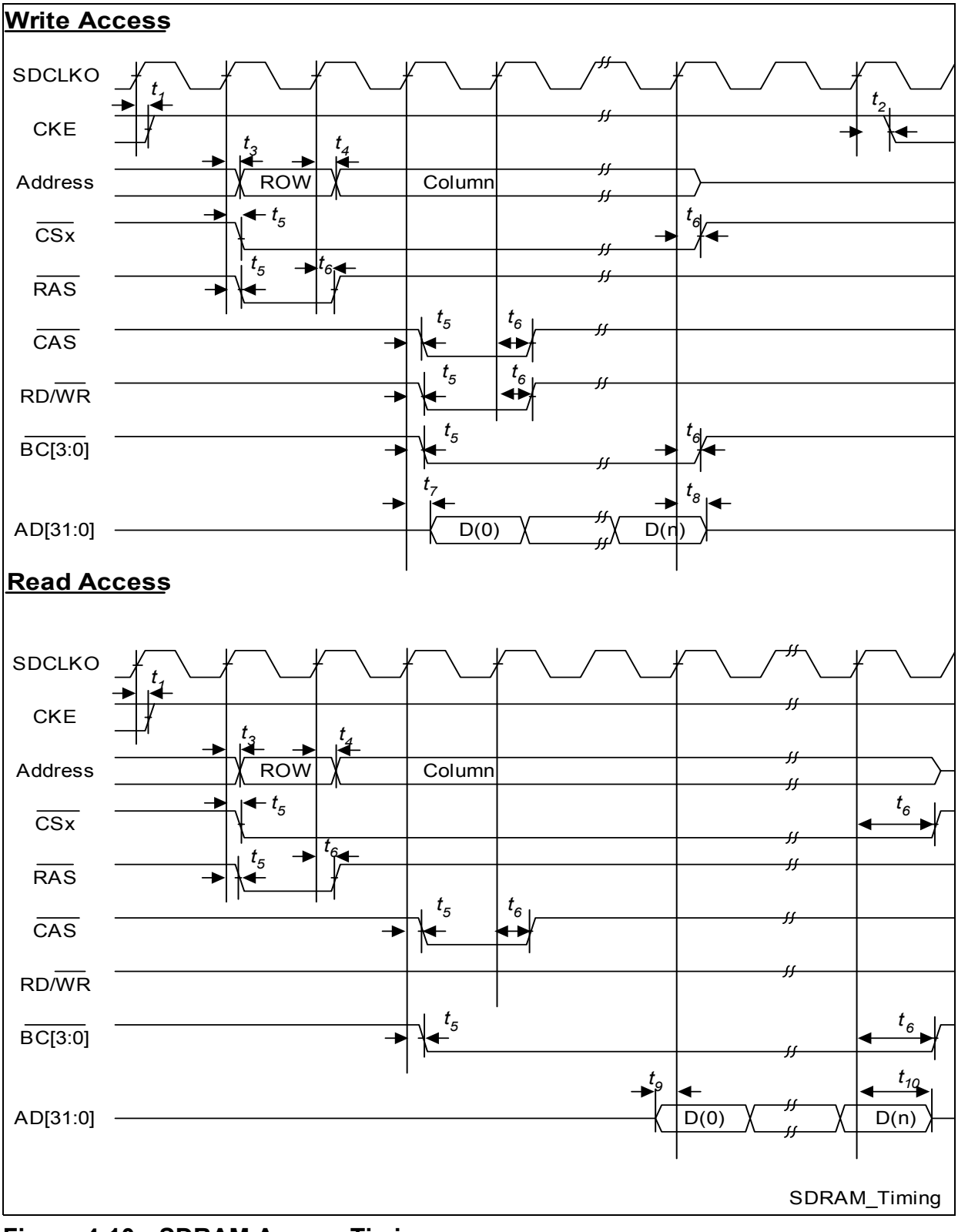


Figure 4-10 SDRAM Access Timing

5 Package Outline

Plastic Package, P-LBGA-208-2 (SMD)
(Low Profile Ball

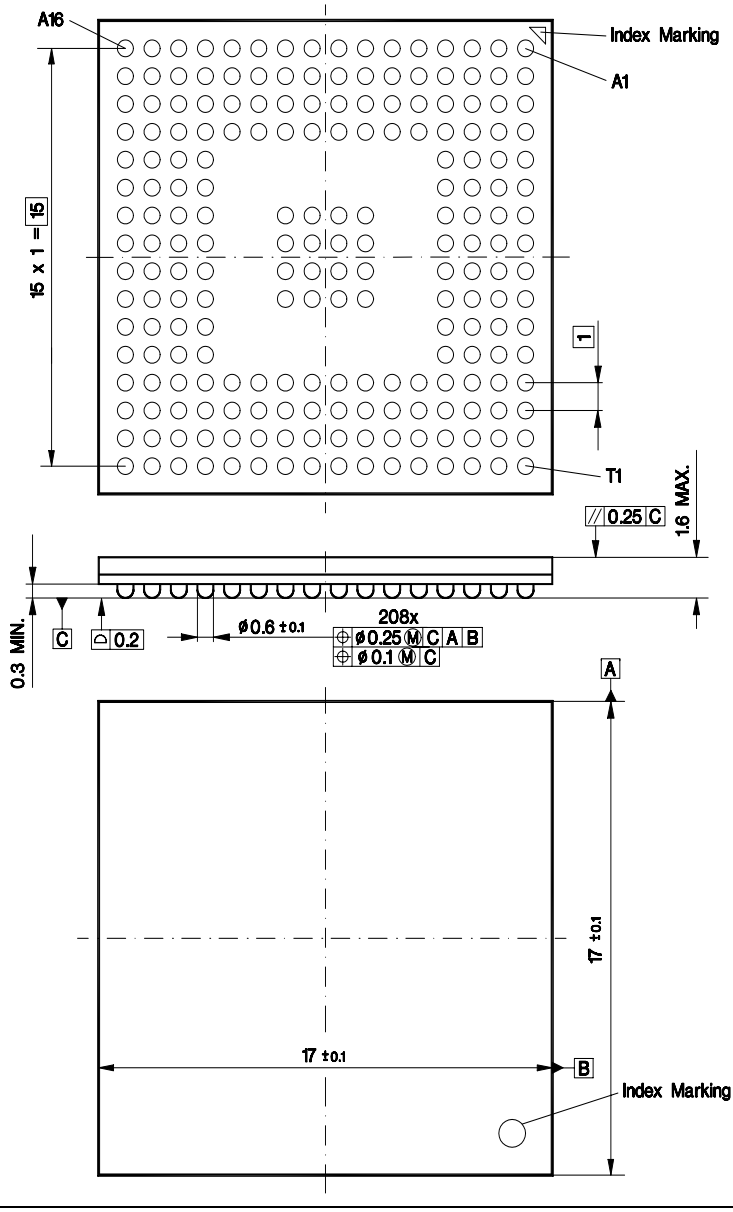


Figure 5-1 P-LBGA-208-2 Package

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm