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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm304t-i-pt

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
U1CTS	I	ST	Yes	UART1 Clear-to-Send.
U1RTS	O	—	Yes	UART1 Ready-to-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
U2CTS	I	ST	Yes	UART2 Clear-to-Send.
U2RTS	O	—	Yes	UART2 Ready-to-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
U3CTS	I	ST	Yes	UART3 Clear-to-Send.
U3RTS	O	—	Yes	UART3 Ready-to-Send.
U3RX	I	ST	Yes	UART3 receive.
U3TX	O	—	Yes	UART3 transmit.
U4CTS	I	ST	Yes	UART4 Clear-to-Send.
U4RTS	O	—	Yes	UART4 Ready-to-Send.
U4RX	I	ST	Yes	UART4 receive.
U4TX	O	—	Yes	UART4 transmit.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCK3	I/O	ST	Yes	Synchronous serial clock input/output for SPI3.
SDI3	I	ST	Yes	SPI3 data in.
SDO3	O	—	Yes	SPI3 data out.
SS3	I/O	ST	Yes	SPI3 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

- Note 1:** This pin is not available on all devices. For more information, see the “Pin Diagrams” section for pin availability.
- 2:** AVDD must be connected at all times.

FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EP512GM3XX/6XX/7XX DEVICES⁽¹⁾

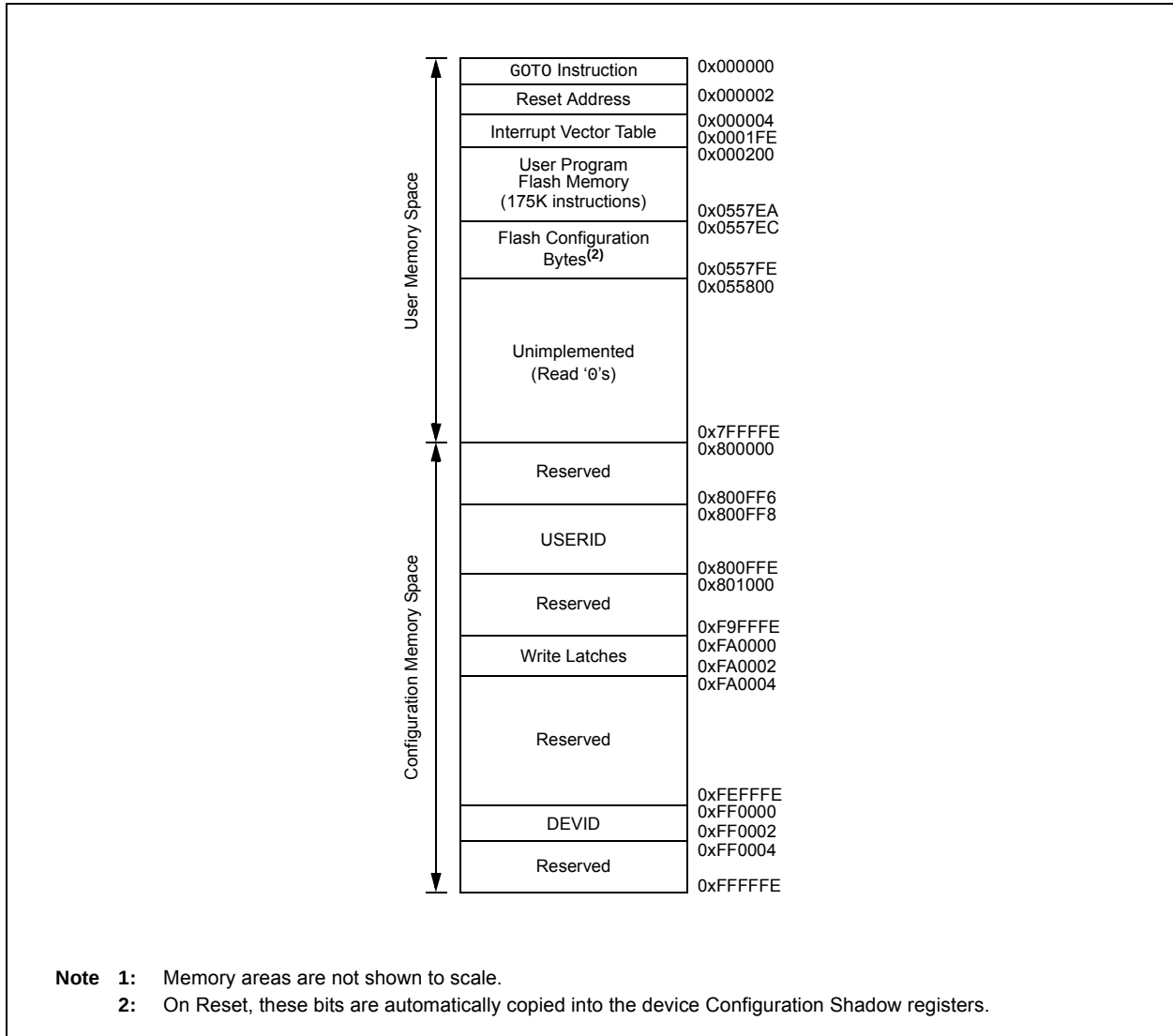


TABLE 4-4: TIMERS REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																0000
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register																0000
TMR3HLD	0108	Timer3 Holding Register (For 32-bit timer operations only)																xxxx
TMR3	010A	Timer3 Register																0000
PR2	010C	Period Register 2																FFFF
PR3	010E	Period Register 3																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR4	0114	Timer4 Register																0000
TMR5HLD	0116	Timer5 Holding Register (For 32-bit timer operations only)																xxxx
TMR5	0118	Timer5 Register																0000
PR4	011A	Period Register 4																FFFF
PR5	011C	Period Register 5																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR6	0122	Timer6 Register																0000
TMR7HLD	0124	Timer7 Holding Register (For 32-bit timer operations only)																xxxx
TMR7	0126	Timer7 Register																0000
PR6	0128	Period Register 6																FFFF
PR7	012A	Period Register 7																FFFF
T6CON	012C	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T7CON	012E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR8	0130	Timer8 Register																0000
TMR9HLD	0132	Timer9 Holding Register (For 32-bit timer operations only)																xxxx
TMR9	0134	Timer9 Register																0000
PR8	0136	Period Register 8																FFFF
PR9	0138	Period Register 9																FFFF
T8CON	013A	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T9CON	013C	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: ADC1 AND ADC2 REGISTER MAP (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
ADC2BUF9	0352	ADC2 Data Buffer 9																	xxxx
ADC2BUFA	0354	ADC2 Data Buffer 10																	xxxx
ADC2BUFB	0356	ADC2 Data Buffer 11																	xxxx
ADC2BUFC	0358	ADC2 Data Buffer 12																	xxxx
ADC2BUFD	035A	ADC2 Data Buffer 13																	xxxx
ADC2BUFE	035C	ADC2 Data Buffer 14																	xxxx
ADC2BUFF	035E	ADC2 Data Buffer 15																	xxxx
AD2CON1	0360	ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0	SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE	0000	
AD2CON2	0362	VCFG2	VCFG1	VCFG0	OFFCAL	—	CSCNA	CHPS1	CHPS0	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000	
AD2CON3	0364	ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000	
AD2CHS123	0366	—	—	—	CH123SB2	CH123SB1	CH123NB1	CH123NB0	CH123SB0	—	—	—	CH123SA2	CH123SA1	CH123NA1	CH123NA0	CH123SA0	0000	
AD2CHS0	0368	CH0NB	—	CH0SB5 ⁽¹⁾	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA	—	CH0SA5 ⁽¹⁾	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000	
AD2CSSH	036E	CSS<31:16>																	0000
AD2CSSL	0370	CSS<15:0>																	0000
AD2CON4	0372	—	—	—	—	—	—	—	ADDMAEN	—	—	—	—	—	DMABL2	DMABL1	DMABL0	0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Bits 13 and bit 5 are reserved in the AD2CHS0 register, unlike the AD1CHS0 register.

TABLE 4-34: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGM3XX DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		
RPINR0	06A0	—	INT1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>								0000	
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>								0000	
RPINR7	06AE	—	IC2R<6:0>								—	IC1R<6:0>								0000
RPINR8	06B0	—	IC4R<6:0>								—	IC3R<6:0>								0000
RPINR9	06B2	—	IC6R<6:0>								—	IC5R<6:0>								0000
RPINR10	06B4	—	IC8R<6:0>								—	IC7R<6:0>								0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>								0000	
RPINR12	06B8	—	FLT2R<6:0>								—	FLT1R<6:0>								0000
RPINR14	06BC	—	QEB1R<6:0>								—	QEA1R<6:0>								0000
RPINR15	06BE	—	HOME1R<6:0>								—	INDX1R<6:0>								0000
RPINR16	06C0	—	QEB2R<6:0>								—	QEA2R<6:0>								0000
RPINR17	06C2	—	HOME2R<6:0>								—	INDX2R<6:0>								0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>								0000	
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>								0000	
RPINR22	06CC	—	SCK2R<6:0>								—	SDI2R<6:0>								0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>								0000	
RPINR24	06D0	—	CSCKR<6:0>								—	CSDIR<6:0>								0000
RPINR25	06D2	—	—	—	—	—	—	—	—	—	COFSR<6:0>								0000	
RPINR27	06D6	—	U3CTSR<6:0>								—	U3RXR<6:0>								0000
RPINR28	06D8	—	U4CTSR<6:0>								—	U4RXR<6:0>								0000
RPINR29	06DA	—	SCK3R<6:0>								—	SDI3R<6:0>								0000
RPINR30	06DC	—	—	—	—	—	—	—	—	—	SS3R<6:0>								0000	
RPINR37	06EA	—	SYNCI1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR38	06EC	—	DTCMP1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR39	06EE	—	DTCMP3R<6:0>								—	DTCMP2R<6:0>								0000
RPINR40	06F0	—	DTCMP5R<6:0>								—	DTCMP4R<6:0>								0000
RPINR41	06F2	—	—	—	—	—	—	—	—	—	DTCMP6R<6:0>								0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGM3XX/6XX/7XX

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB<15:0>																DF9F
PORTB	0E12	RB<15:0>																xxxx
LATB	0E14	LATB<15:0>																xxxx
ODCB	0E16	ODCB<15:0>																0000
CNENB	0E18	CNIEB<15:0>																0000
CNPUB	0E1A	CNPUB<15:0>																0000
CNPDB	0E1C	CNPDB<15:0>																0000
ANSELB	0E1E	—	—	—	—	—	—	ANSB<9:7>			—	—	—	ANSB<3:0>				010F

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-51: PORTB REGISTER MAP FOR dsPIC33EPXXXGM304/604 DEVICES

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
OC5 – Output Compare 5	49	41	0x000066	IFS2<9>	IEC2<9>	IPC10<6:4>
OC6 – Output Compare 6	50	42	0x000068	IFS2<10>	IEC2<10>	IPC10<10:8>
OC7 – Output Compare 7	51	43	0x00006A	IFS2<11>	IEC2<11>	IPC10<14:12>
OC8 – Output Compare 8	52	44	0x00006C	IFS2<12>	IEC2<12>	IPC11<2:0>
PMP – Parallel Master Port ⁽²⁾	53	45	0x00006E	IFS2<13>	IEC2<13>	IPC11<6:4>
Reserved	54	46	0x000070	—	—	—
T6 – Timer6	55	47	0x000072	IFS2<15>	IEC2<15>	IPC11<14:12>
T7 – Timer7	56	48	0x000074	IFS3<0>	IEC3<0>	IPC12<2:0>
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>
T8 – Timer8	59	51	0x00007A	IFS3<3>	IEC3<3>	IPC12<14:12>
T9 – Timer9	60	52	0x00007C	IFS3<4>	IEC3<4>	IPC13<2:0>
INT3 – External Interrupt 3	61	53	0x00007E	IFS3<5>	IEC3<5>	IPC13<6:4>
INT4 – External Interrupt 4	62	54	0x000080	IFS3<6>	IEC3<6>	IPC13<10:8>
C2RX – CAN2 RX Data Ready ⁽¹⁾	63	55	0x000082	IFS3<7>	IEC3<7>	IPC13<14:12>
C2 – CAN2 Event ⁽¹⁾	64	56	0x000084	IFS3<8>	IEC3<8>	IPC14<2:0>
PSEM – PCPWM Primary Event	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>
QE11 – QE11 Position Counter Compare	66	58	0x000088	IFS3<10>	IEC3<10>	IPC14<10:8>
DCIE – DCI Fault Interrupt	67	59	0x00008A	IFS3<11>	IEC3<11>	IPC14<14:12>
DCI – DCI Transfer Done	68	60	0x00008C	IFS3<12>	IEC3<12>	IPC15<2:0>
Reserved	69	61	0x00008E	—	—	—
RTCC – Real-Time Clock and Calendar ⁽²⁾	70	62	0x000090	IFS3<14>	IEC3<14>	IPC15<10:8>
Reserved	71-72	63-64	0x000092-0x000094	—	—	—
U1E – UART1 Error Interrupt	73	65	0x000096	IFS4<1>	IEC4<1>	IPC16<6:4>
U2E – UART2 Error Interrupt	74	66	0x000098	IFS4<2>	IEC4<2>	IPC16<10:8>
CRC – CRC Generator Interrupt	75	67	0x00009A	IFS4<3>	IEC4<3>	IPC16<14:12>
Reserved	76-77	68-69	0x00009C-0x00009E	—	—	—
C1TX – CAN1 TX Data Request ⁽¹⁾	78	70	0x0000A0	IFS4<6>	IEC4<6>	IPC17<10:8>
C2TX – CAN2 TX Data Request ⁽¹⁾	79	71	0x0000A2	IFS4<7>	IEC4<7>	IPC17<14:12>
Reserved	80	72	0x0000A4	—	—	—
PSESM – PCPWM Secondary Event	81	73	0x0000A6	IFS4<9>	IEC4<9>	IPC18<6:4>
Reserved	82	74	0x0000A8	—	—	—
QE12 – QE12 Position Counter Compare	83	75	0x0000AA	IFS4<11>	IEC4<11>	IPC18<14:12>
Reserved	84	76	0x0000AC	—	—	—
CTMU – CTMU Interrupt	85	77	0x0000AE	IFS4<13>	IEC4<13>	IPC19<6:4>
Reserved	86-88	78-80	0x0000B0-0x0000B4	—	—	—
U3E – UART3 Error Interrupt	89	81	0x0000B6	IFS5<1>	IEC5<1>	IPC20<6:4>
U3RX – UART3 Receiver	90	82	0x0000B8	IFS5<2>	IEC5<2>	IPC20<10:8>
U3TX – UART3 Transmitter	91	83	0x0000BA	IFS5<3>	IEC5<3>	IPC20<14:12>
Reserved	92-94	84-86	0x0000BC-0x0000C0	—	—	—
U4E – UART4 Error Interrupt	95	87	0x0000C2	IFS5<7>	IEC5<7>	IPC21<14:12>
U4RX – UART4 Receiver	96	88	0x0000C4	IFS5<8>	IEC5<8>	IPC22<2:0>
U4TX – UART4 Transmitter	97	89	0x0000C6	IFS5<9>	IEC5<9>	IPC22<6:4>

Note 1: This interrupt source is available on dsPIC33EPXXXGM6XX/7XX devices only.

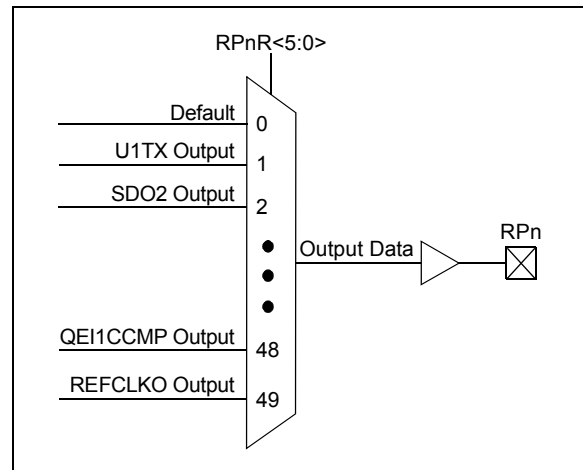
Note 2: This interrupt source is not available on 44-pin devices.

11.4.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 11-30 through Register 11-42). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUT FOR RPn



11.4.5.1 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 11-29: RPINR41: PERIPHERAL PIN SELECT INPUT REGISTER 41

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	DTCMP6R<6:0>							
bit 7								bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7

Unimplemented: Read as '0'

bit 6-0

DTCMP6R<6:0>: Assign PWM Dead-Time Compensation Input 6 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•
•
•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 17-6: POSxHLD: POSITION COUNTER x HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **POSHLD<15:0>**: Holding Register for Reading and Writing POSxCNT bits

REGISTER 17-7: VELxCNT: VELOCITY COUNTER x REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VELCNT<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VELCNT<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **VELCNT<15:0>**: Velocity Counter x bits

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 17-19: INTxHLDH: INTERVAL TIMERx HOLD HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INTHLD<31:16>**: Holding Register for Reading and Writing INTxTMRH bits

REGISTER 17-20: INTxHLDL: INTERVAL TIMERx HOLD LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTHLD<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **INTHLD<15:0>**: Holding Register for Reading and Writing INTxTMRL bits

REGISTER 21-10: CxCFG2: CANx BAUD RATE CONFIGURATION REGISTER 2

U-0	R/W-x	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	WAKFIL	—	—	—	SEG2PH2	SEG2PH1	SEG2PH0
bit 15						bit 8	

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG1	PRSEG0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **WAKFIL:** Select CAN Bus Line Filter for Wake-up bit

1 = Uses CAN bus line filter for wake-up

0 = CAN bus line filter is not used for wake-up

bit 13-11 **Unimplemented:** Read as '0'

bit 10-8 **SEG2PH<2:0>:** Phase Segment 2 bits

111 = Length is 8 x T_Q

.

.

.

000 = Length is 1 x T_Q

bit 7 **SEG2PHTS:** Phase Segment 2 Time Select bit

1 = Freely programmable

0 = Maximum of SEG1PHx bits or Information Processing Time (IPT), whichever is greater

bit 6 **SAM:** Sample of the CAN Bus Line bit

1 = Bus line is sampled three times at the sample point

0 = Bus line is sampled once at the sample point

bit 5-3 **SEG1PH<2:0>:** Phase Segment 1 bits

111 = Length is 8 x T_Q

.

.

.

000 = Length is 1 x T_Q

bit 2-0 **PRSEG<2:0>:** Propagation Time Segment bits

111 = Length is 8 x T_Q

.

.

.

000 = Length is 1 x T_Q

21.4 CAN Message Buffers

CAN Message Buffers are part of RAM memory. They are not CAN Special Function Registers. The user application must directly write into the RAM area that is configured for CAN Message Buffers. The location and size of the buffer area is defined by the user application.

BUFFER 21-1: CANx MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'
 bit 12-2 **SID<10:0>:** Standard Identifier bits
 bit 1 **SRR:** Substitute Remote Request bit
 When IDE = 0:
 1 = Message will request remote transmission
 0 = Normal message
 When IDE = 1:
 The SRR bit must be set to '1'.
 bit 0 **IDE:** Extended Identifier bit
 1 = Message will transmit an Extended Identifier
 0 = Message will transmit a Standard Identifier

BUFFER 21-2: CANx MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	EID<17:14>			
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<13:6>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'
 bit 11-0 **EID<17:6>:** Extended Identifier bits

REGISTER 26-8: CVR2CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	—	—	CVRR1	VREFSEL	—	—
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE	CVRR0	CVRSS	CVR3	CVR2	CVR1	CVR0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-12 **Unimplemented:** Read as '0'
- bit 11 **CVRR1:** Comparator Voltage Reference Range Selection bit
See bit 5.
- bit 10 **VREFSEL:** Voltage Reference Select bit
1 = Reference source for inverting input is from CVR2
0 = Reference source for inverting input is from CVR1
- bit 9-8 **Unimplemented:** Read as '0'
- bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down
- bit 6 **CVROE:** Comparator Voltage Reference Output Enable on CVREF2O Pin bit
1 = Voltage level is output on the CVREF2O pin
0 = Voltage level is disconnected from the CVREF2O pin
- bit 11, 5 **CVRR<1:0>:** Comparator Voltage Reference Range Selection bits
11 = 0.00 CVRSRC to 0.94, with CVRSRC/16 step-size
10 = 0.33 CVRSRC to 0.96, with CVRSRC/24 step-size
01 = 0.00 CVRSRC to 0.67, with CVRSRC/24 step-size
00 = 0.25 CVRSRC to 0.75, with CVRSRC/32 step-size
- bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator voltage reference source, CVRSRC = CVREF+ – AVSS
0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS
- bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection $0 \leq \text{CVR<3:0>} \leq 15$ bits
 When CVRR<1:0> = 11:
 $\text{CVREF} = (\text{CVR<3:0>/16}) \bullet (\text{CVRSRC})$
 When CVRR<1:0> = 10:
 $\text{CVREF} = (1/3) \bullet (\text{CVRSRC}) + (\text{CVR<3:0>/24}) \bullet (\text{CVRSRC})$
 When CVRR<1:0> = 01:
 $\text{CVREF} = (\text{CVR<3:0>/24}) \bullet (\text{CVRSRC})$
 When CVRR<1:0> = 00:
 $\text{CVREF} = (1/4) \bullet (\text{CVRSRC}) + (\text{CVR<3:0>/32}) \bullet (\text{CVRSRC})$

NOTES:

29.2 Programmable CRC Control Registers

REGISTER 29-1: CRCCON1: CRC CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0
CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0
bit 15							bit 8

R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CRCEN:** CRC Enable bit
 1 = CRC module is enabled
 0 = CRC module is disabled; all state machines, pointers and CRCWDAT/CRCDAT are reset, other SFRs are not reset
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **CSIDL:** CRC Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-8 **VWORD<4:0>:** Valid Word Pointer Value bits
 Indicates the number of valid words in the FIFO; has a maximum value of 8 when PLEN<4:0> > 7 or 16 when PLEN<4:0> ≤ 7
- bit 7 **CRCFUL:** CRC FIFO Full bit
 1 = FIFO is full
 0 = FIFO is not full
- bit 6 **CRCMPT:** CRC FIFO Empty Bit
 1 = FIFO is empty
 0 = FIFO is not empty
- bit 5 **CRCISEL:** CRC Interrupt Selection bit
 1 = Interrupt on FIFO empty; final word of data is still shifting through CRC
 0 = Interrupt on shift complete and CRCWDAT results are ready
- bit 4 **CRCGO:** CRC Start bit
 1 = Start CRC serial shifter
 0 = CRC serial shifter is turned off
- bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit
 1 = Data word is shifted into the CRC starting with the LSb (little endian)
 0 = Data word is shifted into the CRC starting with the MSb (big endian)
- bit 2-0 **Unimplemented:** Read as '0'

FIGURE 33-13: QEAX/QEBx INPUT CHARACTERISTICS

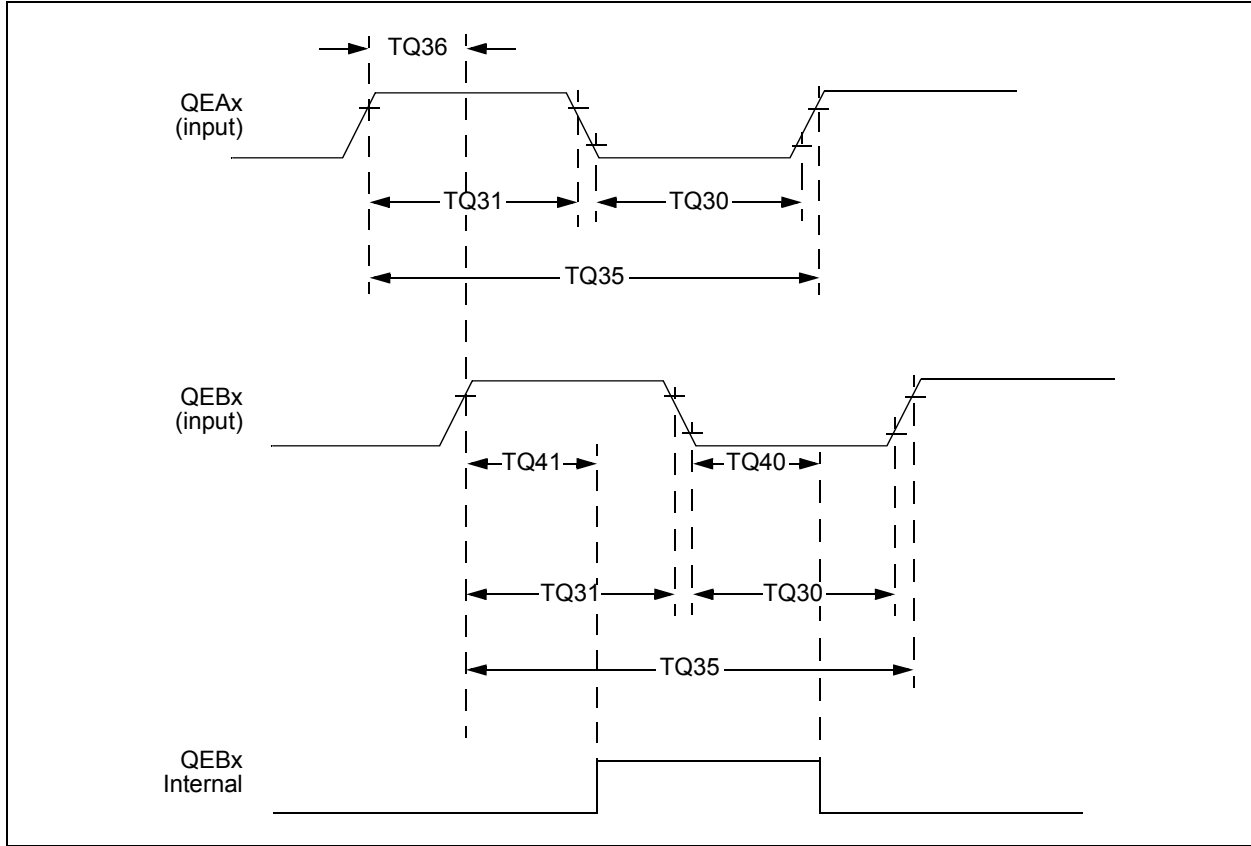


TABLE 33-30: QUADRATURE DECODER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param No.	Symbol	Characteristic ⁽¹⁾	Typ. ⁽²⁾	Max.	Units	Conditions
TQ30	TQuL	Quadrature Input Low Time	6 Tcy	—	ns	
TQ31	TQuH	Quadrature Input High Time	6 Tcy	—	ns	
TQ35	TQuIN	Quadrature Input Period	12 Tcy	—	ns	
TQ36	TQuP	Quadrature Phase Period	3 Tcy	—	ns	
TQ40	TQuFL	Filter Time to Recognize Low with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)
TQ41	TQuFH	Filter Time to Recognize High with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: N = Index Channel Digital Filter Clock Divide Select bits. Refer to the "dsPIC33/PIC24 Family Reference Manual", "Quadrature Encoder Interface (QE)" (DS70601). Please see the Microchip web site for the latest "dsPIC33/PIC24 Family Reference Manual" sections.

TABLE 33-61: DMA MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DM1	DMA Byte/Word Transfer Latency	1 TCY ⁽²⁾	—	—	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.

TABLE 34-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
HDO10	VOL	Output Low Voltage 4x Sink Driver Pins ⁽²⁾	—	—	0.4	V	$I_{OL} \leq 5\text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
		Output Low Voltage 8x Sink Driver Pins ⁽³⁾	—	—	0.4	V	$I_{OL} \leq 8\text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
HDO20	VOH	Output High Voltage 4x Source Driver Pins ⁽²⁾	2.4	—	—	V	$I_{OH} \geq -10\text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
		Output High Voltage 8x Source Driver Pins ⁽³⁾	2.4	—	—	V	$I_{OH} \geq 15\text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
HDO20A	VOH1	Output High Voltage 4x Source Driver Pins ⁽²⁾	1.5	—	—	V	$I_{OH} \geq -3.9\text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			2.0	—	—		$I_{OH} \geq -3.7\text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			3.0	—	—		$I_{OH} \geq -2\text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
		Output High Voltage 8x Source Driver Pins ⁽³⁾	1.5	—	—	V	$I_{OH} \geq -7.5\text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			2.0	—	—		$I_{OH} \geq -6.8\text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)
			3.0	—	—		$I_{OH} \geq -3\text{ mA}$, $V_{DD} = 3.3\text{V}$ (Note 1)

Note 1: Parameters are characterized, but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

3: Includes the following pins:

For 44-pin devices: RA3, RA4, RA7, RA9, RA10, RB7, RB<15:9>, RC1 and RC<9:3>

For 64-pin devices: RA4, RA7, RA<10:9>, RB7, RB<15:9>, RC1, RC<9:3>, RC15 and RG<8:7>

For 100-pin devices: RA4, RA7, RA9, RA10, RB7, RB<15:9>, RC1, RC<9:3>, RC15, RD<3:1> and RG<8:6>

TABLE 34-9: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
HD130	EP	Program Flash Memory Cell Endurance	10,000	—	—	E/W	-40°C to $+150^{\circ}\text{C}$ ⁽²⁾ 1000 E/W cycles or less and no other specifications are violated
HD134	TRETD	Characteristic Retention	20	—	—	Year	

Note 1: These parameters are assured by design, but are not characterized or tested in manufacturing.

2: Programming of the Flash memory is allowed up to $+150^{\circ}\text{C}$.

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