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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 30x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm306-e-pt

Email: info@E-XFL.COM

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# 3.0 CPU

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33/PIC24 Family Reference Manual", "CPU" (DS70359), which is available from the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word, with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle, effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

### 3.1 Registers

The dsPIC33EPXXXGM3XX/6XX/7XX devices have sixteen 16-bit Working registers in the programmer's model. Each of the Working registers can act as a data, address or address offset register. The 16th Working register (W15) operates as a Software Stack Pointer for interrupts and calls.

### 3.2 Instruction Set

The device instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

# 3.3 Data Space Addressing

The Base Data Space can be addressed as 4K words or 8 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operate solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EP devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Space boundary is device-specific.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space at any 16K program word boundary. The program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Data Space Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to "Data Memory" (DS70595) and "Program Memory" (DS70613) in the "dsPIC33/ PIC24 Family Reference Manual" for more details on EDS, PSV and table accesses.

On dsPIC33EP devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

# 3.4 Addressing Modes

The CPU supports these addressing modes:

- · Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

# dsPIC33EPXXXGM3XX/6XX/7XX

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	_	US1	US0	EDT <sup>(1)</sup>	DL2	DL1	DL0
bit 15					·	·	bit 8
R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3 <sup>(2)</sup>	SFA	RND	IF
bit 7							bit 0
Legend:		C = Clearable	e bit				
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15	VAR: Variable 1 = Variable e 0 = Fixed exc	e Exception Pro exception proce eption process	ocessing Later essing latency sing latency is	ncy Control bit is enabled enabled			
bit 13_12		P Multiply Lips	u ianed/Signed	Control bite			
bit 11	<ul> <li>11 = Reserved</li> <li>10 = DSP engine multiplies are mixed-sign</li> <li>01 = DSP engine multiplies are unsigned</li> <li>00 = DSP engine multiplies are signed</li> <li>EDT: Early DO Loop Termination Control bit<sup>(1)</sup></li> <li>1 = Terminates executing DO loop at end of current loop iteration</li> </ul>						
bit 10-8	DL<2:0>: DO 111 = 7 DO IO	Loop Nesting I ops are active op is active ops are active	∟evel Status b	its			
bit 7	SATA: ACCA 1 = Accumula 0 = Accumula	Saturation En Itor A saturatio Itor A saturatio	able bit n is enabled n is disabled				
bit 6	SATB: ACCB 1 = Accumula 0 = Accumula	Saturation En itor B saturatio itor B saturatio	able bit n is enabled n is disabled				
bit 5	SATDW: Data 1 = Data Spac 0 = Data Spac	a Space Write f ce write satura ce write satura	from DSP Eng tion is enabled tion is disable	iine Saturation ว d	Enable bit		
bit 4	ACCSAT: Acc 1 = 9.31 satur 0 = 1.31 satur	cumulator Satu ration (super sa ration (normal	ration Mode S aturation) saturation)	Select bit			
Note 1: Thi	s bit is always r	ead as '0'.					

# REGISTER 3-2: CORCON: CORE CONTROL REGISTER<sup>(3)</sup>

2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

3: Refer to the "dsPIC33/PIC24 Family Reference Manual", "CPU" (DS70359) for more detailed information.

# 4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/ 7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33/PIC24 Family Reference Manual", "Program Memory" (DS70613), which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXXGM3XX/6XX/7XX family architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

#### 4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGM3XX/6XX/7XX devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in Section 4.7 "Interfacing Program and Data Memory Spaces".

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-3.



# FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP128GM3XX/6XX/7XX DEVICES<sup>(1)</sup>

# 4.5 Modulo Addressing

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a Bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

#### 4.5.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y space Modulo Addressing EA calcula-
	tions assume word-sized data (LSb of
	every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

#### 4.5.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register bits, MODCON<15:0>, contain enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM) to which Modulo Addressing is to be applied is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit is set (MODCON<15>).

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit is set (MODCON<14>).

#### FIGURE 4-14: MODULO ADDRESSING OPERATION EXAMPLE



REGISTER 11-9:	<b>RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12</b>

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
_				FLT2R<6:0>						
bit 15							bit 8			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
_				FLT1R<6:0>						
bit 7							bit 0			
Legend:										
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'				
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkı	nown			
bit 15	Unimplemer	ted: Read as '	0'							
bit 14-8	FLT2R<6:0> (see Table 11	: Assign PWM I -2 for input pin	Fault 2 (FLT2 selection nur	) to the Corresp nbers)	onding RPn F	Pin bits				
	1111100 <b>=  </b>	1111100 = Input tied to RPI124								
	•									
	•									
	• 000001 = 1	nout tied to CM	P1							
	0000000 = 1	nput tied to Vss	;							
bit 7	Unimplemer	ted: Read as '	0'							
bit 6-0	FLT1R<6:0>	: Assign PWM I	Fault 1 (FLT1	) to the Corresp	onding RPn F	Pin bits				
	(see Table 11-2 for input pin selection numbers)									
	1111100 <b>=  </b>	nput tied to RPI	124							
	•									
	•									
	•	oput tied to CM	P1							
	0000000 = 1	nput tied to Vss	;							

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	—		—	—	—	—
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				COFSR<6:02	>		
bit 7							bit 0
Legend:							
R = Readable b	oit	W = Writable	bit	U = Unimplemented bit, read as '0'			
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			

# REGISTER 11-19: RPINR25: PERIPHERAL PIN SELECT INPUT REGISTER 25

#### bit 15-7 Unimplemented: Read as '0'

bit 6-0 **COFSR<6:0>:** Assign DCI Frame Sync Input (COFS) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers) 1111100 = Input tied to RPI124

•

0000001 = Input tied to CMP1 0000000 = Input tied to Vss

# REGISTER 11-38: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8<sup>(1)</sup>

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—			RP70	R<5:0>		
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	_			RP69	R<5:0>		

bit 7	
-------	--

bit 7

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	<b>RP70R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP70 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	<b>RP69R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP69 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is not available on dsPIC33EPXXXGM304/604 devices.

# REGISTER 11-39: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9<sup>(1)</sup>

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—			RP97	R<5:0>		
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				RP81F	<sub>2&lt;5</sub> .0>(2)		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	<b>RP97R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	<b>RP81R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP81 Output Pin bits <sup>(2)</sup> (see Table 11-3 for peripheral function numbers)
Note 1:	This register is not available on dsPIC33EPXXXGM304/604 devices.

2: These bits are not available on dsPIC33EPXXXGM306/706 devices.

bit 0

bit 0

REGISTER 11-42: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12	REGISTER 11-42:	<b>RPOR12: PERIPHERAL</b>	PIN SELECT	<b>OUTPUT REGISTE</b>	ER 12 <sup>(1)</sup>
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U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
_	—		RP127R<5:0>					
bit 15							bit 8	
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—		RP126R<5:0>					
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit		bit	U = Unimplemented bit, read as '0'					
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown	
bit 15-14	Unimpleme	nted: Read as '	0'					
bit 13-8	RP127R<5:	0>: Peripheral C	Output Functio	on is Assigned to	o RP127 Outp	ut Pin bits		
	(see Table 11-3 for peripheral function numbers)							
bit 7-6	Unimpleme	nted: Read as '	0'					
bit 5-0	5-0 <b>RP126R&lt;5:0&gt;:</b> Peripheral Output Function is Assigned to RP126 Output Pin bits (see Table 11-3 for peripheral function numbers)							

Note 1: This register is not available on dsPIC33EPXXXGM30X/604/706 devices.

# REGISTER 16-7: STPER: PWMx SECONDARY MASTER TIME BASE PERIOD REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
			STPE	R<15:8>			
bit 15							bit 8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
			STPE	R<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cle	ared	x = Bit is unkr	nown	

bit 15-0 STPER<15:0>: PWMx Secondary Master Time Base (PMTMR) Period Value bits

#### REGISTER 16-8: SSEVTCMP: PWMx SECONDARY SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SSEVTC	CMP<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SSEVT	CMP<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		it	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cle	ared	x = Bit is unkr	nown	

bit 15-0 SSEVTCMP<15:0>: PWMx Secondary Special Event Compare Count Value bits

# 17.1 QEI Control Registers

#### REGISTER 17-1: QEIxCON: QEIx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIEN	—	QEISIDL	PIMOD2 <sup>(1)</sup>	PIMOD1 <sup>(1)</sup>	PIMOD0 <sup>(1)</sup>	IMV1 <sup>(2,4)</sup>	IMV0 <sup>(2,4)</sup>
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INTDIV2 <sup>(3)</sup>	INTDIV1 <sup>(3)</sup>	INTDIV0 <sup>(3)</sup>	CNTPOL	GATEN	CCM1	CCM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	<b>QEIEN:</b> QEIx Module Counter Enable bit
	1 = Module counters are enabled
	0 = Module counters are disabled, but SFRs can be read or written to
bit 14	Unimplemented: Read as '0'
bit 13	QEISIDL: QEIx Stop in Idle Mode bit
	<ul> <li>1 = Discontinues module operation when device enters Idle mode</li> <li>0 = Continues module operation in Idle mode</li> </ul>
bit 12-10	PIMOD<2:0>: Position Counter Initialization Mode Select bits <sup>(1)</sup>
	111 = Reserved
	110 = Modulo Count mode for position counter
	101 = Resets the position counter when the position counter equals the QEIxGEC register
	100 = Second index event after home event initializes the position counter with contents of the QEIxIC register
	011 = First index event after home event initializes the position counter with contents of the QEIxIC register
	010 = Next index input event initializes the position counter with contents of the QEIxIC register
	001 = Every index input event resets the position counter
	000 = Index input event does not affect position counter
bit 9-8	IMV<1:0>: Index Match Value bits <sup>(2,4)</sup>
	<ul> <li>1 = Required state of Phase B input signal for match on index pulse</li> <li>0 = Required state of Phase A input signal for match on index pulse</li> </ul>
bit 7	Unimplemented: Read as '0'
Note 1:	when $CGM<1:0> = 10$ or $CGM<1:0> = 11$ , all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

- 2: When CCM<1:0> = 00, and QEAx and QEBx values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset.
- 3: The selected clock rate should be at least twice the expected maximum quadrature count rate.
- 4: The match value applies to the A and B inputs after the swap and polarity bits have been applied.

# **REGISTER 17-6: POSxHLD: POSITION COUNTER x HOLD REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			POSHI	_D<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			POSH	LD<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cle	ared	x = Bit is unkr	nown	

bit 15-0 **POSHLD<15:0>:** Holding Register for Reading and Writing POSxCNT bits

## REGISTER 17-7: VELxCNT: VELOCITY COUNTER x REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			VELC	NT<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			VELC	NT<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		it	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cle	ared	x = Bit is unkr	nown	

bit 15-0 VELCNT<15:0>: Velocity Counter x bits

REGISTER 20-2:	UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN <sup>(1)</sup>	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7			•				bit 0

Legend: C = Clearable bit		HC = Hardware Clearable bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: UARTx Transmit Polarity Inversion bit

lf	IREN = 0:	
1	= UxTX Idle state is '(	0'

0 = UxTX Idle state is '1'

- If IREN = 1:

   1 = IrDA encoded UxTX Idle state is '1'

   0 = IrDA encoded UxTX Idle state is '0'

   bit 12
   Unimplemented: Read as '0'

   bit 11
   UTXBRK: UARTx Transmit Break bit

   1 = Sends Sync Break on next transmission Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion

   0 = Sync Break transmission is disabled or has completed

   bit 10
   UTXEN: UARTx Transmit Enable bit<sup>(1)</sup>

   1 = Transmit is enabled, UxTX pin is controlled by UARTx

   0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset: UxTX pin is
  - 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by the PORT
- bit 9 UTXBF: UARTx Transmit Buffer Full Status bit (read-only)
  - 1 = Transmit buffer is full
  - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
  - 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
  - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
  - 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
  - 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
  - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters
- Note 1: Refer to the "dsPIC33/PIC24 Family Reference Manual", "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582) for information on enabling the UART module for transmit operation.

## 21.4 CAN Message Buffers

CAN Message Buffers are part of RAM memory. They are not CAN Special Function Registers. The user application must directly write into the RAM area that is configured for CAN Message Buffers. The location and size of the buffer area is defined by the user application.

## BUFFER 21-1: CANx MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	_	_	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE
bit 7							bit 0
-							
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimplei	mented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15-13	Unimplemen	ted: Read as '	0'				
bit 12-2	SID<10:0>: S	Standard Identif	ier bits				
bit 1	SRR: Substitut	ute Remote Re	quest bit				
	When IDE =	0:					
	1 = Message	will request rer	note transmis	ssion			
	0 = Normal m	nessage					
	When IDE = 2	1:					
	The SRR bit I	must be set to '	1'.				
bit 0	IDE: Extende	d Identifier bit					
	1 = Message 0 = Message	will transmit ar will transmit a	n Extended Id Standard Ider	entifier ntifier			

#### BUFFER 21-2: CANx MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
_	—	—	_		EID<	17:14>	
bit 15							bit 8
r							
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID<	:13:6>			
bit 7							bit 0
Legend:							
R = Readable	R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'						
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			

bit 15-12 Unimplemented: Read as '0'

bit 11-0 EID<17:6>: Extended Identifier bits

### BUFFER 21-7: CANx MESSAGE BUFFER WORD 6

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte	7<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte	6<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set	et '0' = Bit is cleared x = Bit is unknown			nown	

bit 15-8 Byte 7<15:8>: CANx Message Byte 7

bit 7-0 Byte 6<7:0>: CANx Message Byte 6

### BUFFER 21-8: CANx MESSAGE BUFFER WORD 7

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—			FILHIT<4:0>(1	)	
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12-8	FILHIT<4:0>: Filter Hit Code bits <sup>(1)</sup>
	Encodes number of filter that resulted in writing this buffer.

bit 7-0 Unimplemented: Read as '0'

**Note 1:** Only written by module for receive buffers, unused for transmit buffers.





# REGISTER 28-3: PMADDR: PARALLEL MASTER PORT ADDRESS REGISTER (MASTER MODES ONLY)<sup>(1,2)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
CS2	CS1	ADDR13	ADDR12	ADDR11	ADDR10	ADDR9	ADDR8	
bit 15	•	•		·		•	bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	
bit 7	•	•		·		•	bit 0	
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'		
-n = Value at Reset '1' = Bit is set				'0' = Bit is cleared x = Bit is unknown				
bit 15 bit 14	CS2: Chip Set If PMCON<7: 1 = Chip Sete 0 = Chip Sete If PMCON<7: Bit functions a CS1: Chip Sete If PMCON<7: 1 = Chip Sete 0 = Chip Sete If PMCON<7: Bit functions a	elect 2 bit $6 \ge 10 \text{ or } 01$ : $2 \ge 10 \text{ or } 01$ : $2 \ge 10 \text{ or } 00$ : $3 \ge 400 \text{ R}^3$ . $4 \ge 10 \text{ or } 00$ : $4 \ge 10 \text{ or } 00$ : $4 \ge 10 \text{ or } 10$ : $4 \ge 10 \text{ or } 10$ : $4 \ge 10 \text{ or } 00$ : $4 \ge 10 $						
bit 13-0	ADDR<13:0>	ADDR<13:0>: Destination Address bits						

**Note 1:** In Enhanced Slave mode, PMADDR functions as PMDOUT1, one of the two Data Buffer registers.

2: This register is not available on 44-pin devices.

#### TABLE 33-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Parameter No.	Тур. <sup>(2)</sup>	Max.	Units	Conditions			
Power-Down Current (IPD) <sup>(1)</sup>							
DC60d	35	100	μA	-40°C		Base Power-Down Current	
DC60c	40	200	μA	+25°C	2 21/		
DC60b	250	500	μA	+85°C	3.3V		
DC60c	1000	2500	μA	+125°C			
DC61d	8	10	μA	-40°C		Watchdog Timer Current: ∆IwDT <sup>(3)</sup>	
DC61c	10	15	μA	+25°C	2.21/		
DC61b	12	20	μA	+85°C	3.3V		
DC61c	13	25	μA	+125°C			

Note 1: IPD (Sleep) current is measured as follows:

CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with
 external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- CLKO is configured as an I/O input pin in the Configuration Word
- · All I/O pins are configured as outputs and driving low
- $\overline{\text{MCLR}}$  = VDD, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all ones)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
   ITAC is disabled
- JTAG is disabled
- 2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise specified.
- **3:** The ∆ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

# TABLE 33-37:SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS

		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)						
AC CHARACTERISTICS								
			Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial					
	1	1			$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended			
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Тур. <sup>(2)</sup>	Max.	Units	Conditions	
SP70	FscP	Maximum SCKx Input Frequency	—		11	MHz	(Note 3)	
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCKx Input Rise Time	—		-	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDOx Data Output Fall Time	—			ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDOx Data Output Rise Time	—			ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30			ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30			ns		
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx ↓ Input	120	_	—	ns		
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance	10		50	ns	(Note 4)	
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	1.5 Tcy + 40	_	—	ns	(Note 4)	
SP60	TssL2doV	SDOx Data Output Valid after SSx Edge	—	—	50	ns		

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.



#### FIGURE 33-28: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

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