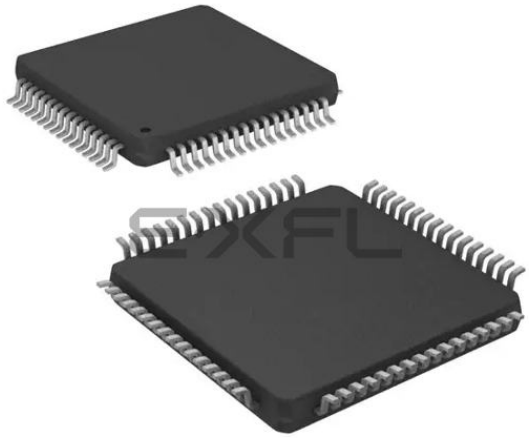
# Microchip Technology - DSPIC33EP128GM306-H/PT Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | - |
| Connectivity | I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 53 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | - |
| Data Converters | A/D 30x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 150°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm306-h-pt |

REGISTER 6-1: RCON: RESET CONTROL REGISTER(1)

| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRAPR | IOPUWR | — | — | VREGSF | — | CM | VREGS |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| EXTR | SWR | SWDTEN(2) | WDTO | SLEEP | IDLE | BOR | POR |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

*bit 15* TRAPR: *Trap Reset Flag bit*
**1** = *A Trap Conflict Reset has occurred*
**0** = *A Trap Conflict Reset has not occurred*

*bit 14* IOPUWR: *Illegal Opcode or Uninitialized W Access Reset Flag bit*
**1** = *An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset*
**0** = *An illegal opcode or Uninitialized W Register Reset has not occurred*

*bit 13-12* Unimplemented: *Read as '***0***'*

*bit 11* VREGSF: *Flash Voltage Regulator Standby During Sleep bit*
**1** = *Flash Voltage regulator is active during Sleep*
**0** = *Flash Voltage regulator goes into Standby mode during Sleep*

*bit 10* Unimplemented: *Read as '***0***'*

*bit 9* CM: *Configuration Mismatch Flag bit*
**1** = *A Configuration Mismatch Reset has occurred.*
**0** = *A Configuration Mismatch Reset has NOT occurred*

*bit 8* VREGS: *Voltage Regulator Standby During Sleep bit*
**1** = *Voltage regulator is active during Sleep*
**0** = *Voltage regulator goes into Standby mode during Sleep*

*bit 7* EXTR: *External Reset (*$\overline{MCLR}$*) Pin bit*
**1** = *A Master Clear (pin) Reset has occurred*
**0** = *A Master Clear (pin) Reset has not occurred*

*bit 6* SWR: *Software* **RESET** *(Instruction) Flag bit*
**1** = *A* **RESET** *instruction has been executed*
**0** = *A* **RESET** *instruction has not been executed*

*bit 5* SWDTEN: *Software Enable/Disable of WDT bit* (2)
**1** = *WDT is enabled*
**0** = *WDT is disabled*

*bit 4* WDTO: *Watchdog Timer Time-out Flag bit*
**1** = *WDT time-out has occurred*
**0** = *WDT time-out has not occurred*

Note 1: *All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.*

2: *If the FWDTEN Configuration bit is '***1***' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.*


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**TABLE 4-7: PTG REGISTER MAP**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTGCST | 0AC0 | PTGEN | — | PTGSIDL | PTGTOGL | — | PTGSWT | PTGSSEN | PTGIVIS | PTGSTRT | PTGWDTO | — | — | — | — | PTGITM1 | PTGITM0 | 0000 |
| PTGCON | 0AC2 | PTGCLK2 | PTGCLK1 | PTGCLK0 | PTGDIV4 | PTGDIV3 | PTGDIV2 | PTGDIV1 | PTGDIV0 | PTGPWD3 | PTGPWD2 | PTGPWD1 | PTGPWD0 | — | PTGWDT2 | PTGWDT1 | PTGWDT0 | 0000 |
| PTGBTE | 0AC4 | ADCTS4 | ADCTS3 | ADCTS2 | ADCTS1 | IC4TSS | IC3TSS | IC2TSS | IC1TSS | OC4CS | OC3CS | OC2CS | OC1CS | OC4TSS | OC3TSS | OC2TSS | OC1TSS | 0000 |
| PTGHOLD | 0AC6 | PTGHOLD<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGT0LIM | 0AC8 | PTGT0LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGT1LIM | 0ACA | PTGT1LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGSDLIM | 0ACC | PTGSDLIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGC0LIM | 0ACE | PTGC0LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGC1LIM | 0AD0 | PTGC1LIM<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGADJ | 0AD2 | PTGADJ<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGL0 | 0AD4 | PTGL0<15:0> | | | | | | | | | | | | | | | | 0000 |
| PTGQPTR | 0AD6 | — | — | — | — | — | — | — | — | — | — | — | PTGQPTR<4:0> | | | | | 0000 |
| PTGQUE0 | 0AD8 | STEP1<7:0> | | | | | | | | STEP0<7:0> | | | | | | | | 0000 |
| PTGQUE1 | 0ADA | STEP3<7:0> | | | | | | | | STEP2<7:0> | | | | | | | | 0000 |
| PTGQUE2 | 0ADC | STEP5<7:0> | | | | | | | | STEP4<7:0> | | | | | | | | 0000 |
| PTGQUE3 | 0ADE | STEP7<7:0> | | | | | | | | STEP6<7:0> | | | | | | | | 0000 |
| PTGQUE4 | 0AE0 | STEP9<7:0> | | | | | | | | STEP8<7:0> | | | | | | | | 0000 |
| PTGQUE5 | 0AE2 | STEP11<7:0> | | | | | | | | STEP10<7:0> | | | | | | | | 0000 |
| PTGQUE6 | 0AE4 | STEP13<7:0> | | | | | | | | STEP12<7:0> | | | | | | | | 0000 |
| PTGQUE7 | 0AE6 | STEP15<7:0> | | | | | | | | STEP14<7:0> | | | | | | | | 0000 |
| PTGQUE8 | 0x0AE8 | STEP17<7:0> | | | | | | | | STEP16<7:0> | | | | | | | | 0000 |
| PTGQUE9 | 0x0AEA | STEP19<7:0> | | | | | | | | STEP18<7:0> | | | | | | | | 0000 |
| PTGQUE10 | 0x0AEC | STEP21<7:0> | | | | | | | | STEP20<7:0> | | | | | | | | 0000 |
| PTGQUE11 | 0x0AEE | STEP23<7:0> | | | | | | | | STEP22<7:0> | | | | | | | | 0000 |
| PTGQUE12 | 0x0AF0 | STEP25<7:0> | | | | | | | | STEP24<7:0> | | | | | | | | 0000 |
| PTGQUE13 | 0x0AF2 | STEP27<7:0> | | | | | | | | STEP26<7:0> | | | | | | | | 0000 |
| PTGQUE14 | 0x0AF4 | STEP29<7:0> | | | | | | | | STEP28<7:0> | | | | | | | | 0000 |
| PTGQUE15 | 0x0AF6 | STEP31<7:0> | | | | | | | | STEP30<7:0> | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-22: ADC1 AND ADC2 REGISTER MAP**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC1BUF0 | 0300 | ADC1 Data Buffer 0 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF1 | 0302 | ADC1 Data Buffer 1 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF2 | 0304 | ADC1 Data Buffer 2 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF3 | 0306 | ADC1 Data Buffer 3 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF4 | 0308 | ADC1 Data Buffer 4 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF5 | 030A | ADC1 Data Buffer 5 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF6 | 030C | ADC1 Data Buffer 6 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF7 | 030E | ADC1 Data Buffer 7 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF8 | 0310 | ADC1 Data Buffer 8 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF9 | 0312 | ADC1 Data Buffer 9 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFA | 0314 | ADC1 Data Buffer 10 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFB | 0316 | ADC1 Data Buffer 11 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFC | 0318 | ADC1 Data Buffer 12 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFD | 031A | ADC1 Data Buffer 13 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFE | 031C | ADC1 Data Buffer 14 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFF | 031E | ADC1 Data Buffer 15 | | | | | | | | | | | | | | | | xxxx |
| AD1CON1 | 0320 | ADON | — | ADSIDL | ADDMABM | — | AD12B | FORM1 | FORM0 | SSRC2 | SSRC1 | SSRC0 | SSRCG | SIMSAM | ASAM | SAMP | DONE | 0000 |
| AD1CON2 | 0322 | VCFG2 | VCFG1 | VCFG0 | OFFCAL | — | CSCNA | CHPS1 | CHPS0 | BUFS | SMPI4 | SMPI3 | SMPI2 | SMPI1 | SMPI0 | BUFM | ALTS | 0000 |
| AD1CON3 | 0324 | ADRC | — | — | SAMC4 | SAMC3 | SAMC2 | SAMC1 | SAMC0 | ADCS7 | ADCS6 | ADCS5 | ADCS4 | ADCS3 | ADCS2 | ADCS1 | ADCS0 | 0000 |
| AD1CHS123 | 0326 | — | — | — | CH123SB2 | CH123SB1 | CH123NB1 | CH123NB0 | CH123SB0 | — | — | — | CH123SA2 | CH123SA1 | CH123NA1 | CH123NA0 | CH123SA0 | 0000 |
| AD1CHS0 | 0328 | CH0NB | — | CH0SB5 | CH0SB4 | CH0SB3 | CH0SB2 | CH0SB1 | CH0SB0 | CH0NA | — | CH0SA5 | CH0SA4 | CH0SA3 | CH0SA2 | CH0SA1 | CH0SA0 | 0000 |
| AD1CSSH | 032E | CSS<31:16> | | | | | | | | | | | | | | | | 0000 |
| AD1CSSL | 0330 | CSS<15:0> | | | | | | | | | | | | | | | | 0000 |
| AD1CON4 | 0332 | — | — | — | — | — | — | — | ADDMAEN | — | — | — | — | — | DMABL2 | DMABL1 | DMABL0 | 0000 |
| ADC2BUF0 | 0340 | ADC2 Data Buffer 0 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF1 | 0342 | ADC2 Data Buffer 1 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF2 | 0344 | ADC2 Data Buffer 2 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF3 | 0346 | ADC2 Data Buffer 3 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF4 | 0348 | ADC2 Data Buffer 4 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF5 | 034A | ADC2 Data Buffer 5 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF6 | 034C | ADC2 Data Buffer 6 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF7 | 034E | ADC2 Data Buffer 7 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUF8 | 0350 | ADC2 Data Buffer 8 | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Bits 13 and bit 5 are reserved in the AD2CHS0 register, unlike the AD1CHS0 register.



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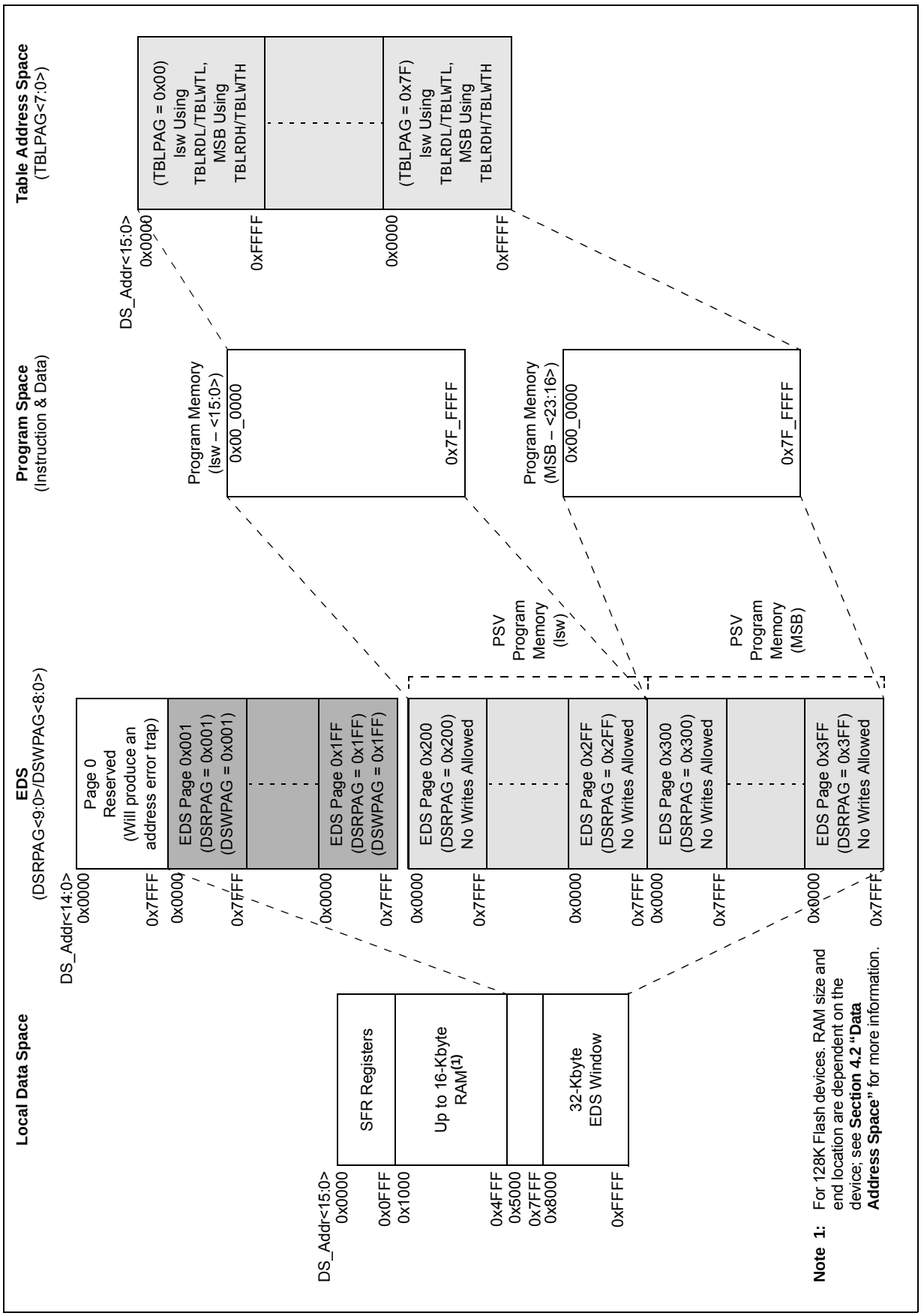
**FIGURE 4-10: PAGED DATA MEMORY SPACE**




**Note 1:** For 128K Flash devices, RAM size and end location are dependent on the device; see **Section 4.2 "Data Address Space"** for more information.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**REGISTER 13-2: TyCON (T3CON, T5CON, T7CON AND T9CON) CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON(1) | — | TSIDL(2) | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE(1) | TCKPS1(1) | TCKPS0(1) | — | — | TCS(1,3) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timery On bit(1)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(2)
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(1,3)
1 = External clock from pin, TyCK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through TxCON.

**2:** When 32-bit timer operation is enabled (T32 = 1) in the Timerx Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

**3:** The TyCK pin is not available on all timers. See the **"Pin Diagrams"** section for the available pins.

**REGISTER 16-25: PWMCAPx: PWMx PRIMARY TIME BASE CAPTURE REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PWMCAPx<15:8>(1,2) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PWMCAPx<7:0>(1,2) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PWMCAPx<15:0>:** PWMx Captured Time Base Value bits(1,2)
The value in this register represents the captured PWMx time base value when a leading edge is detected on the current-limit input.

**Note 1:** The capture feature is only available on a primary output (PWMxH).
**2:** This feature is active only after LEB processing on the current-limit input signal is complete.

**TABLE 33-53: OP AMP/COMPARATOR VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 2): 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| VR310 | TSET | Settling Time | — | 1 | 10 | μs | **(Note 1)** |

**Note 1:** Settling time is measured while CVRR = 1 and the CVR<3:0> bits transition from '0000' to '1111'.

**2:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

**TABLE 33-54: OP AMP/COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| VRD310 | CVRES | Resolution | CVRSRC/24 | — | CVRSRC/32 | LSb | |
| VRD311 | CVRAA | Absolute Accuracy of Internal DAC Input to Comparators | — | — | ±25 | mV | AVDD = CVRSRC = 3.3V |
| VRD312 | CVRAA1 | Absolute Accuracy of CVREFXO pins | — | — | +75/-25 | mV | AVDD = CVRSRC = 3.3V |
| VRD313 | CVRSRC | Input Reference Voltage | 0 | — | AVDD + 0.3 | V | |
| VRD314 | CVROUT | Buffer Output Resistance | — | 1.5k | — | Ω | |
| VRD315 | CVCL | Permissible Capacitive Load (CVREFXO pins) | — | — | 25 | pF | |
| VRD316 | IOCVR | Permissible Current Output (CVREFXO pins) | — | — | 1 | mA | |
| VRD317 | ION | Current Consumed When Module is Enabled | — | — | 500 | μA | AVDD = 3.6V |
| VRD318 | IOFF | Current Consumed When Module is Disabled | — | — | 1 | nA | AVDD = 3.6V |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

**NOTES:**


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