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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 30x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm306t-i-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 4-1:	CPU CORE REGISTER MAP	(CONTINUED)
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SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	С	0000
CORCON	0044	VAR	—	US1	US0	EDT	DL1	DL2	DL0	SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020
MODCON	0046	XMODEN	DEN YMODEN BWM3 BWM2 BWM1 BWM0 YWM3 YWM2 YWM1 YWM0 XWM3 XWM2 XWM1 XW											XWM0	0000			
XMODSRT	0048							XMC	DSRT<15:0	>							_	0000
XMODEND	004A							XMC	DEND<15:0)>							_	0001
YMODSRT	004C							YMC	DSRT<15:0	>							_	0000
YMODEND	004E							YMC	DEND<15:0)>							_	0001
XBREV	0050	BREN							XBF	REV<14:0>								0000
DISICNT	0052	_	_							DISICNT<	13:0>							0000
TBLPAG	0054	_	— — — — — — — TBLPAG<7:0>										0000					
MSTRPR	0058								MSTRPR<	:15:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-46: PORTA REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES

								1			1		1		1		(1
SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	TRISA	<15:14>	_			TRISA<	12:7>			—	—	TRISA4	-	—	TRISA	<1:0>	DF9F
PORTA	0E02	RA<1	5:14>	_			RA<12	2:7>			_	_	RA4	_	_	RA<	1:0>	0000
LATA	0E04	LATA<	15:14>	_			LATA<1	2:7>			_	_	LATA4	_	_	LATA	<1:0>	0000
ODCA	0E06	ODCA<	<15:14>	_			ODCA<	12:7>			_	_	ODCA4	_	_	ODCA	<1:0>	0000
CNENA	0E08	CNIEA	<15:14>	_			CNIEA<	12:7>			_	_	CNIEA4	_	_	CNIEA	<1:0>	0000
CNPUA	0E0A	CNPUA	<15:14>	_			CNPUA<	:12:7>			_	_	CNPUA4	_	_	CNPU	4<1:0>	0000
CNPDA	0E0C	CNPDA	<15:14>	_			CNPDA<	:12:7>			_	_	CNPDA4	_	_	CNPD	4<1:0>	0000
ANSELA	0E0E	ANSA<	<15:14>	_	ANSA<	12:11>		ANSA9	_	_	_	_	ANSA4		_	ANSA	<1:0>	1813

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-47: PORTA REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00		—	_			TRISA<	12:7>				—	TRISA4	_	—	TRISA	<1:0>	DF9F
PORTA	0E02	—	—	_		RA<12:7>					_	_	RA4	-	—	RA<	RA<1:0>	
LATA	0E04	—	_				LATA<1	2:7>			_	_	LATA4		_	LATA	<1:0>	0000
ODCA	0E06	—	—	_			ODCA<	12:7>			_	—	ODCA4	-	—	ODCA	<1:0>	0000
CNENA	0E08	—	—				CNIEA<	12:7>			—	_	CNIEA4		_	CNIEA	<1:0>	0000
CNPUA	0E0A	—	_				CNPUA<	12:7>			_	_	CNPUA4		_	CNPU	4<1:0>	0000
CNPDA	0E0C	—	—			CNPDA<12:7>					_	—	CNPDA4		—	CNPD	۹<1:0>	0000
ANSELA	0E0E	_	_		ANSA<	12:11>	_	ANSA9	_		_	_	ANSA4		_	ANSA	<1:0>	1813

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-48: PORTA REGISTER MAP FOR dsPIC33EPXXXGM304/604 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	_	_	_	_	_		TRISA	<10:7>		_	_		-	TRISA<4:0	>		DF9F
PORTA	0E02	_	_	_	-	—	RA<10:7>				—	_		RA<4:0>				
LATA	0E04	_	_	_	_	—		LATA<	10:7>		—	_		LATA<4:0>			0000	
ODCA	0E06	_	_	_	_	—		ODCA.	<10:7>		—	_	ODCA<4:0>				0000	
CNENA	0E08	—	_	—	—	—		CNIEA	<10:7>		_	—		(CNIEA<4:0	>		0000
CNPUA	0E0A	_	_	_	_	—		CNPUA	<10:7>		—	_		C	NPUA<4:0	>		0000
CNPDA	0E0C	_	_	_	_	_	CNPDA<10:7>		_	_		C	NPDA<4:0	>		0000		
ANSELA	0E0E	_	_	_	_	_	_	ANSA9	_	_	_	_	ANSA4	_		ANSA<2:0>	>	1813

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Logondy							bit 0
							bit 0
bit 7							
OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
bit 15							bit 8
IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

'0' = Bit is cleared

REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

bit 15-8 **IC8MD:IC1MD:** Input Capture x (x = 1-8) Module Disable bits

'1' = Bit is set

1 = Input Capture x module is disabled

-n = Value at POR

0 = Input Capture x module is enabled

bit 7-0 OC8MD:OC1MD: Output Compare x (x = 1-8) Module Disable bits

1 = Output Compare x module is disabled

0 = Output Compare x module is enabled

x = Bit is unknown





16.1.2 WRITE-PROTECTED REGISTERS

On dsPIC33EPXXXGM3XX/6XX/7XX devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FOSCSEL<6>). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring: PWMLOCK = 0.

To gain write access to these locked registers, the user application must write two consecutive values of 0xABCD and 0x4321 to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in Example 16-1.

EXAMPLE 16-1: PWM1 WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

; FLT32 pin must be pulle	d high externally in order to clear and disable the fault
; Writing to FCLCON1 regi	ster requires unlock sequence
<pre>mov #0xabcd, w10 mov #0x4321, w11 mov #0x0000, w0 mov w10, PWMKEY mov w11, PWMKEY mov w0, FCLCON1</pre>	<pre>; Load first unlock key to w10 register ; Load second unlock key to w11 register ; Load desired value of FCLCON1 register in w0 ; Write first unlock key to PWMKEY register ; Write second unlock key to PWMKEY register ; Write desired value to FCLCON1 register</pre>
; Set PWM ownership and p	olarity using the IOCON1 register
; Writing to IOCON1 regis	ter requires unlock sequence
<pre>mov #0xabcd, w10 mov #0x4321, w11 mov #0xF000, w0 mov w10, PWMKEY mov w11, PWMKEY mov w0, IOCON1</pre>	<pre>; Load first unlock key to w10 register ; Load second unlock key to w11 register ; Load desired value of IOCON1 register in w0 ; Write first unlock key to PWMKEY register ; Write second unlock key to PWMKEY register ; Write desired value to IOCON1 register</pre>

REGISTER 16-14: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	Ex<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	Ex<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 **PHASEx<15:0>:** Phase-Shift Value or Independent Time Base Period for the PWMx Generator bits

- Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs.
 2: If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
 - Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent Time Base Period Value for PWMxH and PWMxL.

REGISTER 16-15: SPHASEx: PWMx SECONDARY PHASE-SHIFT REGISTER^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SPHAS	Ex<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SPHAS	SEx<7:0>			
bit 7							bit 0
Legend:							
R = Readable b	oit	W = Writable bit	t	U = Unimpler	mented bit, read	l as '0'	

bit 15-0 **SPHASEx<15:0>:** Secondary Phase Offset for PWMxL Output Pin bits (used in Independent PWM mode only)

'1' = Bit is set

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:

Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), SPHASEx<15:0> = Not used.

'0' = Bit is cleared

- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), SPHASEx<15:0> = Phase-Shift Value for PWMxL only.
- 2: If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
 - Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), SPHASEx<15:0> = Not used.
 - True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), SPHASEx<15:0> = Independent Time Base Period Value for PWMxL only.

-n = Value at POR

x = Bit is unknown

21.0 CONTROLLER AREA NETWORK (CAN) MODULE (dsPIC33EPXXXGM6XX/7XX DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Enhanced Controller Area Network (ECAN™)"** (DS70353), which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

21.1 Overview

The Controller Area Network (CAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/ protocol was designed to allow communications within noisy environments. The dsPIC33EPXXXGM6XX/7XX devices contain two CAN modules.

The CAN module is a communication controller, implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details. The CAN module features are as follows:

- Implementation of the CAN protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- · Standard and Extended Data Frames
- 0-8 Bytes of Data Length
- Programmable Bit Rate, up to 1 Mbit/sec
- Automatic Response to Remote Transmission Requests
- Up to 8 Transmit Buffers with Application Specified Prioritization and Abort Capability (each buffer can contain up to 8 bytes of data)
- Up to 32 Receive Buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 Full (Standard/Extended Identifier) Acceptance Filters
- Three Full Acceptance Filter Masks
- DeviceNet[™] Addressing Support
- Programmable Wake-up Functionality with Integrated Low-Pass Filter
- Programmable Loopback mode supports Self-Test Operation
- Signaling via Interrupt Capabilities for all CAN Receiver and Transmitter Error States
- · Programmable Clock Source
- Programmable Link to Input Capture 2 (IC2) module for Timestamping and Network Synchronization
- · Low-Power Sleep and Idle modes

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—	_	—	—	_	_	—
bit 7							bit 0
Logondi							
R = Reada	uhle hit	W = Writable	hit	II = I Inimplen	nented hit read	l as 'N'	
-n = Value	at POR	'1' = Rit is set	bit	$0^{\circ} = \text{Bit is clear}$	ared	x = Ritis unkr	nown
					area		lowin
bit 15-10	ITRIM<5:0>:	Current Source	e Trim bits				
	011111 = Ma	iximum positive	e change from	nominal curren	t + 62%		
	011110 = Ma	iximum positive	e change from	nominal curren	t + 60%		
	•						
	•						
	000010 = M ir	nimum positive	change from r	nominal current	+ 4%		
	000001 = Mir	nimum positive	change from r	nominal current	+ 2%		
	1111111 = Mir	minal current o	e change from	nominal curren	t – 2%		
	111110 = Mi r	nimum negative	e change from	nominal curren	t – 4%		
	•						
	•						
	100010 = Ma	ximum negativ	e change from	nominal currer	nt – 60%		
	100001 = Ma	iximum negativ	e change from	nominal currer	nt – 62%		
bit 9-8	IRNG<1:0>: (Current Source	Range Select	bits			
	11 = 100 × Ba	ase Current ⁽²⁾					
	$10 = 10 \times Bas$	se Current ⁽²⁾					
	$01 = Base Cu00 = 1000 \times E$	Base Current ^{(1,}	2)				
bit 7-0	Unimplemen	ted: Read as '	0'				
Note 1:	This current range	e is not availab	le for use with	the internal ten	nperature meas	surement diode	2
2:	Refer to the CTM	U Current Sou	rce Specificatio	ons (Table 33-5	5) in Section 3	3.0 "Electrica	1
	Characteristics"	for the current	range selectio	n values.	,		

REGISTER 22-3: CTMUICON: CTMU CURRENT CONTROL REGISTER⁽³⁾

3: Current sources are not generated when 12-Bit ADC mode is chosen. Current sources are active only when 10-Bit ADC mode is chosen.

R/W-0	R/W-0	R/W-0	R/W-0	U	-0	R/W-0	R/W-0	R/W-0
VCFG2 ⁽¹⁾	VCFG1	¹⁾ VCFG0 ⁽¹⁾	OFFCAL	-	_	CSCNA	CHPS1	CHPS0
bit 15								bit 8
R-0	R/W-0	R/W-0	R/W-0	R/V	V-0	R/W-0	R/W-0	R/W-0
BUFS	SMPI4	SMPI3	SMPI2	SM	PI1	SMPI0	BUFM	ALTS
bit 7								bit 0
Legend: R = Readable	bit	W = Writable bi		U = U	nimpler	mented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set	•	'0' = B	it is cle	ared	x = Bit is unk	nown
bit 15-13	VCFG<2:	0>: Converter Voltag	e Reference	Configu	uration	bits ⁽¹⁾		
	Value	VREFH	VREFL					
	000	Avdd	Avss					
	001	External VREF+(2)	Avss					
	010	Avdd	External VR	2EF-(2)				
	011	External VREF+(2)	External VR	_{REF-} (2)				
	1xx	Avdd	Avss					
bit 12	OFFCAL:	Offset Calibration N	ode Select b	it				

NO. ADCY CONTROL DECISTED

1 = + and – inputs of channel Sample-and-Hold are connected to AVss

0 = + and – inputs of channel Sample-and-Hold are normal

- bit 11 Unimplemented: Read as '0'
- bit 10 **CSCNA:** Input Scan Select bit
 - 1 = Scans inputs for CH0+ during Sample MUXA

0 = Does not scan inputs

bit 9-8 CHPS<1:0>: Channel Select bits

In 12-Bit Mode (AD12B = 1), CHPS<1:0> Bits are Unimplemented and are Read as '00':

- 1x = Converts CH0, CH1, CH2 and CH3
- 01 = Converts CH0 and CH1
- 00 = Converts CH0
- bit 7 **BUFS:** Buffer Fill Status bit (only valid when BUFM = 1)
 - 1 = ADCx is currently filling the second half of the buffer; the user application should access data in the first half of the buffer
 - 0 = ADCx is currently filling the first half of the buffer; the user application should access data in the second half of the buffer
- **Note 1:** The '001', '010' and '011' bit combinations for VCFG<2:0> are not applicable on ADC2.
 - 2: ADC2 does not support external VREF± inputs.

REGISTER 25-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	—	—	—	—	—	_
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—	—			PTGQPTR<4:0	>	
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unk	nown

bit 15-5 Unimplemented: Read as '0'

bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits This register points to the currently active Step command in the step queue.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 25-13: PTGQUEX: PTG STEP QUEUE REGISTER x (x = 0-15)^(1,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			STEP(2x +	- 1)<7:0> (2)				
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	STEP(2x)<7:0> ⁽²⁾							
bit 7							bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8STEP(2x + 1)<7:0>: PTG Step Queue Pointer Register bits⁽²⁾
A queue location for storage of the STEP(2x +1) command byte.bit 7-0STEP(2x)<7:0>: PTG Step Queue Pointer Register bits⁽²⁾

A queue location for storage of the STEP(2x) command byte.

- **Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).
 - 2: Refer to Table 25-1 for the Step command encoding.
 - 3: The Step registers maintain their values on any type of Reset.

REGISTER 26-2: CMxCON: OP AMP/COMPARATOR x CONTROL REGISTER (x = 1, 2, 3 OR 5)

bit 7

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CON	COE	CPOL	—	—	OPMODE ⁽²⁾	CEVT ⁽³⁾	COUT
bit 15							bit 8
R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1 ⁽³⁾	EVPOL0 ⁽³⁾	_	CREF ⁽¹⁾	_	_	CCH1 ⁽¹⁾	CCH0 ⁽¹⁾

_	-					
		ł	ni	t	n	

Legend:						
R = Readable	e bit	W = Writable bit	U = Unimplemented bit	, read as '0'		
-n = Value at	POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		
bit 15	CON: Op 1 = Com 0 = Com	o Amp/Comparator Enable b parator is enabled parator is disabled	it			
bit 14	COE: Co 1 = Com 0 = Com	omparator Output Enable bit parator output is present on parator output is internal only	the CxOUT pin y			
bit 13	it 13 CPOL: Comparator Output Polarity Select bit 1 = Comparator output is inverted 0 = Comparator output is not inverted					
bit 12-11	Unimple	mented: Read as '0'				
bit 10	OPMOD	E: Op Amp Select bit ⁽²⁾				
	1 = Op a 0 = Op a	mp is enabled mp is disabled				
bit 9	CEVT: C	omparator Event bit ⁽³⁾				
	1 = Con inter 0 = Con	nparator event, according to rupts until the bit is cleared nparator event did not occur	the EVPOL<1:0> settings, occ	curred; disables future triggers and		
bit 8	COUT: C	Comparator Output bit				
	When CI 1 = VIN+ 0 = VIN+ When CI 1 = VIN+ 0 = VIN+	POL = 0 (non-inverted polarit > VIN- < VIN- POL = 1 (inverted polarity): < VIN-	t <u>y):</u>			

- **Note 1:** Inputs that are selected and not available will be tied to Vss. See the "**Pin Diagrams**" section for available inputs for each package.
 - **2:** The op amp and the comparator can be used simultaneously in these devices. The OPMODE bit only enables the op amp while the comparator is still functional.
 - **3:** After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the Comparator Event bit, CEVT (CMxCON<9>), and the Comparator Combined Interrupt Flag, CMPIF (IFS1<2>), **must be cleared** before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

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U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	
—	—	—	—	—	WDAY2	WDAY1	WDAY0	
bit 15							bit 8	
U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
—	_	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unkn		iown		
bit 15-11	Unimplemen	ted: Read as '	0'					
bit 10-8	WDAY<2:0>:	Binary Coded	Decimal Value	e of Weekday I	Digit bits			
	Contains a value from 0 to 6.							
bit 7-6	Unimplemented: Read as '0'							
bit 5-4	5-4 HRTEN<1:0>: Binary Coded Decimal Value of Hour's Tens Digit bits							
	Contains a value from 0 to 2.							

REGISTER 27-6: RTCVAL (WHEN RTCPTR<1:0> = 01): WEEKDAY AND HOURS VALUE REGISTER⁽¹⁾

Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 27-7: RTCVAL (WHEN RTCPTR<1:0> = 00): MINUTES AND SECONDS VALUE REGISTER

HRONE<3:0>: Binary Coded Decimal Value of Hour's Ones Digit bits

U-0	R/W-x						
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8
U-0	R/W-x						
_	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7		•				•	bit 0
I a manual.							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14-12	MINTEN<2:0>: Binary Coded Decimal Value of Minute's Tens Digit bits
	Contains a value from 0 to 5.
bit 11-8	MINONE<3:0>: Binary Coded Decimal Value of Minute's Ones Digit bits
	Contains a value from 0 to 9.
bit 7	Unimplemented: Read as '0'
bit 6-4	SECTEN<2:0>: Binary Coded Decimal Value of Second's Tens Digit bits
	Contains a value from 0 to 5.
bit 3-0	SECONE<3:0>: Binary Coded Decimal Value of Second's Ones Digit bits
	Contains a value from 0 to 9.

bit 3-0

29.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33/PIC24 Family Reference Manual", "32-Bit Programmable Cyclic Redundancy Check (CRC)" (DS70346), which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-Programmable (up to 32nd order) polynomial CRC equation
- Interrupt Output
- Data FIFO

The programmable CRC generator provides a hardware-implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- · Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 29-1. A simple version of the CRC shift engine is shown in Figure 29-2.



FIGURE 29-1: CRC BLOCK DIAGRAM

dsPIC33EPXXXGM3XX/6XX/7XX





29.1 Overview

The CRC module can be programmed for CRC polynomials of up to the 32nd order, using up to 32 bits. Polynomial length, which reflects the highest exponent in the equation, is selected by the PLEN<4:0> bits (CRCCON2<4:0>).

The CRCXORL and CRCXORH registers control which exponent terms are included in the equation. Setting a particular bit includes that exponent term in the equation; functionally, this includes an XOR operation on the corresponding bit in the CRC engine. Clearing the bit disables the XOR.

For example, consider two CRC polynomials, one a 16-bit equation and the other a 32-bit equation:

 $\begin{array}{c} x16+x12+x5+1\\ \text{ and }\\ x32+x26+x23+x22+x16+x12+x11+x10+x8+\\ x7+x5+x4+x2+x+1 \end{array}$

To program these polynomials into the CRC generator, set the register bits as shown in Table 29-1.

Note that the appropriate positions are set to '1' to indicate that they are used in the equation (for example, X26 and X23). The 0 bit required by the equation is always XORed; thus, X0 is a don't care. For a polynomial of length N, it is assumed that the *N*th bit will always be used, regardless of the bit setting. Therefore, for a polynomial length of 32, there is no 32nd bit in the CRCxOR register.

TABLE 29-1:	CRC SETUP EXAMPLES FOR
	16 AND 32-BIT POLYNOMIAL

CBC Control	Bit Values				
Bits	16-Bit Polynomial	32-Bit Polynomial			
PLEN<4:0>	01111	11111			
X<31:16>	0000 0000 0000 000x	0000 0100 1100 0001			
X<15:0>	0001 0000 0010 000x	0001 1101 1011 011x			

REGISTER 30-1: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
			DEVID<	23:16> ⁽¹⁾			
bit 23							bit 16
R	R	R	R	R	R	R	R
			DEVID<	:15:8> (1)			
bit 15							bit 8
R	R	R	R	R	R	R	R
			DEVID	<7:0> ⁽¹⁾			
bit 7							bit 0
Legend:	: R = Read-Only bit U = Unimplemented bit						

bit 23-0 **DEVID<23:0>:** Device Identifier bits⁽¹⁾

Note 1: Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration *Bits*" (DS70663) for the list of device ID values.

REGISTER 30-2: DEVREV: DEVICE REVISION REGISTER

R	R	R	R	R	R	R	R
			DEVREV<	<23:16> (1)			
bit 23							bit 16
R	R	R	R	R	R	R	R
			DEVREV	<15:8> ⁽¹⁾			
bit 15							bit 8
R	R	R	R	R	R	R	R
			DEVREV	/<7:0> ⁽¹⁾			
bit 7							bit 0
Legend:	: R = Read-only bit U = Unimplemented bit						

bit 23-0 **DEVREV<23:0>:** Device Revision bits⁽¹⁾

Note 1: Refer to the "dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration *Bits*" (DS70663) for the list of device revision values.

DC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial								
				$-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended						
Param No.	Symbol	Characteristic	Min.	Conditions						
	VIL	Input Low Voltage								
DI10		Any I/O Pin and MCLR	Vss	—	0.2 VDD	V				
DI18		I/O Pins with SDAx, SCLx	Vss	—	0.3 VDD	V	SMBus disabled			
DI19		I/O Pins with SDAx, SCLx	Vss	—	0.8	V	SMBus enabled			
	Vih	Input High Voltage								
DI20		I/O Pins Not 5V Tolerant	0.8 Vdd	—	Vdd	V	(Note 3)			
		I/O Pins 5V Tolerant and MCLR	0.8 VDD	—	5.5	V	(Note 3)			
		I/O Pins with SDAx, SCLx	0.8 Vdd	—	5.5	V	SMBus disabled			
		I/O Pins with SDAx, SCLx	2.1	—	5.5	V	SMBus enabled			
	ICNPU	Change Notification Pull-up Current								
DI30			150	250	550	μA	VDD = 3.3V, VPIN = VSS			
	ICNPD	Change Notification Pull-Down Current ⁽⁴⁾								
DI31			20	50	100	μA	VDD = 3.3V, VPIN = VDD			

TABLE 33-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

- 2: Negative current is defined as current sourced by the pin.
- 3: See the "Pin Diagrams" section for the 5V tolerant I/O pins.
- 4: VIL source < (Vss 0.3). Characterized but not tested.

5: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

- 6: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.
- 7: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.





TABLE 33-31: QEIX INDEX PULSE TIMING REQUIREMENTS

AC CHARACTERISTICS			$ \begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array} $				
Param No.	Param Symbol Characteristic ⁽¹⁾		Min.	Max.	Units	Conditions	
TQ50	TqIL	Filter Time to Recognize Low with Digital Filter	3 * N * Tcy	_	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)	
TQ51	TqiH	Filter Time to Recognize High with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 2)	
TQ55	Tqidxr	Index Pulse Recognized to Position Counter Reset (ungated index)	3 Тсү	—	ns		

Note 1: These parameters are characterized but not tested in manufacturing.

2: Alignment of index pulses to QEAx and QEBx is shown for Position Counter Reset timing only. Shown for forward direction only (QEAx leads QEBx). Same timing applies for reverse direction (QEAx lags QEBx) but index pulse recognition occurs on falling edge.

34.2 AC Characteristics and Timing Parameters

The information contained in this section defines dsPIC33EPXXXGM3XX/6XX/7XX AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in **Section 33.2 "AC Characteristics and Timing Parameters"**, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in Section 33.2 "AC Characteristics and Timing Parameters" is the Industrial and Extended temperature equivalent of HOS53.

TABLE 34-10: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)				
Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ Operating voltage VDD range as described in Table 34-1.				

FIGURE 34-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



35.2 Package Details

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Lead Pitch	е	0.80 BSC			
Overall Height	Α	1.20			
Molded Package Thickness	A2 0.95 1.00			1.05	
Standoff	A1	0.05	0.15		
Foot Length	L	0.45 0.60 0.7			
Footprint	L1	1.00 REF			
Foot Angle	¢	0° 3.5° 7°			
Overall Width	E	12.00 BSC			
Overall Length D 12.00 BSC					
Molded Package Width E1			10.00 BSC		
Molded Package Length	D1	10.00 BSC			
Lead Thickness	С	0.09 – 0.20			
Lead Width	b	0.30 0.37 0.45			
Mold Draft Angle Top	α	11° 12° 13°			
Mold Draft Angle Bottom	β	11° 12° 13°			

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

100-Lead Plastic Thin Quad Flatpack (PT)-12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	0.40 BSC			
Contact Pad Spacing	C1	13.40		
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B