

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XE

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm310-e-bg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Ref-erence Manual"*, which are available from the Microchip web site (www.microchip.com). These documents should be considered as the general reference for the operation of a particular module or device feature.

- "Introduction" (DS70573)
- "CPU" (DS70359)
- "Data Memory" (DS70595)
- "Program Memory" (DS70613)
- "Flash Programming" (DS70609)
- "Interrupts" (DS70000600)
- "Oscillator" (DS70580)
- "Reset" (DS70602)
- "Watchdog Timer and Power-Saving Modes" (DS70615)
- "I/O Ports" (DS70000598)
- "Timers" (DS70362)
- "Input Capture" (DS70000352)
- "Output Compare" (DS70005157)
- "High-Speed PWM" (DS70645)
- "Quadrature Encoder Interface (QEI)" (DS70601)
- "Analog-to-Digital Converter (ADC)" (DS70621)
- "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582)
- "Serial Peripheral Interface (SPI)" (DS70005185)
- "Inter-Integrated Circuit™ (I²C™)" (DS70000195)
- "Data Converter Interface (DCI) Module" (DS70356)
- "Enhanced Controller Area Network (ECAN™)" (DS70353)
- "Direct Memory Access (DMA)" (DS70348)
- "Programming and Diagnostics" (DS70608)
- "Op Amp/Comparator" (DS70000357)
- "32-Bit Programmable Cyclic Redundancy Check (CRC)" (DS70346)
- "Parallel Master Port (PMP)" (DS70576)
- "Device Configuration" (DS70000618)
- "Peripheral Trigger Generator (PTG)" (DS70669)
- "Charge Time Measurement Unit (CTMU)" (DS70661)

dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 2-7: INTERLEAVED PFC



FIGURE 2-8: BEMF VOLTAGE MEASURED USING THE ADC MODULE



3.5 **Programmer's Model**

The programmer's model for the dsPIC33EPXXXGM3XX/ 6XX/7XX devices is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGM3XX/ 6XX/7XX devices contain control registers for Modulo Addressing and Bit-Reversed Addressing, and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Table 4-1.

Register(s) Name	Description
W0 through W15	Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine Status register
SPLIM	Stack Pointer Limit Value register
TBLPAG	Table Memory Page Address register
DSRPAG	Extended Data Space (EDS) Read Page register
DSWPAG	Extended Data Space (EDS) Write Page register
RCOUNT	REPEAT Loop Count register
DCOUNT	DO Loop Count register
DOSTARTH ⁽¹⁾ , DOSTARTL ⁽¹⁾	DO Loop Start Address register (High and Low)
DOENDH, DOENDL	DO Loop End Address register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Note 1: The DOSTARTH and DOSTARTL registers are read-only.

REGISTER 5-2: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—		—		_		—
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMADR	U<23:16>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 **NVMADRU<23:16>:** Nonvolatile Memory Upper Write Address bits Selects the upper 8 bits of the location to program or erase in program Flash memory. This register may be read or written to by the user application.

REGISTER 5-3: NVMADR: NONVOLATILE MEMORY LOWER ADDRESS REGISTER

'1' = Bit is set

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
1017 A					1010 A		1010 A
			NVMA	DR<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit		W = Writable bit		U = Unimpler	mented bit. read	l as '0'	

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Lower Write Address bits Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written to by the user application.

'0' = Bit is cleared

-n = Value at POR

x = Bit is unknown

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-29). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



11.4.4.1 Virtual Connections

dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 26-1 in Section 26.0 "Op Amp/Comparator Module") and the PTG module (see Section 25.0 "Peripheral Trigger Generator (PTG) Module").

In addition, dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual connections to the filtered QEIx module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in Section 17.0 "Quadrature Encoder Interface (QEI) Module").

Virtual connections provide a simple way of interperipheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of `b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEIx module allows peripherals to be connected to the QEIx digital filter input. To utilize this filter, the QEIx module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEIx digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43

RPINR15 = 0x2500; RPINR7 = 0x009;	/* /*	Connect Connect	the the	QEI IC1	1 HOME: input	l input to the	to RP37 digital	(pin 43 filter) */ on th	e FHOME1	input	*/
QEI1IOC = 0x4000; QEI1CON = 0x8000;	/* /*	Enable t Enable t	the Q the Q	2EI 2EI	digita: module	l filte: */	r */					

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC2R<6:0>			
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC1R<6:0>			
bit 7							bit C
Legend:							
R = Readat	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkı	nown
bit 15	Unimpleme	ented: Read as '	0'				
bit 14-8	IC2R<6:0>: (see Table 2	Assign Input Ca	apture 2 (IC2 selection nu) to the Correspo mbers)	onding RPn P	in bits	
	1111100 =	Input tied to RPI	1124				
	•						
	•						
	0000001 = 0000000 =	Input tied to CM Input tied to Vss	P1				
bit 7	Unimpleme	ented: Read as '	0'				
bit 6-0	IC1R<6:0>: (see Table ?	Assign Input Ca 11-2 for input pin	apture 1 (IC1) selection nu) to the Correspo mbers)	onding RPn P	in bits	
	1111100 =	Input tied to RP	1124				
	•						
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss	3				

REGISTER 11-4: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

REGISTER 11-30: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—			RP35	R<5:0>		
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				RP20	R<5:0>		
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplem	nented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15-14	Unimpleme	nted: Read as '	0'				
bit 13-8	RP35R<5:0>	Peripheral Ou	tput Function	n is Assigned to	RP35 Output	Pin bits	

	(see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP20R<5:0>: Peripheral Output Function is Assigned to RP20 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-31: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	_			RP37R<	<5:0>			
bit 15							bit 8	
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	_			RP36R<	<5:0>			
bit 7							bit 0	
Legend:								
R = Readable I	bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
-n = Value at P	-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown						nown	
							,	
bit 15-14	Unimpleme	nted: Read as '	0'					

bit 13-8 **RP37R<5:0>:** Peripheral Output Function is Assigned to RP37 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **RP36R<5:0>:** Peripheral Output Function is Assigned to RP36 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

- bit 4-0 SYNCSEL<4:0>: Trigger/Synchronization Source Selection bits 11111 = OCxRS compare event is used for synchronization 11110 = INT2 is the source for compare timer synchronization 11101 = INT1 is the source for compare timer synchronization 11100 = CTMU trigger is the source for compare timer synchronization 11011 = ADC1 interrupt is the source for compare timer synchronization 11010 = Analog Comparator 3 is the source for compare timer synchronization 11001 = Analog Comparator 2 is the source for compare timer synchronization 11000 = Analog Comparator 1 is the source for compare timer synchronization 10111 = Input Capture 8 interrupt is the source for compare timer synchronization 10110 = Input Capture 7 interrupt is the source for compare timer synchronization 10101 = Input Capture 6 interrupt is the source for compare timer synchronization 10100 = Input Capture 5 interrupt is the source for compare timer synchronization 10011 = Input Capture 4 interrupt is the source for compare timer synchronization 10010 = Input Capture 3 interrupt is the source for compare timer synchronization 10001 = Input Capture 2 interrupt is the source for compare timer synchronization 10000 = Input Capture 1 interrupt is the source for compare timer synchronization 01111 = GP Timer5 is the source for compare timer synchronization 01110 = GP Timer4 is the source for compare timer synchronization 01101 = GP Timer3 is the source for compare timer synchronization 01100 = GP Timer2 is the source for compare timer synchronization 01011 = GP Timer1 is the source for compare timer synchronization 01010 = PTGx trigger is the source for compare timer synchronization⁽³⁾ 01001 = Compare timer is unsynchronized 01000 = Output Compare 8 is the source for compare timer synchronization^(1,2) 00111 = Output Compare 7 is the source for compare timer synchronization^(1,2) 00110 = Output Compare 6 is the source for compare timer synchronization^(1,2) 00101 = Output Compare 5 is the source for compare timer synchronization^(1,2) 00100 = Output Compare 4 is the source for compare timer synchronization^(1,2) 00011 = Output Compare 3 is the source for compare timer synchronization^(1,2) 00010 = Output Compare 2 is the source for compare timer synchronization^(1,2) 00001 = Output Compare 1 is the source for compare timer synchronization^(1,2) 00000 = Compare timer is unsynchronized
- Note 1: Do not use the OCx module as its own synchronization or trigger source.
 - 2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.
 - 3: Each Output Compare x module (OCx) has one PTG Trigger/Sync source. See Section 25.0 "Peripheral Trigger Generator (PTG) Module" for more information.

PTGO4 = OC1, OC5 PTGO5 = OC2, OC6 PTGO6 = OC3, OC7 PTGO7 = OC4, OC8

16.2 PWMx Control Registers

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU ⁽¹⁾	SYNCPOL ⁽¹⁾	SYNCOEN ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN ⁽¹⁾	SYNCSRC2 ⁽¹⁾	SYNCSRC1 ⁽¹⁾	SYNCSRC0 ⁽¹⁾	SEVTPS3 ⁽¹⁾	SEVTPS2(1)	SEVTPS1 ⁽¹⁾	SEVTPS0 ⁽¹⁾
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	t HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	PTEN: PWMx Module Enable bit
	1 = PWMx module is enabled
	0 = PWMx module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	PTSIDL: PWMx Time Base Stop in Idle Mode bit
	 1 = PWMx time base halts in CPU Idle mode 0 = PWMx time base runs in CPU Idle mode
bit 12	SESTAT: Special Event Interrupt Status bit
	1 = Special event interrupt is pending
	0 = Special event interrupt is not pending
bit 11	SEIEN: Special Event Interrupt Enable bit
	1 = Special event interrupt is enabled
	0 = Special event interrupt is disabled
bit 10	EIPU: Enable Immediate Period Updates bit ⁽¹⁾
	1 = Active Period register is updated immediately
	0 = Active Period register updates occur on PWMx cycle boundaries
bit 9	SYNCPOL: Synchronize Input and Output Polarity bit ⁽¹⁾
	1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
	0 = SYNCI1/SYNCO1 is active-high
bit 8	SYNCOEN: Primary Time Base Sync Enable bit ⁽¹⁾
	1 = SYNCO1 output is enabled
	0 = SYNCO1 output is disabled
bit 7	SYNCEN: External Time Base Synchronization Enable bit ⁽¹⁾
	1 = External synchronization of primary time base is enabled
	0 = External synchronization of primary time base is disabled
Note 1:	These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.
•	

2: See Section 25.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

REGISTER 18-1: SPIx STAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

bit 1 SPITBF: SPIx Transmit Buffer Full Status bit

1 = Transmit has not yet started, SPIxTXB is full

0 = Transmit has started, SPIxTXB is empty

Standard Buffer Mode:

Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer Mode:

Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 SPIRBF: SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full

0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer Mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer Mode:

Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

REGISTER 20-2:	UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN ⁽¹⁾	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7 bit						bit 0	

Legend:	C = Clearable bit	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: UARTx Transmit Polarity Inversion bit

lf	IREN = 0:	
1	= UxTX Idle state is '(0'

0 = UxTX Idle state is '1'

- If IREN = 1:

 1 = IrDA encoded UxTX Idle state is '1'

 0 = IrDA encoded UxTX Idle state is '0'

 bit 12
 Unimplemented: Read as '0'

 bit 11
 UTXBRK: UARTx Transmit Break bit

 1 = Sends Sync Break on next transmission Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion

 0 = Sync Break transmission is disabled or has completed

 bit 10
 UTXEN: UARTx Transmit Enable bit⁽¹⁾

 1 = Transmit is enabled, UxTX pin is controlled by UARTx

 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset: UxTX pin is
 - 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by the PORT
- bit 9 UTXBF: UARTx Transmit Buffer Full Status bit (read-only)
 - 1 = Transmit buffer is full
 - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
 - 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
 - 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
 - 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
 - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters
- Note 1: Refer to the "dsPIC33/PIC24 Family Reference Manual", "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582) for information on enabling the UART module for transmit operation.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0
bit 15	-	-					bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0
bit 7							bit 0
Legend:							
R = Readable bit W = Writable		bit	U = Unimpler	nented bit, read	l as '0'		
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	

REGISTER 21-15: CxBUFPNT4: CANx FILTERS 12-15 BUFFER POINTER REGISTER 4

bit 15-12	F15BP<3:0>: RX Buffer Mask for Filter 15 bits 1111 = Filter hits received in RX FIFO buffer 1110 = Filter hits received in RX Buffer 14
	•
	0001 = Filter hits received in RX Buffer 1 0000 = Filter hits received in RX Buffer 0
bit 11-8	F14BP<3:0>: RX Buffer Mask for Filter 14 bits (same values as bits 15-12)
bit 7-4	F13BP<3:0>: RX Buffer Mask for Filter 13 bits (same values as bits 15-12)
bit 3-0	F12BP<3:0>: RX Buffer Mask for Filter 12 bits (same values as bits 15-12)

REGISTER 23-5:	ADxCHS123: ADCx INPUT CHANNEL 1,	2, 3 SELECT REGISTER
----------------	----------------------------------	----------------------

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	—	—	CH123SB2	CH123SB1	CH123NB1	CH123NB0	CH123SB0		
bit 15							bit 8		
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	—	—	CH123SA2	CH123SA1	CH123NA1	CH123NA0	CH123SA0		
bit 7							bit 0		
Legend:									
R = Reada	ible bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'			
-n = Value	at POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkno	own		
bit 15-13 bit 12-11	 bit 15-13 Unimplemented: Read as '0' bit 12-11 CH123SB<2:1>: Channels 1, 2, 3 Positive Input Select for Sample B bits 1xx = CH1 positive input is AN0 (Op Amp 2), CH2 positive input is AN25 (Op Amp 5), CH3 positive input is AN6 (Op Amp 3) 011 = CH1 positive input is AN3 (Op Amp 1), CH2 positive input is AN0 (Op Amp 2), CH3 positive input is AN25 (Op Amp 5) 010 = CH1 positive input is AN3 (Op Amp 1), CH2 positive input is AN0 (Op Amp 2), CH3 positive input is AN3 (Op Amp 1), CH2 positive input is AN0 (Op Amp 2), CH3 positive input is AN3 (Op Amp 1), CH2 positive input is AN0 (Op Amp 2), CH3 positive input is AN3 (Op Amp 1), CH2 positive input is AN0 (Op Amp 2), CH3 positive input is AN3 (Op Amp 1), CH2 positive input is AN3 (Op Amp 2), CH3 positive input is AN3 (Op Amp 1), CH2 positive input is AN3 (Op Amp 2), CH3 positive input is AN3 (Op Amp 1), CH2 positive input is AN3 (Op Amp 2), CH3 positive input is AN3 (Op Amp 1), CH2 positive input is AN3 (Op Amp 2), CH3 positive input is AN3 (Op Amp 1), CH2 positive input is AN3 (Op Amp 2), CH3 positive input is AN3 (Op Amp 1), CH2 positive input is AN3 (Op Amp 2), CH3 positive input is AN3 (Op Amp 1), CH2 positive input is AN3 (Op Amp 2), CH3 positive input is AN3 (Op Amp 2), CH3								
bit 10-9	001 = CH1p 000 = CH1p CH123NB<1 11 = CH1 ne 10 = CH1 ne 0x = CH1 C	 cositive input is positive input is cositive input is channels gative input is cH3 pegat 	AN3, CH2 p0 AN0, CH2 pos 1, 2, 3 Negativ AN9, CH2 neg AN6, CH2 neg ve input is VR	sitive input is A sitive input select ative input is A ative input is A FEI (1)	AN4, CH3 posit AN1, CH3 posit t for Sample B AN10, CH3 neg AN7, CH3 nega	ive input is AN3 ive input is AN2 bits jative input is AI ative input is AN	N11 8		
bit 8	CH123SB0:	Channels 1, 2,	3 Positive Inp	ut Select for S	ample B bit				
bit o	See bits<12:	11> for bit select	tions.						
bit 7-5	Unimplemer	ted: Read as '	0'						
bit 4-3	CH123SA<2	:1>: Channels	1, 2, 3 Positive	e Input Select	for Sample A b	its			
	 1xx = CH1 positive input is AN0 (Op Amp 2), CH2 positive input is AN25 (Op Amp 5), CH3 positive input is AN6 (Op Amp 3) 011 = CH1 positive input is AN3 (Op Amp 1), CH2 positive input is AN0 (Op Amp 2), CH3 positive input is AN25 (Op Amp 5) 010 = CH1 positive input is AN3 (Op Amp 1), CH2 positive input is AN0 (Op Amp 2), CH3 positive input is AN6 (Op Amp 3) 001 = CH1 positive input is AN3, CH2 positive input is AN4, CH3 positive input is AN5 001 = CH1 positive input is AN3, CH2 positive input is AN4, CH3 positive input is AN5 								
bit 2-1	CH123NA<1 11 = CH1 ne 10 = CH1 ne 0x = CH1, Cl	 000 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2 CH123NA<1:0>: Channels 1, 2, 3 Negative Input Select for Sample A bits 11 = CH1 negative input is AN9, CH2 negative input is AN10, CH3 negative input is AN11 10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8 0x = CH1, CH2, CH3 negative input is VREFL 							
	See hits<4:3	> for the hit sel	ections		ample A bit				
Note 1:	The negative input	It to VREFL hap	pens only whe	en VCFG<2:0>	= 2 or 3 in the	ADxCON2 regi	ster. When		

Ote 1: The negative input to VREFL happens only when VCFG<2:0> = 2 or 3 in the ADXCON2 register VCFG<2:0> = 0 or 1, this negative input is internally routed to AVss.

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0
bit 7		•	•				bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	l as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15-13 bit 12-8	PTGCLK<2:0 111 = Reserv 110 = Reserv 101 = PTG m 100 = PTG m 011 = PTG m 010 = PTG m 001 = PTG m 000 = PTG m PTGDIV<4:02 11111 = Divic 00001 = Divic 00001 = Divic	 Select PTG red red nodule clock so PTG Module de-by-32 de-by-31 	Module Clock urce will be T3 urce will be T2 urce will be T4 urce will be T4 urce will be F6 urce will be F6 clock Presca	Source bits CLK CLK CLK D SC Ier (divider) bi	ts		
bit 7-4	<pre>PTGPWD<3:0>: PTG Trigger Output Pulse-Width bits 1111 = All trigger outputs are 16 PTG clock cycles wide 1110 = All trigger outputs are 15 PTG clock cycles wide</pre>						
bit 2-0		0>: Select PTG	~ Watchdog Tir	mer Time-out	Count Value hits	3	
UIL 2-U	111 = Watche 110 = Watche 101 = Watche 011 = Watche 011 = Watche 010 = Watche 001 = Watche 001 = Watche	dog Timer will t dog Timer is dis	ime-out after 5 ime-out after 2 ime-out after 1 ime-out after 3 ime-out after 3 ime-out after 8 sabled	512 PTG clock 256 PTG clock 28 PTG clock 34 PTG clocks 32 PTG clocks 6 PTG clocks 8 PTG clocks	Sound value bits	,	

REGISTER 25-2: PTGCON: PTG CONTROL REGISTER

REGISTER 25-6: PTGSDLIM: PTG STEP DELAY LIMIT REGISTER^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		10110		INA :45:05			
			PIGSDL	IIVI<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSDI	_IM<7:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGSDLIM<15:0>:** PTG Step Delay Limit Register bits Holds a PTG step delay value, representing the number of additional PTG clocks, between the start of a Step command and the completion of a Step command.

- **Note 1:** A base step delay of one PTG clock is added to any value written to the PTGSDLIM register (Step Delay = (PTGSDLIM) + 1).
 - 2: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 25-7: PTGC0LIM: PTG COUNTER 0 LIMIT REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC0	_IM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC0	LIM<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit	t	W = Writable bit		U = Unimpler	nented bit, read	l as '0'	

bit 15-0 **PTGC0LIM<15:0>:** PTG Counter 0 Limit Register bits

'1' = Bit is set

May be used to specify the loop count for the PTGJMPC0 Step command or as a limit register for the General Purpose Counter 0.

'0' = Bit is cleared

-n = Value at POR

x = Bit is unknown

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 27-10: ALRMVAL (WHEN ALRMPTR<1:0> = 00): ALARM MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x						
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x						
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14-12	MINTEN<2:0>: Binary Coded Decimal Value of Minute's Tens Digit bits
	Contains a value from 0 to 5.
bit 11-8	MINONE<3:0>: Binary Coded Decimal Value of Minute's Ones Digit bits
	Contains a value from 0 to 9.
bit 7	Unimplemented: Read as '0'
bit 6-4	SECTEN<2:0>: Binary Coded Decimal Value of Second's Tens Digit bits
	Contains a value from 0 to 5.
bit 3-0	SECONE<3:0>: Binary Coded Decimal Value of Second's Ones Digit bits
	Contains a value from 0 to 9.



AC CHARACTERISTICS			Standard Ope (unless other Operating tem	rating C wise stat perature	onditions: 3.0V to 3.6V ted) $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended			
Param No.	Symb	Characteristic	Min. Typ. ⁽¹⁾		Max.	Units	Conditions	
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	_	60	MHz	EC	
		Oscillator Crystal Frequency	3.5 10 32.4	 32.768	10 25 33.1	MHz MHz kHz	XT HS SOSC	
OS20	Tosc	Tosc = 1/Fosc	8.33	_	DC	ns	TA = +125°C	
		Tosc = 1/Fosc	7.14	—	DC	ns	TA = +85°C	
OS25	Тсү	Instruction Cycle Time ⁽²⁾	16.67	—	DC	ns	TA = +125°C	
			14.28		DC	ns	TA = +85°C	
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.375 x Tosc	_	0.625 x Tosc	ns	EC	
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time		_	20	ns	EC	
OS40	TckR	CLKO Rise Time ⁽³⁾	—	5.2	—	ns		
OS41	TckF	CLKO Fall Time ⁽³⁾	—	5.2	_	ns		
OS42	Gм	External Oscillator Transconductance ⁽⁴⁾	—	12	—	mA/V	HS, VDD = 3.3V, TA = +25°C	
			_	6	_	mA/V	XT, VDD = 3.3V, TA = +25°C	

TABLE 33-16: EXTERNAL CLOCK TIMING REQUIREMENTS

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- 2: Instruction cycle period (Tcr) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.
- 3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4: This parameter is characterized, but not tested in manufacturing.



TABLE 33-22: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS ⁽¹⁾

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Charae	cteristic ⁽²⁾	Min.	Тур.	Max.	Units	Conditions
TA10	TTXH T1CK High Synchronous Time mode		Greater of: 20 or (TCY + 20)/N	_	_	ns	Must also meet Parameter TA15, N = Prescaler value (1, 8, 64, 256)	
			Asynchronous	35	_	—	ns	
TA11	TTXL T1CK Low S Time m		Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TA15, N = Prescaler value (1, 8, 64, 256)
			Asynchronous	10		—	ns	
TA15	ΤτχΡ	T1CK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N		_	ns	N = Prescaler value (1, 8, 64, 256)
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS (T1CON<1>) bit)		DC	_	50	kHz	
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

Note 1: Timer1 is a Type A.

2: These parameters are characterized, but are not tested in manufacturing.

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$					
Param No.	Symbol	Characteristic	acteristic Min Typ Max				Conditions		
		ADC A	Accuracy	(12-Bit	Mode) ⁽¹⁾				
HAD20a	Nr	Resolution ⁽³⁾	1:	2 Data B	its	bits			
HAD21a	INL	Integral Nonlinearity	-6	_	6	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V		
HAD22a	DNL	Differential Nonlinearity	-1	—	1	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V		
HAD23a	Gerr	Gain Error	-10	_	10	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V		
HAD24a EOFF Offset Error -5 -5 LSb VINL = AVSS = VRE AVDD = VREFH = 3.							Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V		
		Dynamic	Performa	nce (12·	Bit Mode	e) ⁽²⁾			
HAD33a	FNYQ	Input Signal Bandwidth	_	—	200	kHz			

TABLE 34-14: ADCx MODULE SPECIFICATIONS (12-BIT MODE)

Note 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

TABLE 34-15: ADCx MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS				rd Opera otherwing tempe	ating Con ise stated erature	ditions: d) -40°C ≤	: 3.0V to 3.6V TA ≤ +150°C
Param No.	Symbol	Characteristic	Min Typ Max			Units	Conditions
		ADC A	ccuracy	(10-Bit I	Mode) ⁽¹⁾		
HAD20b	Nr	Resolution ⁽³⁾	1() Data B	its	bits	
HAD21b	INL	Integral Nonlinearity	-1.5	—	1.5	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
HAD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
HAD23b	Gerr	Gain Error	-2.5	—	2.5	LSb	Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
HAD24bEOFFOffset Error-1.251.25LSbVINL = AVSS = VREFL =AVDD = VREFH = 3.6V							Vinl = AVss = Vrefl = 0V, AVdd = Vrefh = 3.6V
		Dynamic F	Performa	nce (10-	Bit Mode	e) ⁽²⁾	
HAD33b	FNYQ	Input Signal Bandwidth	_	_	400	kHz	

Note 1: These parameters are characterized, but are tested at 20 ksps only.

2: These parameters are characterized by similarity, but are not tested in manufacturing.

3: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

APPENDIX A: REVISION HISTORY

Revision A (February 2013)

This is the initial released version of this document.

Revision B (June 2013)

Changes to Section 5.0 "Flash Program Memory", Register 5-1. Changes to Section 6.0 "Resets", Figure 6-1. Changes to Section 26.0 "Op Amp/Comparator Module", Register 26-2. Updates to most of the tables in Section 33.0 "Electrical Characteristics". Minor text edits throughout the document.

Revision C (September 2013)

Changes to Figure 23-1. Changes to Figure 26-2. Changes to Table 30-2. Changes to Section 33.0 "Electrical Characteristics". Added Section 34.0 "High-Temperature Electrical Characteristics" to the data sheet. Minor typographical edits throughout the document.

Revision D (August 2014)

This revision incorporates the following updates:

- Sections:
 - Updated Section 2.0 "Guidelines for Getting Started with 16-Bit Digital Signal Controllers", Section 8.0 "Direct Memory Access (DMA)", Section 10.3 "Doze Mode", Section 21.0 "Controller Area Network (CAN) Module (dsPIC33EPXXXGM6XX/7XX Devices Only)", Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)", Section 23.1.2 "12-Bit ADCx Configuration", Section 21.4 "CAN Message Buffers", Section 35.0 "Packaging Information"
- · Figures:
 - Updated **"Pin Diagrams"**, Figure 1-1, Figure 9-1
- · Registers:
 - Updated Register 5-1, Register 8-2, Register 21-1, Register 23-2
- · Tables:
 - Updated Table 1-1, Table 7-1, Table 8-1, Table 34-9, Table 1, Table 4-2, Table 4-3, Table 4-25, Table 4-33, Table 4-34, Table 4-39, Table 4-30, Table 4-46, Table 4-47, Table 33-16, Table 34-8