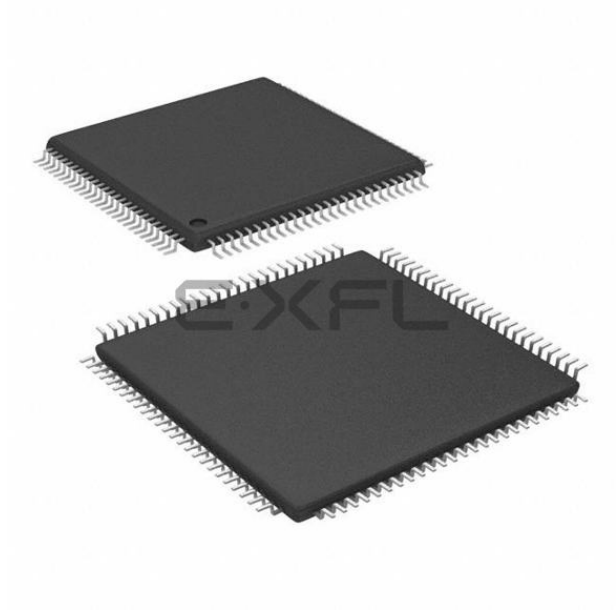
Microchip Technology - DSPIC33EP128GM310-I/PF Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm310-i-pf

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com)

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGM3XX/6XX/7XX family requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used)
  (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP
  (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER(3) (CONTINUED)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **SFA:** Stack Frame Active Status bit
1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1 **RND:** Rounding Mode Select bit
1 = Biased (conventional) rounding is enabled
0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
1 = Integer mode is enabled for DSP multiply
0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is always read as '0'.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.
3: Refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"CPU"** (DS70359) for more detailed information.

TABLE 4-19: UART3 AND UART4 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U3MODE	0250	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U3STA	0252	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U3TXREG	0254	—	—	—	—	—	—	—	UART3 Transmit Register									xxxx
U3RXREG	0256	—	—	—	—	—	—	—	UART3 Receive Register									0000
U3BRG	0258	Baud Rate Generator Prescaler																0000
U4MODE	02B0	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U4STA	02B2	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U4TXREG	02B4	—	—	—	—	—	—	—	UART4 Transmit Register									xxxx
U4RXREG	02B6	—	—	—	—	—	—	—	UART4 Receive Register									0000
U4BRG	02B8	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-20: SPI1, SPI2 AND SPI3 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI2CON1	0262	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI2BUF	0268	SPI2 Transmit and Receive Buffer Register																0000
SPI3STAT	02A0	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI3CON1	02A2	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI3CON2	02A4	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI3BUF	02A8	SPI3 Transmit and Receive Buffer Register																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

NOTES:

REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STB<23:16>:** DMA Secondary Start Address bits (source or destination)

REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **STB<15:0>:** DMA Secondary Start Address bits (source or destination)

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	**1, 2**
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	**1**
Low-Power RC Oscillator (LPRC)	Internal	xx	101	**1**
Secondary (Timer1) Oscillator (SOSC)	Secondary	xx	100	**1**
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	**1**
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	**1**
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	**1**
Fast RC Oscillator (FRC)	Internal	xx	000	**1**

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR<5:0>	Output Name
Default Port	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U2TX	000011	RPn tied to UART2 Transmit
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
$\overline{SS2}$	001010	RPn tied to SPI2 Slave Select
CSDO	001011	RPn tied to DCI Data Output
CSCK	001100	RPn tied to DCI Clock Output
COFS	001101	RPn tied to DCI Frame Sync
C1TX	001110	RPn tied to CAN1 Transmit
C2TX	001111	RPn tied to CAN2 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
OC5	010100	RPn tied to Output Compare 5 Output
OC6	010101	RPn tied to Output Compare 6 Output
OC7	010110	RPn tied to Output Compare 7 Output
OC8	010111	RPn tied to Output Compare 8 Output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
U3TX	011011	RPn tied to UART3 Transmit
$\overline{U3RTS}$	011100	RPn tied to UART3 Ready-to-Send
U4TX	011101	RPn tied to UART4 Transmit
$\overline{U4RTS}$	011110	RPn tied to UART4 Ready-to-Send
SDO3	011111	RPn tied to SPI3 Slave Output
SCK3	100000	RPn tied to SPI3 Clock Output
$\overline{SS3}$	100001	RPn tied to SPI3 Slave Select
SYNCO1	101101	RPn tied to PWM Primary Time Base Sync Output
SYNCO2	101110	RPn tied to PWM Secondary Time Base Sync Output
QEI1CCMP	101111	RPn tied to QEI1 Counter Comparator Output
QEI2CCMP	110000	RPn tied to QEI2 Counter Comparator Output
REFCLKO	110001	RPn tied to Reference Clock Output
C4OUT	110010	RPn tied to Comparator Output 4
C5OUT	110011	RPn tied to Comparator Output 5

REGISTER 11-18: RPINR24: PERIPHERAL PIN SELECT INPUT REGISTER 24

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CSCK2R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CSDIR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **CSCK2R<6:0>:** Assign DCI Clock Input (CSCK) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **CSDIR<6:0>:** Assign DCI Data Input (CSDI) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-40: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP118R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP113R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP118R<5:0>:** Peripheral Output Function is Assigned to RP118 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP113R<5:0>:** Peripheral Output Function is Assigned to RP113 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is not available on dsPIC33EPXXXGM30X/604/706 devices.

REGISTER 11-41: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP125R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP120R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP125R<5:0>:** Peripheral Output Function is Assigned to RP125 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP120R<5:0>:** Peripheral Output Function is Assigned to RP120 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is not available on dsPIC33EPXXXGM30X/604/706 devices.

17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33/PIC24 Family Reference Manual*", **"Quadrature Encoder Interface (QEI)"** (DS70601) which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

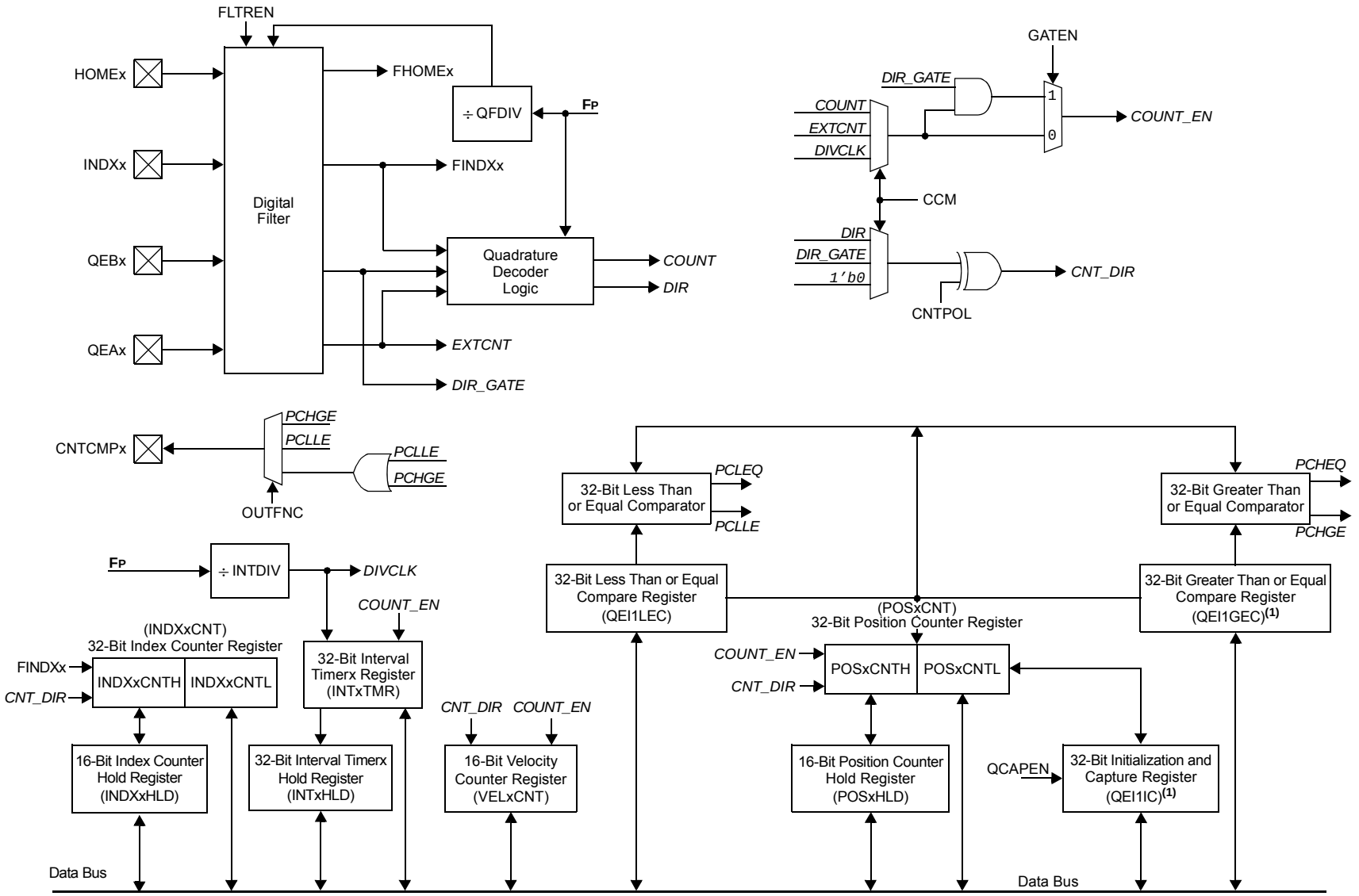
This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High Register
- 32-Bit Position Compare Low Register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEIx block diagram.

FIGURE 17-1: QEIx BLOCK DIAGRAM



Note 1: These registers map to the same memory location.

17.1 QEI Control Registers

REGISTER 17-1: QEIxCON: QEIx CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIEN	—	QEISIDL	PIMOD2(1)	PIMOD1(1)	PIMOD0(1)	IMV1(2,4)	IMV0(2,4)
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INTDIV2(3)	INTDIV1(3)	INTDIV0(3)	CNTPOL	GATEN	CCM1	CCM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **QEIEN:** QEIx Module Counter Enable bit
1 = Module counters are enabled
0 = Module counters are disabled, but SFRs can be read or written to

bit 14 **Unimplemented:** Read as '0'

bit 13 **QEISIDL:** QEIx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **PIMOD<2:0>:** Position Counter Initialization Mode Select bits(1)
111 = Reserved
110 = Modulo Count mode for position counter
101 = Resets the position counter when the position counter equals the QEIxGEC register
100 = Second index event after home event initializes the position counter with contents of the QEIxIC register
011 = First index event after home event initializes the position counter with contents of the QEIxIC register
010 = Next index input event initializes the position counter with contents of the QEIxIC register
001 = Every index input event resets the position counter
000 = Index input event does not affect position counter

bit 9-8 **IMV<1:0>:** Index Match Value bits(2,4)
1 = Required state of Phase B input signal for match on index pulse
0 = Required state of Phase A input signal for match on index pulse

bit 7 **Unimplemented:** Read as '0'

Note 1: When CCM<1:0> = 10 or CCM<1:0> = 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.

2: When CCM<1:0> = 00, and QEAx and QEBx values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset.

3: The selected clock rate should be at least twice the expected maximum quadrature count rate.

4: The match value applies to the A and B inputs after the swap and polarity bits have been applied.

21.4 CAN Message Buffers

CAN Message Buffers are part of RAM memory. They are not CAN Special Function Registers. The user application must directly write into the RAM area that is configured for CAN Message Buffers. The location and size of the buffer area is defined by the user application.

BUFFER 21-1: CANx MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-2 **SID<10:0>:** Standard Identifier bits

bit 1 **SRR:** Substitute Remote Request bit

When IDE = 0:
1 = Message will request remote transmission
0 = Normal message

When IDE = 1:
The SRR bit must be set to '1'.

bit 0 **IDE:** Extended Identifier bit

1 = Message will transmit an Extended Identifier
0 = Message will transmit a Standard Identifier

BUFFER 21-2: CANx MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	EID<17:14>			
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<13:6>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **EID<17:6>:** Extended Identifier bits

27.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Real-Time Clock and Calendar (RTCC)"** (DS70584), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This chapter discusses the Real-Time Clock and Calendar (RTCC) module and its operation.

Some of the key features of this module are:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (military time)
- Calendar: Weekday, Date, Month and Year
- Alarm Configurable
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Compact Firmware
- Optimized for Low-Power Operation
- User Calibration with Auto-Adjust
- Calibration Range: ±2.64 Seconds Error per Month
- Requirements: External 32.768 kHz Clock Crystal
- Alarm Pulse or Seconds Clock Output on RTCC Pin

The RTCC module is intended for applications where accurate time must be maintained for extended periods with minimum to no intervention from the CPU. The RTCC module is optimized for low-power usage to provide extended battery lifetime while keeping track of time.

The RTCC module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

The hours are available in 24-hour (military time) format. The clock provides a granularity of one second with half-second visibility to the user.

29.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33/PIC24 Family Reference Manual*", **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS70346), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-Programmable (up to 32nd order) polynomial CRC equation
- Interrupt Output
- Data FIFO

The programmable CRC generator provides a hardware-implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 29-1. A simple version of the CRC shift engine is shown in Figure 29-2.

FIGURE 29-1: CRC BLOCK DIAGRAM

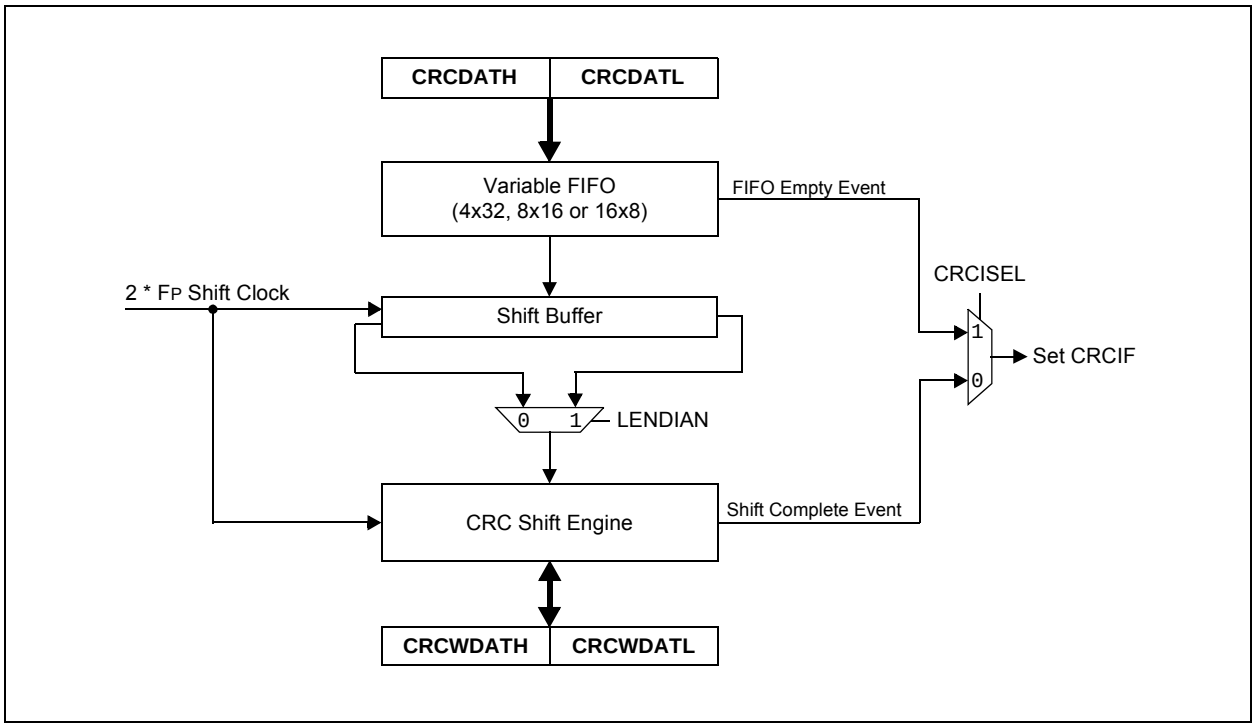


TABLE 33-9: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	**Typ.(2)**	**Max.**	**Doze Ratio**	**Units**	**Conditions**		
Doze Current (IDOZE)(1)							
DC73a	20	53	1:2	mA	-40°C	3.3V	70 MIPS
DC73g	8	30	1:128	mA			
DC70a	19	53	1:2	mA	+25°C	3.3V	60 MIPS
DC70g	8	30	1:128	mA			
DC71a	20	53	1:2	mA	+85°C	3.3V	60 MIPS
DC71g	10	30	1:128	mA			
DC72a	25	42	1:2	mA	+125°C	3.3V	50 MIPS
DC72g	12	30	1:128	mA			

Note 1: IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing

```
while(1)
{
NOP();
}
```

- JTAG is disabled

2: Data in the “Typical” column is at 3.3V, +25°C unless otherwise specified.

FIGURE 33-30: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

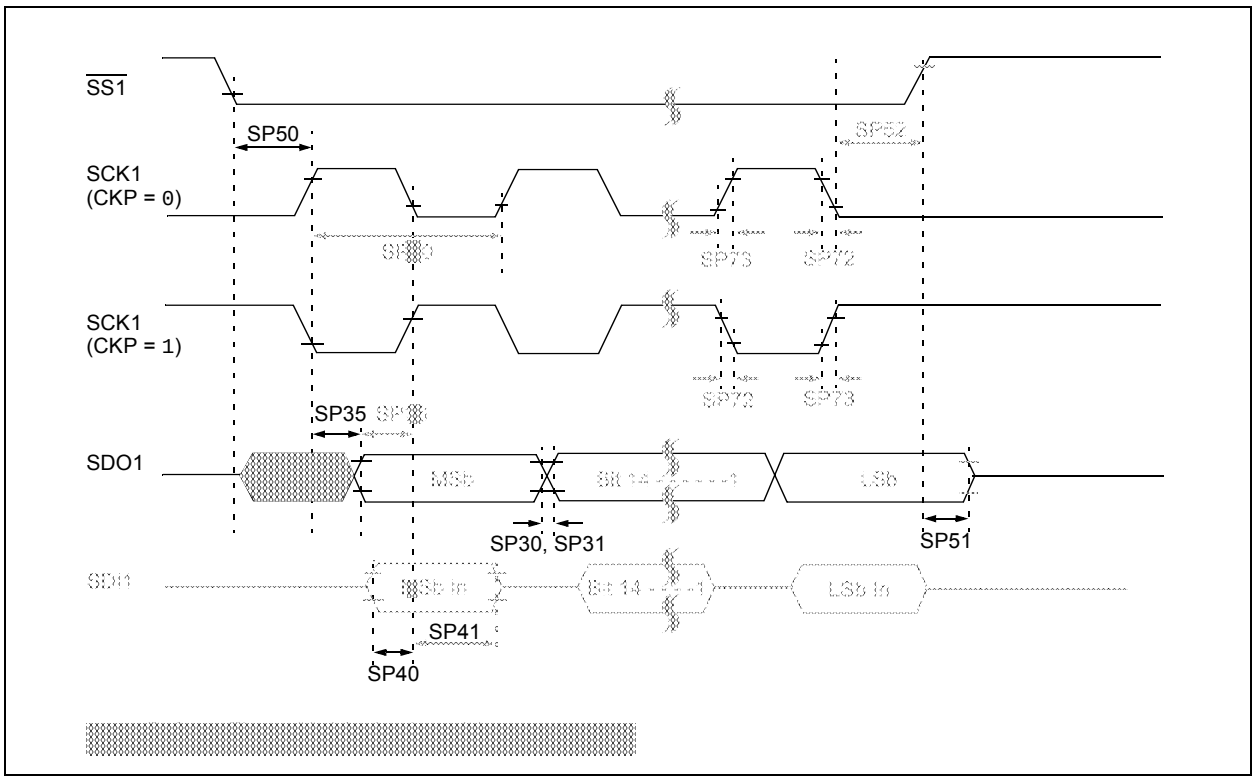


TABLE 33-47: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	**(Note 3)**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 33-58: ADCx MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)(1) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
ADC Accuracy (10-Bit Mode)							
AD20b	Nr	Resolution	10 Data Bits			bits	
AD21b	INL	Integral Nonlinearity	-0.625	—	0.625	LSb	-40°C ≤ TA ≤ +85°C **(Note 2)**
			-1.5	—	1.5	LSb	+85°C < TA ≤ +125°C **(Note 2)**
AD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	-40°C ≤ TA ≤ +85°C **(Note 2)**
			-0.25	—	0.25	LSb	+85°C < TA ≤ +125°C **(Note 2)**
AD23b	GERR	Gain Error	-2.5	—	2.5	LSb	-40°C ≤ TA ≤ +85°C **(Note 2)**
			-2.5	—	2.5	LSb	+85°C < TA ≤ +125°C **(Note 2)**
AD24b	EOFF	Offset Error	-1.25	—	1.25	LSb	-40°C ≤ TA ≤ +85°C **(Note 2)**
			-1.25	—	1.25	LSb	+85°C < TA ≤ +125°C **(Note 2)**
AD25b	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance (10-Bit Mode)							
AD30b	THD	Total Harmonic Distortion(3)	—	64	—	dB	
AD31b	SINAD	Signal to Noise and Distortion(3)	—	57	—	dB	
AD32b	SFDR	Spurious Free Dynamic Range(3)	—	72	—	dB	
AD33b	FNYQ	Input Signal Bandwidth(3)	—	550	—	kHz	
AD34b	ENOB	Effective Number of Bits(3)	—	9.4	—	bits	

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, may have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.

TABLE 33-60: ADCx CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(4)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADCx Clock Period	75	—	—	ns	
AD51	tRC	ADCx Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	12 TAD	—	—	
AD56	FCNV	Throughput Rate	—	—	1.1	Msps	Using simultaneous sampling
AD57a	TSAMP	Sample Time When Sampling Any ANx Input	2 TAD	—	—	—	
AD57b	TSAMP	Sample Time When Sampling the Op Amp Outputs	4 TAD	—	—	—	
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger(2)	2 TAD	—	3 TAD	—	Auto-convert trigger not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit(2)	2 TAD	—	3 TAD	—	
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1)(2)	—	0.5 TAD	—	—	
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On(2)	—	—	20	μs	**(Note 3)**

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

3: The parameter, tDPU, is the time required for the ADCx module to stabilize at the appropriate level when the module is turned on (AD1CON1<ADON> = 1). During this time, the ADCx result is indeterminate.

4: These parameters are characterized, but not tested in manufacturing.