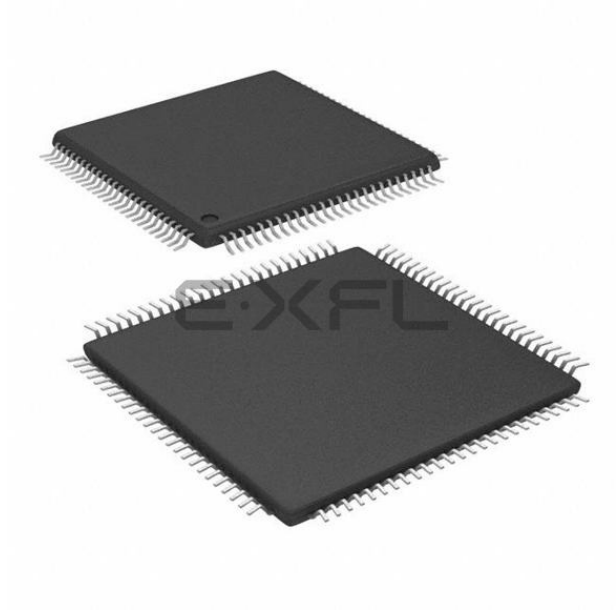
Microchip Technology - DSPIC33EP128GM310-I/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm310-i-pt

3.6 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA(3)	SB(3)	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0(2)	R/W-0(2)	R/W-0(2)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(1)	IPL1(1)	IPL0(1)	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OA:** Accumulator A Overflow Status bit
1 = Accumulator A has overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit
1 = Accumulator B has overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit(3)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit(3)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit
1 = Accumulator A or B has overflowed
0 = Neither Accumulator A or B has overflowed

bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit
1 = Accumulator A or B is saturated or has been saturated at some time
0 = Neither Accumulator A or B is saturated

bit 9 **DA:** DO Loop Active bit
1 = DO loop in progress
0 = DO loop not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

Note 1: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

2: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

3: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

TABLE 4-34: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGM3XX DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—	INT1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>							0000
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>							0000
RPINR7	06AE	—	IC2R<6:0>							—	IC1R<6:0>							0000
RPINR8	06B0	—	IC4R<6:0>							—	IC3R<6:0>							0000
RPINR9	06B2	—	IC6R<6:0>							—	IC5R<6:0>							0000
RPINR10	06B4	—	IC8R<6:0>							—	IC7R<6:0>							0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>							0000
RPINR12	06B8	—	FLT2R<6:0>							—	FLT1R<6:0>							0000
RPINR14	06BC	—	QEB1R<6:0>							—	QEA1R<6:0>							0000
RPINR15	06BE	—	HOME1R<6:0>							—	INDX1R<6:0>							0000
RPINR16	06C0	—	QEB2R<6:0>							—	QEA2R<6:0>							0000
RPINR17	06C2	—	HOME2R<6:0>							—	INDX2R<6:0>							0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>							0000
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>							0000
RPINR22	06CC	—	SCK2R<6:0>							—	SDI2R<6:0>							0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>							0000
RPINR24	06D0	—	CSCKR<6:0>							—	CSDIR<6:0>							0000
RPINR25	06D2	—	—	—	—	—	—	—	—	—	COFSR<6:0>							0000
RPINR27	06D6	—	U3CTSR<6:0>							—	U3RXR<6:0>							0000
RPINR28	06D8	—	U4CTSR<6:0>							—	U4RXR<6:0>							0000
RPINR29	06DA	—	SCK3R<6:0>							—	SDI3R<6:0>							0000
RPINR30	06DC	—	—	—	—	—	—	—	—	—	SS3R<6:0>							0000
RPINR37	06EA	—	SYNCI1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR38	06EC	—	DTCMP1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR39	06EE	—	DTCMP3R<6:0>							—	DTCMP2R<6:0>							0000
RPINR40	06F0	—	DTCMP5R<6:0>							—	DTCMP4R<6:0>							0000
RPINR41	06F2	—	—	—	—	—	—	—	—	—	DTCMP6R<6:0>							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STB<23:16>:** DMA Secondary Start Address bits (source or destination)

REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **STB<15:0>:** DMA Secondary Start Address bits (source or destination)

9.1 CPU Clocking System

The dsPIC33EPXXXGM3XX/6XX/7XX family of devices provides seven system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator
- Secondary (LP) Oscillator

Instruction execution speed or device operating frequency, FCY, is given by Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

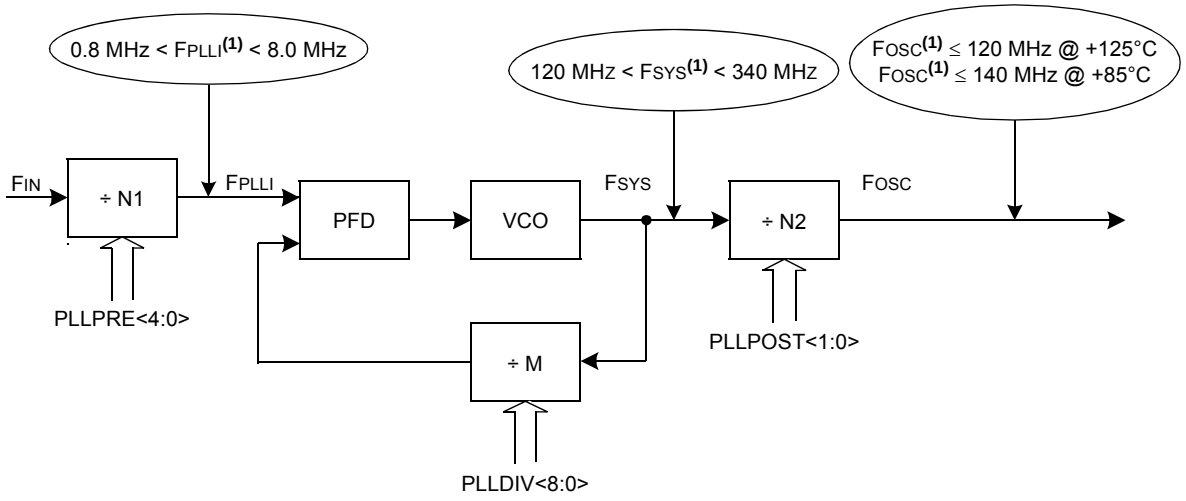
$$FCY = FOSC/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (FIN) and output frequency (FOSC).

Equation 9-3 provides the relationship between input frequency (FIN) and VCO frequency (FSYS).

FIGURE 9-2: PLL BLOCK DIAGRAM



Note 1: This frequency range must be met at all times.

EQUATION 9-2: FOSC CALCULATION

$$FOSC = FIN \times \left(\frac{M}{N1 \times N2}\right) = FIN \times \left(\frac{(PLLDIV<8:0> + 2)}{(PLLPRE<4:0> + 2) \times 2(PLLPOST<1:0> + 1)}\right)$$

Where:

$N1 = PLLPRE<4:0> + 2$

$N2 = 2 \times (PLLPOST<1:0> + 1)$

$M = PLLDIV<8:0> + 2$

EQUATION 9-3: FVCO CALCULATION

$$FSYS = FIN \times \left(\frac{M}{N1}\right) = FIN \times \left(\frac{(PLLDIV<8:0> + 2)}{(PLLPRE<4:0> + 2)}\right)$$

REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	U4MD	—	REFOMD	CTMUMD	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5 **U4MD:** UART4 Module Disable bit
1 = UART4 module is disabled
0 = UART4 module is enabled

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **REFOMD:** Reference Clock Module Disable bit
1 = Reference clock module is disabled
0 = Reference clock module is enabled

bit 2 **CTMUMD:** CTMU Module Disable bit
1 = CTMU module is disabled
0 = CTMU module is enabled

bit 1-0 **Unimplemented:** Read as ‘0’

REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	PWM6MD	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SPI3MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **PWM6MD:PWM1MD:** PWMx (x = 1-6) Module Disable bit
1 = PWMx module is disabled
0 = PWMx module is enabled

bit 7-1 **Unimplemented:** Read as ‘0’

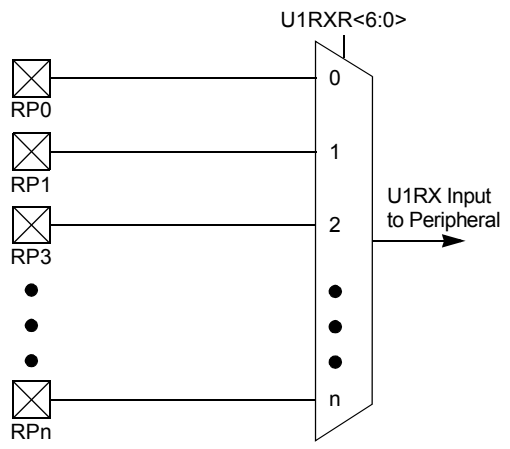
bit 0 **SPI3MD:** SPI3 Module Disable bit
1 = SPI3 module is disabled
0 = SPI3 module is enabled

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-29). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



Note: For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

11.4.4.1 Virtual Connections

dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 26-1 in **Section 26.0 "Op Amp/Comparator Module"**) and the PTG module (see **Section 25.0 "Peripheral Trigger Generator (PTG) Module"**).

In addition, dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual connections to the filtered QEIx module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 "Quadrature Encoder Interface (QEI) Module"**).

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of 'b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEIx module allows peripherals to be connected to the QEIx digital filter input. To utilize this filter, the QEIx module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEIx digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43

```
RPINR15 = 0x2500;      /* Connect the QEI1 HOME1 input to RP37 (pin 43) */
RPINR7 = 0x009;        /* Connect the IC1 input to the digital filter on the FHOME1 input */

QEI1IOC = 0x4000;      /* Enable the QEI digital filter */
QEI1CON = 0x8000;      /* Enable the QEI module */
```

TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name(1)	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<6:0>
External Interrupt 2	INT2	RPINR1	INT2R<6:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<6:0>
Input Capture 1	IC1	RPINR7	IC1R<6:0>
Input Capture 2	IC2	RPINR7	IC2R<6:0>
Input Capture 3	IC3	RPINR8	IC3R<6:0>
Input Capture 4	IC4	RPINR8	IC4R<6:0>
Input Capture 5	IC5	RPINR9	IC5R<6:0>
Input Capture 6	IC6	RPINR9	IC6R<6:0>
Input Capture 7	IC7	RPINR10	IC7R<6:0>
Input Capture 8	IC8	RPINR10	IC8R<6:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<6:0>
PWM Fault 1	FLT1	RPINR12	FLT1R<6:0>
PWM Fault 2	FLT2	RPINR12	FLT2R<6:0>
QEI1 Phase A	QEA1	RPINR14	QEA1R<6:0>
QEI1 Phase B	QEB1	RPINR14	QEB1R<6:0>
QEI1 Index	INDX1	RPINR 15	INDX1R<6:0>
QEI1 Home	HOME1	RPINR15	HOM1R<6:0>
QEI2 Phase A	QEA2	RPINR16	QEA2R<6:0>
QEI2 Phase B	QEB2	RPINR16	QEB2R<6:0>
QEI2 Index	INDX2	RPINR17	INDX2R<6:0>
QEI2 Home	HOME2	RPINR17	HOM2R<6:0>
UART1 Receive	U1RX	RPINR18	U1RXR<6:0>
UART2 Receive	U2RX	RPINR19	U2RXR<6:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<6:0>
SPI2 Clock Input	SCK2	RPINR22	SCK2R<6:0>
SPI2 Slave Select	$\overline{SS2}$	RPINR23	SS2R<6:0>
DCI Data Input	CSDI	RPINR24	CSDIR>6:0>
DCI Clock Input	CSCK	RPINR24	CSCKR<6:0>
DCI Frame Synchronization Input	COFS	RPINR25	COFSR<6:0>
CAN1 Receive(2)	C1RX	RPINR26	C1RXR<6:0>
CAN2 Receive(2)	C2RX	RPINR26	C2RXR<6:0>
UART3 Receive	U3RX	RPINR27	U3RXR<6:0>
UART3 Clear-to-Send	$\overline{U3CTS}$	RPINR27	U3CTSR<6:0>
UART4 Receive	U4RX	RPINR28	U4RXR<6:0>
UART4 Clear-to-Send	$\overline{U4CTS}$	RPINR28	U4CTSR<6:0>
SPI3 Data Input	SDI3	RPINR29	SDI3R<6:0>
SPI3 Clock Input	SCK3	RPINR29	SCK3R<6:0>
SPI3 Slave Select	$\overline{SS3}$	RPINR 30	SS3R<6:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input is available on dsPIC33EPXXXGM6XX/7XX devices only.

REGISTER 11-14: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	U1RXR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-0 **U1RXR<6:0>:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-15: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	U2RXR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-0 **U2RXR<6:0>:** Assign UART2 Receive (U2RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

12.1 Timer1 Control Register

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS1	—	TSYNC(1)	TCS(1)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer1 On bit(1)
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit(1)
When TCS = 1:
1 = Synchronizes external clock input
0 = Does not synchronize external clock input
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit(1)
1 = External clock is from pin, T1CK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.

REGISTER 17-2: QEIxIOC: QEIx I/O CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R-x	R-x	R-x	R-x
HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **QCAPEN:** QEIx Position Counter Input Capture Enable bit
1 = Index match event of home input triggers a position capture event
0 = Index match event (positive edge) does not trigger a position capture event

bit 14 **FLTREN:** QEAx/QEBx/INDXx/HOMEx Digital Filter Enable bit
1 = Input pin digital filter is enabled
0 = Input pin digital filter is disabled (bypassed)

bit 13-11 **QFDIV<2:0>:** QEAx/QEBx/INDXx/HOMEx Digital Input Filter Clock Divide Select bits
111 = 1:128 clock divide
110 = 1:64 clock divide
101 = 1:32 clock divide
100 = 1:16 clock divide
011 = 1:8 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide

bit 10-9 **OUTFNC<1:0>:** QEIx Module Output Function Mode Select bits
11 = The CNTCMPx pin goes high when QEIxLEC ≥ POSxCNT ≥ QEIxGEC
10 = The CNTCMPx pin goes high when POSxCNT ≤ QEIxLEC
01 = The CNTCMPx pin goes high when POSxCNT ≥ QEIxGEC
00 = Output is disabled

bit 8 **SWPAB:** Swap QEAx and QEBx Inputs bit
1 = QEAx and QEBx are swapped prior to quadrature decoder logic
0 = QEAx and QEBx are not swapped

bit 7 **HOMPOL:** HOMEx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 6 **IDXPOL:** INDXx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 5 **QEBPOL:** QEBx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 4 **QEAPOL:** QEAx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 3 **HOME:** Status of HOMEx Input Pin After Polarity Control bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2 **SPRE<2:0>:** Secondary Prescale bits (Master mode)(3)
111 = Secondary prescale 1:1
110 = Secondary prescale 2:1
•
•
•
000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)(3)
11 = Primary prescale 1:1
10 = Primary prescale 4:1
01 = Primary prescale 16:1
00 = Primary prescale 64:1

Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
2: This bit must be cleared when FRMEN = 1.
3: Do not set both primary and secondary prescalers to the value of 1:1.

REGISTER 21-19: CxFMSKSEL2: CANx FILTERS 15-8 MASK SELECTION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15MSK1	F15MSK0	F14MSK1	F14MSK0	F13MSK1	F13MSK0	F12MSK1	F12MSK0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11MSK1	F11MSK0	F10MSK1	F10MSK0	F9MSK1	F9MSK0	F8MSK1	F8MSK0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **F15MSK<1:0>:** Mask Source for Filter 15 bit
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F14MSK<1:0>:** Mask Source for Filter 14 bit (same values as bits 15-14)

bit 11-10 **F13MSK<1:0>:** Mask Source for Filter 13 bit (same values as bits 15-14)

bit 9-8 **F12MSK<1:0>:** Mask Source for Filter 12 bit (same values as bits 15-14)

bit 7-6 **F11MSK<1:0>:** Mask Source for Filter 11 bit (same values as bits 15-14)

bit 5-4 **F10MSK<1:0>:** Mask Source for Filter 10 bit (same values as bits 15-14)

bit 3-2 **F9MSK<1:0>:** Mask Source for Filter 9 bit (same values as bits 15-14)

bit 1-0 **F8MSK<1:0>:** Mask Source for Filter 8 bit (same values as bits 15-14)

23.3 ADCx Control Registers

REGISTER 23-1: ADxCON1: ADCx CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC, HS	R/C-0, HC, HS
SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE(2)
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HS = Hardware Settable bit	HC = Hardware Clearable bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADON:** ADCx Operating Mode bit
1 = ADCx module is operating
0 = ADCx is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** ADCx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ADDMABM:** ADCx DMA Buffer Build Mode bit
1 = DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer
0 = DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather address to the DMA channel based on the index of the analog input and the size of the DMA buffer

bit 11 **Unimplemented:** Read as '0'

bit 10 **AD12B:** 10-Bit or 12-Bit ADCx Operation Mode bit
1 = 12-bit, 1-channel ADCx operation
0 = 10-bit, 4-channel ADCx operation

bit 9-8 **FORM<1:0>:** Data Output Format bits
For 10-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dd00 0000, where s = .NOT.d<9>)
10 = Fractional (DOUT = dddd dddd dd00 0000)
01 = Signed integer (DOUT = ssss sssd dddd dddd, where s = .NOT.d<9>)
00 = Integer (DOUT = 0000 00dd dddd dddd)
For 12-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dddd 0000, where s = .NOT.d<11>)
10 = Fractional (DOUT = dddd dddd dddd 0000)
01 = Signed integer (DOUT = ssss sddd dddd dddd, where s = .NOT.d<11>)
00 = Integer (DOUT = 0000 dddd dddd dddd)

Note 1: See **Section 25.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.
2: Do not clear the DONE bit in software if ADCx Sample Auto-Start bit is enabled (ASAM = 1).

REGISTER 25-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCTS4	ADCTS3	ADCTS2	ADCTS1	IC4TSS	IC3TSS	IC2TSS	IC1TSS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC4CS	OC3CS	OC2CS	OC1CS	OC4TSS	OC3TSS	OC2TSS	OC1TSS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADCTS4:** Sample Trigger PTGO15 for ADCx bit
1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

bit 14 **ADCTS3:** Sample Trigger PTGO14 for ADCx bit
1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

bit 13 **ADCTS2:** Sample Trigger PTGO13 for ADCx bit
1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

bit 12 **ADCTS1:** Sample Trigger PTGO12 for ADCx bit
1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

bit 11 **IC4TSS:** Trigger/Synchronization Source for IC4 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 10 **IC3TSS:** Trigger/Synchronization Source for IC3 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 9 **IC2TSS:** Trigger/Synchronization Source for IC2 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 8 **IC1TSS:** Trigger/Synchronization Source for IC1 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 7 **OC4CS:** Clock Source for OC4 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 6 **OC3CS:** Clock Source for OC3 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 5 **OC2CS:** Clock Source for OC2 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: This register is only used with the PTGCTRL OPTION = 1111 Step command.

REGISTER 25-4: PTGT0LIM: PTG TIMER0 LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT0LIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGT0LIM<15:0>:** PTG Timer0 Limit Register bits
General purpose Timer0 Limit register (effective only with a PTGT0 Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 25-5: PTGT1LIM: PTG TIMER1 LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGT1LIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGT1LIM<15:0>:** PTG Timer1 Limit Register bits
General purpose Timer1 Limit register (effective only with a PTGT1 Step command).

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

27.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Real-Time Clock and Calendar (RTCC)"** (DS70584), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This chapter discusses the Real-Time Clock and Calendar (RTCC) module and its operation.

Some of the key features of this module are:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (military time)
- Calendar: Weekday, Date, Month and Year
- Alarm Configurable
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Compact Firmware
- Optimized for Low-Power Operation
- User Calibration with Auto-Adjust
- Calibration Range: ±2.64 Seconds Error per Month
- Requirements: External 32.768 kHz Clock Crystal
- Alarm Pulse or Seconds Clock Output on RTCC Pin

The RTCC module is intended for applications where accurate time must be maintained for extended periods with minimum to no intervention from the CPU. The RTCC module is optimized for low-power usage to provide extended battery lifetime while keeping track of time.

The RTCC module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

The hours are available in 24-hour (military time) format. The clock provides a granularity of one second with half-second visibility to the user.

REGISTER 28-2: PMMODE: PARALLEL MASTER PORT MODE REGISTER(4) (CONTINUED)

bit 5-2 **WAITM<3:0>:** Read to Byte Enable Strobe Wait State Configuration bits
1111 = Wait of additional 15 TP
•
•
•
0001 = Wait of additional 1 TP
0000 = No additional Wait cycles (operation forced into one TP)

bit 1-0 **WAITE<1:0>:** Data Hold After Strobe Wait State Configuration bits(1,2,3)
11 = Wait of 4 TP
10 = Wait of 3 TP
01 = Wait of 2 TP
00 = Wait of 1 TP

Note 1: The applied Wait state depends on whether data and address are multiplexed or demultiplexed. See **Section 4.1.8 "Wait States"** in the **"Parallel Master Port (PMP)"** (DS70576) in the *"dsPIC33/PIC24 Family Reference Manual"* for more information.

2: WAITB<1:0> and WAITE<1:0> bits are ignored whenever WAITM<3:0> = 0000.

3: TP = 1/FP.

4: This register is not available on 44-pin devices.

NOTES:

33.2 AC Characteristics and Timing Parameters

This section defines the dsPIC33EPXXXGM3XX/6XX/7XX AC characteristics and timing parameters.

TABLE 33-14: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended Operating voltage VDD range as described in **Section 33.1 "DC Characteristics"**.

FIGURE 33-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

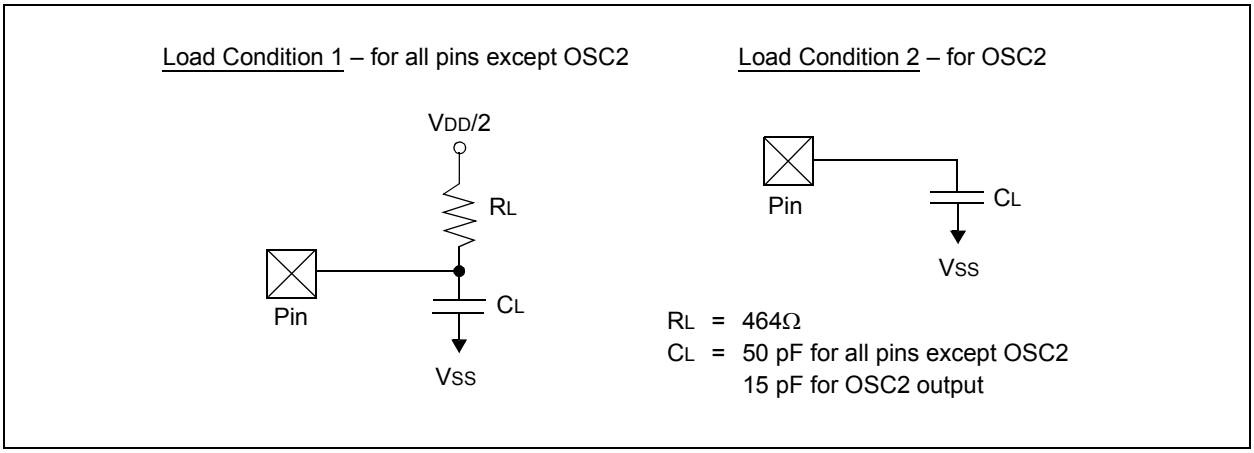


TABLE 33-15: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	COSCO	OSC2 Pin	—	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	CIO	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C™ mode

TABLE 33-46: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	**(Note 3)**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.