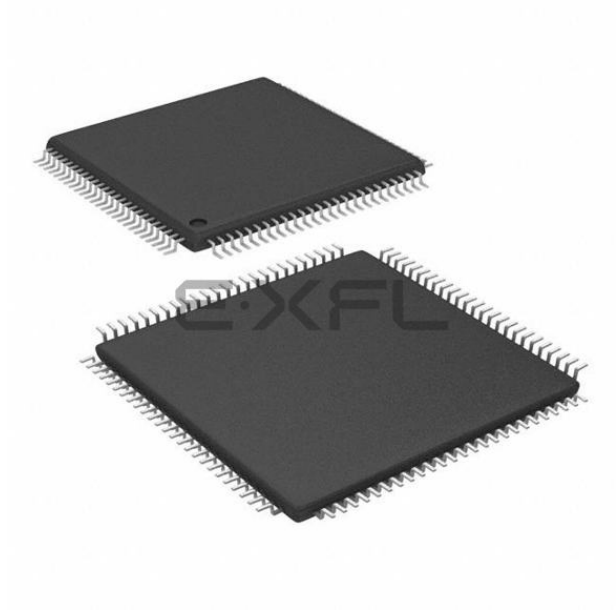
Microchip Technology - DSPIC33EP128GM310T-I/PF Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm310t-i-pf

NOTES:

REGISTER 3-2: CORCON: CORE CONTROL REGISTER(3) (CONTINUED)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **SFA:** Stack Frame Active Status bit
1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1 **RND:** Rounding Mode Select bit
1 = Biased (conventional) rounding is enabled
0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
1 = Integer mode is enabled for DSP multiply
0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is always read as '0'.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.
3: Refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"CPU"** (DS70359) for more detailed information.

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33/PIC24 Family Reference Manual*", **"Program Memory"** (DS70613), which is available from the Microchip web site (www.microchip.com).

The dsPIC33EPXXXGM3XX/6XX/7XX family architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

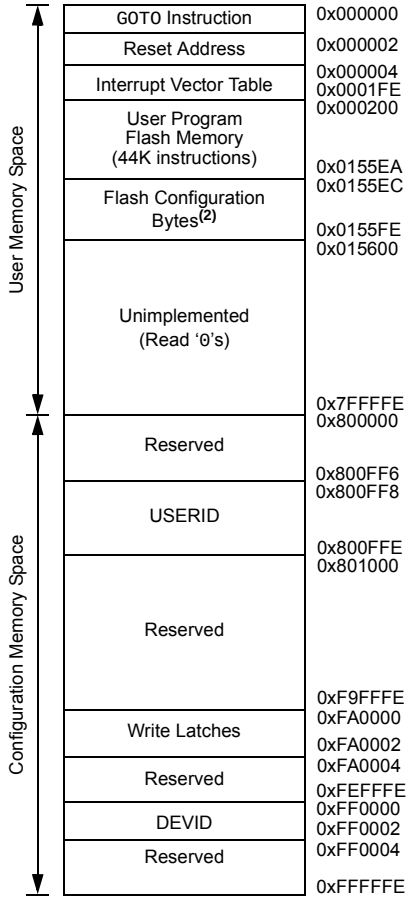
4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGM3XX/6XX/7XX devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in **Section 4.7 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG<7> to read Device ID sections of the configuration memory space.

The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-3.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP128GM3XX/6XX/7XX DEVICES(1)



Note 1: Memory areas are not shown to scale.

2: On Reset, these bits are automatically copied into the device Configuration Shadow registers.

TABLE 4-35: NVM REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0728	WR	WREN	WRERR	NVMSIDL	—	—	RPDF	URERR	—	—	—	—	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000
NVMADR	072A	NVMADR<15:0>																0000
NVMADRU	072C	—	—	—	—	—	—	—	—	NVMADRU<23:16>								0000
NVMKEY	072E	—	—	—	—	—	—	—	—	NVMKEY<7:0>								0000
NVMSRCADRL	0730	NVMSRCADR<15:1>															0	0000
NVMSRCADRH	0732									NVMSRCADRH<23:16>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-36: SYSTEM CONTROL REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	**Note 1**
OSCCON	0742	—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0	CLKLOCK	IOLOCK	LOCK	—	CF	—	LPOSCEN	OSWEN	**Note 2**
CLKDIV	0744	ROI	DOZE2	DOZE1	DOZE0	DOZEN	FRCDIV2	FRCDIV1	FRCDIV0	PLLPOST1	PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0	0030
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>									0030
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: RCON register Reset values are dependent on the type of Reset.
2: OSCCON register Reset values are dependent on the configuration fuses.

TABLE 4-37: REFERENCE CLOCK REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
REFOCON	074E	ROON	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.5.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note:	The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed, but the contents of the register remain unchanged.

4.6 Bit-Reversed Addressing

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms; it is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.6.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when all of these conditions are met:

- BWM bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^N$ bytes, the last 'N' bits of the data buffer start address must be zeros.

XB<14:0> is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:	All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note:	Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

4.7.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

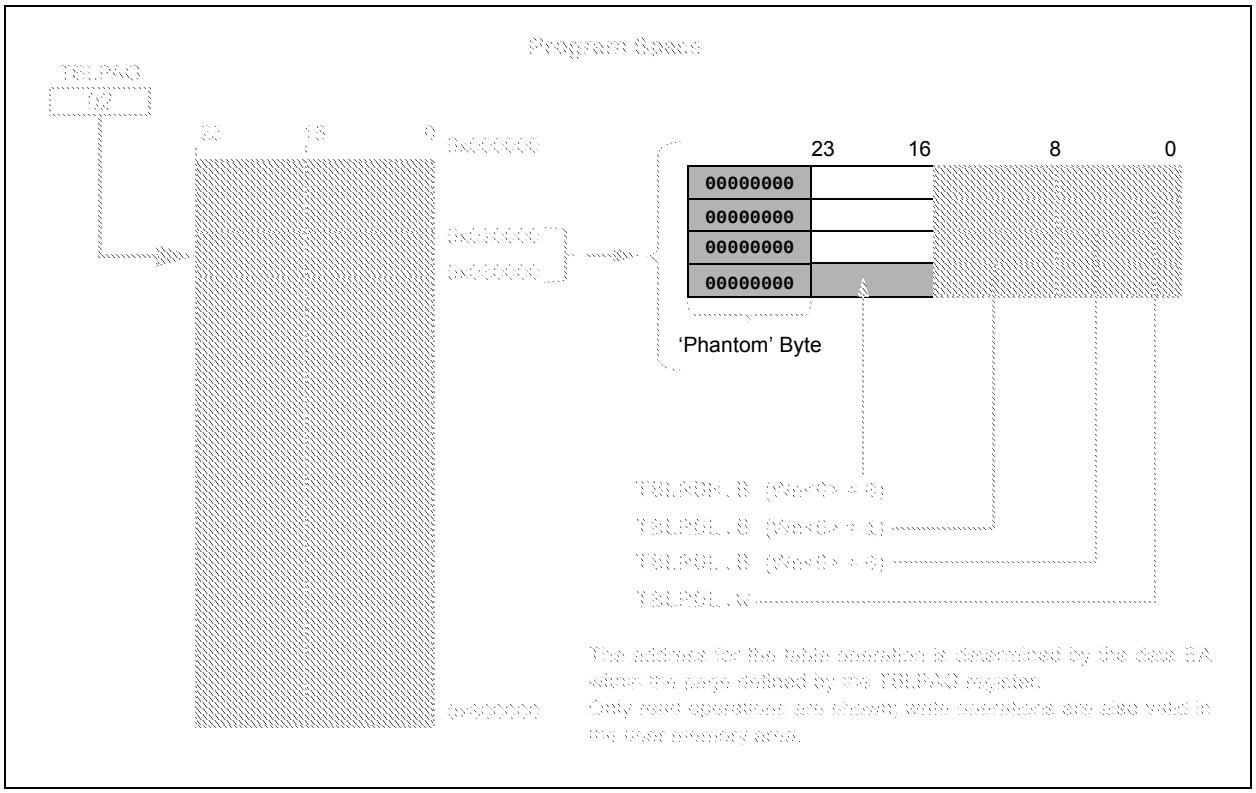
Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
  - In Word mode, this instruction maps the lower word of the Program Space location (P<15:0>) to a data address (D<15:0>)
  - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.
- TBLRDH (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>) is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

FIGURE 4-17: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV3(1)	RODIV2(1)	RODIV1(1)	RODIV0(1)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROON:** Reference Oscillator Output Enable bit
1 = Reference oscillator output is enabled on the REFCLK pin(2)
0 = Reference oscillator output is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit
1 = Reference oscillator output continues to run in Sleep
0 = Reference oscillator output is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Oscillator crystal is used as the reference clock
0 = System clock is used as the reference clock

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits(1)
1111 = Reference clock divided by 32,768
1110 = Reference clock divided by 16,384
1101 = Reference clock divided by 8,192
1100 = Reference clock divided by 4,096
1011 = Reference clock divided by 2,048
1010 = Reference clock divided by 1,024
1001 = Reference clock divided by 512
1000 = Reference clock divided by 256
0111 = Reference clock divided by 128
0110 = Reference clock divided by 64
0101 = Reference clock divided by 32
0100 = Reference clock divided by 16
0011 = Reference clock divided by 8
0010 = Reference clock divided by 4
0001 = Reference clock divided by 2
0000 = Reference clock

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
2: This pin is remappable. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information.

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES (CONTINUED)

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
010 1001	I/O	RP41
010 1010	I/O	RP42
010 1011	I/O	RP43
101 1000	—	—
101 1001	—	—
101 1010	—	—
101 1011	—	—
101 1100	—	—
101 1101	—	—
101 1110	I	RPI94
101 1111	I	RPI95
110 0000	I	RPI96
110 0001	I/O	RP97
110 0010	—	—
110 0011	—	—
110 0100	—	—
110 0101	—	—
110 0110	—	—
110 0111	—	—
110 1000	—	—
110 1001	—	—
110 1010	—	—
110 1011	—	—
101 0101	—	—
101 0110	—	—
101 0111	—	—
110 1100	—	—
110 1101	—	—
110 1110	—	—
110 1111	—	—
111 0000	I	RPI112
111 0001	I/O	RP113
111 0010	—	—
111 0011	—	—
111 0100	—	—
111 0101	—	—
111 0110	I/O	RP118
111 0111	I	RPI119
111 1000	I/O	RP120
111 1001	I	RPI121
111 1010	—	—
111 1011	—	—
111 1100	I	RPI124
111 1101	I/O	RP125
111 1110	I/O	RP126
111 1111	I/O	RP127

Legend: Shaded rows indicate PPS Input register values that are unimplemented.

Note 1: See **Section 11.4.4.1 “Virtual Connections”** for more information on selecting this pin assignment.

REGISTER 11-34: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP43R<5:0>:** Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP42R<5:0>:** Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-35: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP49R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP48R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP49R<5:0>:** Peripheral Output Function is Assigned to RP49 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP48R<5:0>:** Peripheral Output Function is Assigned to RP48 Output Pin bits (see Table 11-3 for peripheral function numbers)

13.0 TIMER2/3, TIMER4/5, TIMER6/7 AND TIMER8/9

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Timers"** (DS70362), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3, Timer4/5, Timer6/7 and Timer8/9 modules are 32-bit timers, which can also be configured as eight independent 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3, Timer4/5, Timer6/7 and Timer8/9 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with All 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare modules
- ADC1 Event Trigger (Timer2/3 only)

Individually, all eight of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON, T5CON, T6CON, T7CON, T8CON and T9CON registers. T2CON, T4CON, T6CON and T8CON are shown in generic form in Register 13-1. T3CON, T5CON, T7CON and T9CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2, Timer4, Timer6 and Timer8 are the least significant word (lsw); Timer3, Timer5, Timer7 and Timer9 are the most significant word (msw) of the 32-bit timers.

Note: For 32-bit operation, T3CON, T5CON, T7CON and T9CON register control bits are ignored. Only T2CON, T4CON, T6CON and T8CON register control bits are used for setup and control. Timer2, Timer4, Timer6 and Timer8 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3, Timer5, Timer7 and Timer9 interrupt flags.

A block diagram for an example of a 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

Note: Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8

R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTMD:** Fault Mode Select bit
- 1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
- 0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit
- 1 = PWM output is driven high on a Fault
- 0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit
- 1 = OCx pin is tri-stated on a Fault condition
- 0 = OCx pin I/O state is defined by the FLTOUT bit on a Fault condition

bit 12 **OCINV:** OCx Invert bit
- 1 = OCx output is inverted
- 0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)
- 1 = Cascade module operation is enabled
- 0 = Cascade module operation is disabled

bit 7 **OCTRIG:** OCx Trigger/Sync Select bit
- 1 = Triggers OCx from source designated by the SYNCSELx bits
- 0 = Synchronizes OCx with source designated by the SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit
- 1 = Timer source has been triggered and is running
- 0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** OCx Output Pin Direction Select bit
- 1 = Output Compare x is tri-stated
- 0 = Output Compare x module drives the OCx pin

Note 1: Do not use the OCx module as its own synchronization or trigger source.

2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

3: Each Output Compare x module (OCx) has one PTG Trigger/Sync source. See **Section 25.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO4 = OC1, OC5
PTGO5 = OC2, OC6
PTGO6 = OC3, OC7
PTGO7 = OC4, OC8

REGISTER 17-3: QEIxSTAT: QEIx STATUS REGISTER

U-0	U-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
bit 15							bit 8

HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
PCIIRQ(1)	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
bit 7							bit 0

Legend:	HS = Hardware Settable bit	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **PCHEQIRQ:** Position Counter Greater Than or Equal Compare Status bit
1 = POSxCNT ≥ QEIxGEC
0 = POSxCNT < QEIxGEC

bit 12 **PCHEQIEN:** Position Counter Greater Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 11 **PCLEQIRQ:** Position Counter Less Than or Equal Compare Status bit
1 = POSxCNT ≤ QEIxLEC
0 = POSxCNT > QEIxLEC

bit 10 **PCLEQIEN:** Position Counter Less Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 9 **POSOVIRQ:** Position Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred

bit 8 **POSOVIEN:** Position Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 7 **PCIIRQ:** Position Counter (Homing) Initialization Process Complete Status bit(1)
1 = POSxCNT was reinitialized
0 = POSxCNT was not reinitialized

bit 6 **PCIIEN:** Position Counter (Homing) Initialization Process Complete interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **VELOVIRQ:** Velocity Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred

bit 4 **VELOVIEN:** Velocity Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **HOMIRQ:** Status Flag for Home Event Status bit
1 = Home event has occurred
0 = No home event has occurred

Note 1: This status bit is only applicable to PIMOD<2:0> = 011 and 100 modes.

REGISTER 21-3: CxVEC: CANx INTERRUPT CODE REGISTER

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0
bit 15							bit 8

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
—	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bits

10000-11111 = Reserved
01111 = Filter 15
•
•
•
00001 = Filter 1
00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits

1000101-1111111 = Reserved
1000100 = FIFO almost full interrupt
1000011 = Receiver overflow interrupt
1000010 = Wake-up interrupt
1000001 = Error interrupt
1000000 = No interrupt
•
•
•
0010000-0111111 = Reserved
0001111 = RB15 buffer interrupt
•
•
•
0001001 = RB9 buffer interrupt
0001000 = RB8 buffer interrupt
0000111 = TRB7 buffer interrupt
0000110 = TRB6 buffer interrupt
0000101 = TRB5 buffer interrupt
0000100 = TRB4 buffer interrupt
0000011 = TRB3 buffer interrupt
0000010 = TRB2 buffer interrupt
0000001 = TRB1 buffer interrupt
0000000 = TRB0 buffer interrupt

REGISTER 21-26: CxTRmnCON: CANx TX/RX BUFFER mn CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm(1)	TXLARBm(1)	TXERRm(1)	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 See Definition for bits 7-0, controls Buffer n

bit 7 **TXENm:** TX/RX Buffer Selection bit
1 = Buffer, TRBn, is a transmit buffer
0 = Buffer, TRBn, is a receive buffer

bit 6 **TXABTm:** Message Aborted bit(1)
1 = Message was aborted
0 = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit(1)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit(1)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit
1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
0 = Clearing the bit to '0' while set requests a message abort

bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
1 = When a remote transmit is received, TXREQx will be set
0 = When a remote transmit is received, TXREQx will be unaffected

bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

Note 1: This bit is cleared when TXREQx is set.

Note: The buffers, SIDx, EIDx, DLCx, Data Field, and Receive Status registers, are located in DMA RAM.

REGISTER 24-5: RSCON: DCI RECEIVE SLOT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **RSE<15:0>:** DCI Receive Slot Enable bits
1 = CSDI data is received during Individual Time Slot n
0 = CSDI data is ignored during Individual Time Slot n

REGISTER 24-6: TSCON: DCI TRANSMIT SLOT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **TSE<15:0>:** DCI Transmit Slot Enable Control bits
1 = Transmit buffer contents are sent during Individual Time Slot n
0 = CSDO pin is tri-stated or driven to logic ‘0’ during the individual time slot, depending on the state of the CSDOM bit

REGISTER 26-7: CVR1CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	—	—	CVRR1	VREFSEL	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE	CVRR0	CVRSS	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **CVRR1:** Comparator Voltage Reference Range Selection bit
See bit 5.

bit 10 **VREFSEL:** Voltage Reference Select bit
1 = $CV_{REFIN} = V_{REF+}$
0 = CV_{REFIN} is generated by the resistor network

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 6 **CVROE:** Comparator Voltage Reference Output Enable on CV_{REF1O} Pin bit
1 = Voltage level is output on the CV_{REF1O} pin
0 = Voltage level is disconnected from the CV_{REF1O} pin

bit 11, 5 **CVRR<1:0>:** Comparator Voltage Reference Range Selection bits
11 = 0.00 CV_{RSRC} to 0.94, with CV_{RSRC}/16 step-size
10 = 0.33 CV_{RSRC} to 0.96, with CV_{RSRC}/24 step-size
01 = 0.00 CV_{RSRC} to 0.67, with CV_{RSRC}/24 step-size
00 = 0.25 CV_{RSRC} to 0.75, with CV_{RSRC}/32 step-size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator voltage reference source, $CV_{RSRC} = CV_{REF+} – AV_{SS}$
0 = Comparator voltage reference source, $CV_{RSRC} = AV_{DD} – AV_{SS}$

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection $0 \le CVR<3:0> \le 15$ bits
When CVRR<1:0> = 11:
$CV_{REF} = (CVR<3:0>/16) \bullet (CV_{RSRC})$
When CVRR<1:0> = 10:
$CV_{REF} = (1/3) \bullet (CV_{RSRC}) + (CVR<3:0>/24) \bullet (CV_{RSRC})$
When CVRR<1:0> = 01:
$CV_{REF} = (CVR<3:0>/24) \bullet (CV_{RSRC})$
When CVRR<1:0> = 00:
$CV_{REF} = (1/4) \bullet (CV_{RSRC}) + (CVR<3:0>/32) \bullet (CV_{RSRC})$

NOTES:

REGISTER 28-4: PMAEN: PARALLEL MASTER PORT ADDRESS ENABLE REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN15	PTEN14	PTEN<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN<7:2>						PTEN<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PTEN15:** PMCS2 Strobe Enable bit
1 = PMA15 functions as either PMA<15> or PMCS2
0 = PMA15 functions as port I/O

bit 14 **PTEN14:** PMCS1 Strobe Enable bit
1 = PMA14 functions as either PMA<14> or PMCS1
0 = PMA14 functions as port I/O

bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
1 = PMA<13:2> function as PMP address lines
0 = PMA<13:2> function as port I/Os

bit 1-0 **PTEN<1:0>:** PMALH/PMALL Strobe Enable bits
1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL
0 = PMA1 and PMA0 function as port I/Os

Note 1: This register is not available on 44-pin devices.

TABLE 33-59: ADCx CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(4)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADCx Clock Period	117.6	—	—	ns	
AD51	tRC	ADCx Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	14 TAD		ns	
AD56	FCNV	Throughput Rate	—	—	500	ksps	
AD57a	TSAMP	Sample Time When Sampling Any ANx Input	3 TAD	—	—	—	
AD57b	TSAMP	Sample Time When Sampling the Op Amp Outputs	3 TAD	—	—	—	
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger(1)	2 TAD	—	3 TAD	—	Auto-convert trigger is not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit(1)	2 TAD	—	3 TAD	—	
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1)(1)	—	0.5 TAD	—	—	
AD63	tDPU	Time to Stabilize Analog Stage from ADCx Off to ADCx On(1)	—	—	20	μs	**(Note 3)**

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

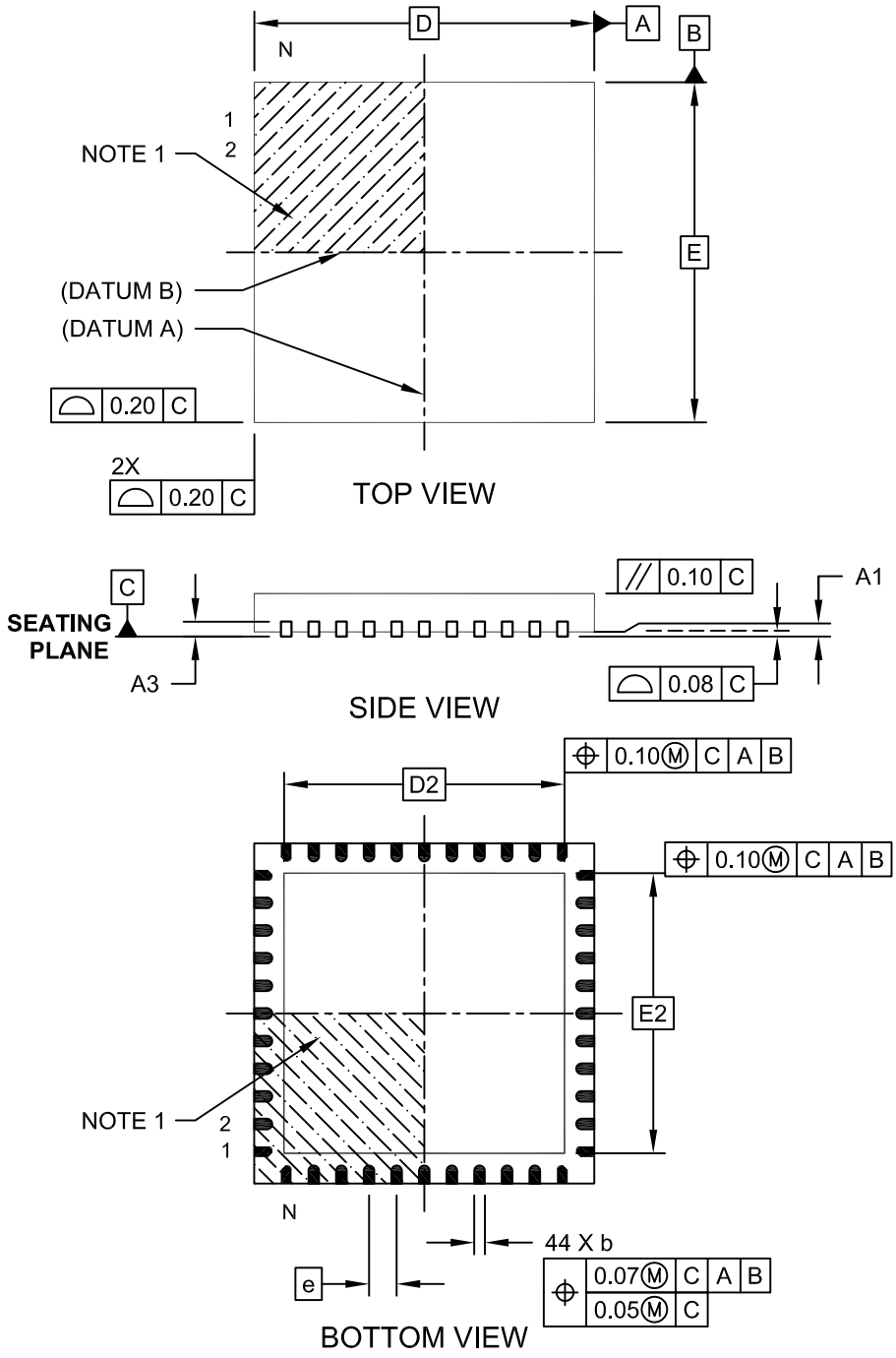
2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

3: The parameter, tDPU, is the time required for the ADCx module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1<15>) = 1). During this time, the ADCx result is indeterminate.

4: These parameters are characterized, but not tested in manufacturing.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-103C Sheet 1 of 2