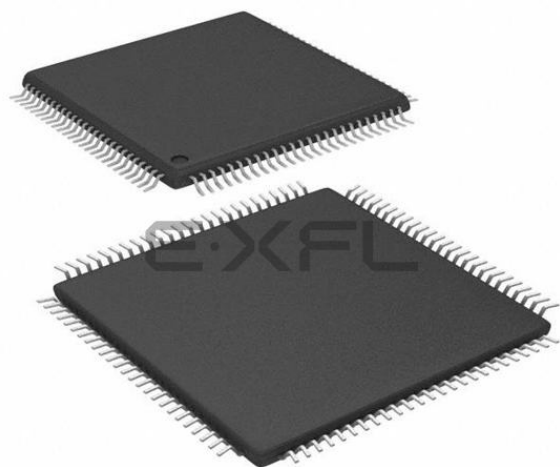




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Details

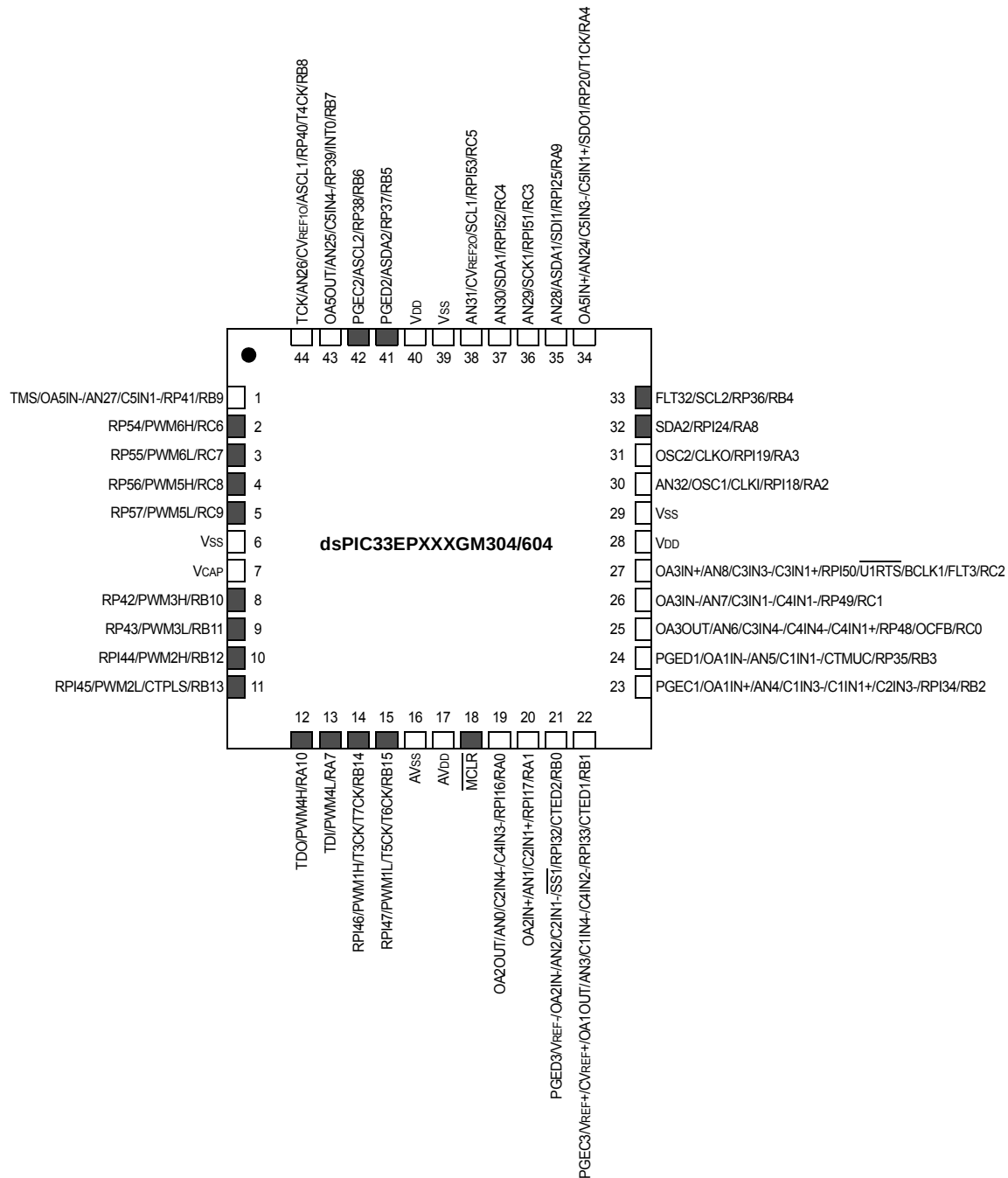
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm310t-i-pt

dsPIC33EPXXXGM3XX/6XX/7XX

Pin Diagrams (Continued)

44-Pin QFN^(1,2,3)

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 2: PIN NAMES: dsPIC33EP128/256/512GM310/710 DEVICES^(1,2,3)

Pin #	Full Pin Name	Pin #	Full Pin Name
A1	TDO/PWM4H/PMD4/RA10	E8	AN47/INT4/RA15
A2	RPI45/PWM2L/CTPLS/PMD3/RB13	E9	RPI72/RD8
A3	RP125/RG13	E10	PGED2/ASDA2/RP37/RB5
A4	RP42/PWM3H/PMD0/RB10	E11	AN46/INT3/RA14
A5	RPI112/RG0	F1	MCLR
A6	RP97/RF1	F2	AN17/ASDA1/RP120/PMA3/RG8
A7	VDD	F3	AN16/RPI121/PMA2/RG9
A8	No Connect	F4	AN18/ASCL1/RPI119/PMA4/RG7
A9	RPI76/RD12	F5	Vss
A10	RP54/RC6	F6	No Connect
A11	TMS/OA5IN-/AN27/C5IN1-/RP41/RB9	F7	No Connect
B1	No Connect	F8	VDD
B2	AN23/RP127/RG15	F9	AN49/OSC1/CLKI/RPI60/RC12
B3	RPI44/PWM2H/PMD2/RB12	F10	Vss
B4	RP43/PWM3L/PMD1/RB11	F11	OSC2/CLKO/RPI63/RC15
B5	RF7	G1	AN21/RE8
B6	RPI96/RF0	G2	AN20/RE9
B7	VCAP	G3	AN22/RG10
B8	RP69/PMRD/RD5	G4	No Connect
B9	RP55/PMBE/RC7	G5	VDD
B10	Vss	G6	Vss
B11	TCK/AN26/CVREF10/SOSCO/RP40/T4CK/RB8	G7	Vss
C1	RPI46/PWM1H/T3CK/T7CK/PMD6/RB14	G8	No Connect
C2	VDD	G9	AN45/RF5
C3	RPI124/RG12	G10	AN43/RG3
C4	RP126/RG14	G11	AN44/RF4
C5	RF6	H1	AN10/RPI28/RA12
C6	No Connect	H2	AN9/RPI27/RA11
C7	RP57/RC9	H3	No Connect
C8	RP56/PMWR/RC8	H4	No Connect
C9	No Connect	H5	No Connect
C10	SOSCI/RPI61/RC13	H6	VDD
C11	AN48/CVREF20/RPI58/PMCS1/RC10	H7	No Connect
D1	PWM5L/RD1	H8	AN28/SDI1/RPI25/RA9
D2	RPI47/PWM1L/T5CK/T6CK/PMD7/RB15	H9	AN29/SCK1/RPI51/RC3
D3	TDI/PWM4L/PMD5/RA7	H10	AN31/SCL1/RPI53/RC5
D4	No Connect	H11	AN42/RG2
D5	No Connect	J1	OA2OUT/AN0/C2IN4-/C4IN3-/RPI16/RA0
D6	No Connect	J2	OA2IN+/AN1/C2IN3-/C2IN1+/RPI17/RA1
D7	RP70/RD6	J3	PGED1/OA1IN-/AN5/C1IN1-/CTMUC/RP35/RTCC/RB3
D8	RPI77/RD13	J4	AVDD
D9	OA5OUT/AN25/C5IN4-/RP39/INT0/RB7	J5	AN11/C1IN2-/U1CTS/FLT4/PMA12/RC11
D10	No Connect	J6	AN35/RG11
D11	PGEC2/ASCL2/RP38/PMCS2/RB6	J7	AN12/C2IN2-/C5IN2-/U2RTS/BCLK2/FLT5/PMA11/RE12

- Note 1:** The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- 3:** The availability of I²C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 30.0 “Special Features”** for more information.

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4.3 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
W0	0000	W0 (WREG)																XXXX	
W1	0002	W1																XXXX	
W2	0004	W2																XXXX	
W3	0006	W3																XXXX	
W4	0008	W4																XXXX	
W5	000A	W5																XXXX	
W6	000C	W6																XXXX	
W7	000E	W7																XXXX	
W8	0010	W8																XXXX	
W9	0012	W9																XXXX	
W10	0014	W10																XXXX	
W11	0016	W11																XXXX	
W12	0018	W12																XXXX	
W13	001A	W13																XXXX	
W14	001C	W14																XXXX	
W15	001E	W15																XXXX	
SPLIM	0020	SPLIM																0000	
ACCAL	0022	ACCAL																0000	
ACCAH	0024	ACCAH																0000	
ACCAU	0026	Sign Extension of ACCA<39>										ACCAU						0000	
ACCBL	0028	ACCBL																0000	
ACCBH	002A	ACCBH																0000	
ACCBU	002C	Sign Extension of ACCB<39>										ACCBU						0000	
PCL	002E	Program Counter Low Word Register																—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	Program Counter High Word Register						0000		
DSRPAG	0032	—	—	—	—	—	—	Data Space Read Page Register										0001	
DSWPAG	0034	—	—	—	—	—	—	—	Data Space Write Page Register										0001
RCOUNT	0036	REPEAT Loop Count Register																0000	
DCOUNT	0038	DCOUNT<15:0>																0000	
DOSTARTL	003A	DOSTARTL<15:1>																—	0000
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>					0000		
DOENDL	003E	DOENDL<15:1>																—	0000
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH<5:0>					0000		

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER⁽²⁾ (CONTINUED)

bit 4-0 **PLLPRE<4:0>**: PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)
11111 = Input divided by 33
•
•
•
00001 = Input divided by 3
00000 = Input divided by 2 (default)

- Note 1:** This bit is cleared when the ROI bit is set and an interrupt occurs.
- 2:** This register resets only on a Power-on Reset (POR).
- 3:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
- 4:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

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REGISTER 11-19: RPINR25: PERIPHERAL PIN SELECT INPUT REGISTER 25

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COFSR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-7
- Unimplemented:** Read as '0'
- bit 6-0
- COFSR<6:0>:** Assign DCI Frame Sync Input (COFS) to the Corresponding RPN Pin bits (see Table 11-2 for input pin selection numbers)
- 1111100 = Input tied to RPI124
- -
 -
- 0000001 = Input tied to CMP1
- 0000000 = Input tied to Vss

REGISTER 11-28: RPINR40: PERIPHERAL PIN SELECT INPUT REGISTER 40

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP5R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP4R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP5R<6:0>**: Assign PWM Dead-Time Compensation Input 5 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•

•

•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DTCMP4R<6:0>**: Assign PWM Dead-Time Compensation Input 4 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•

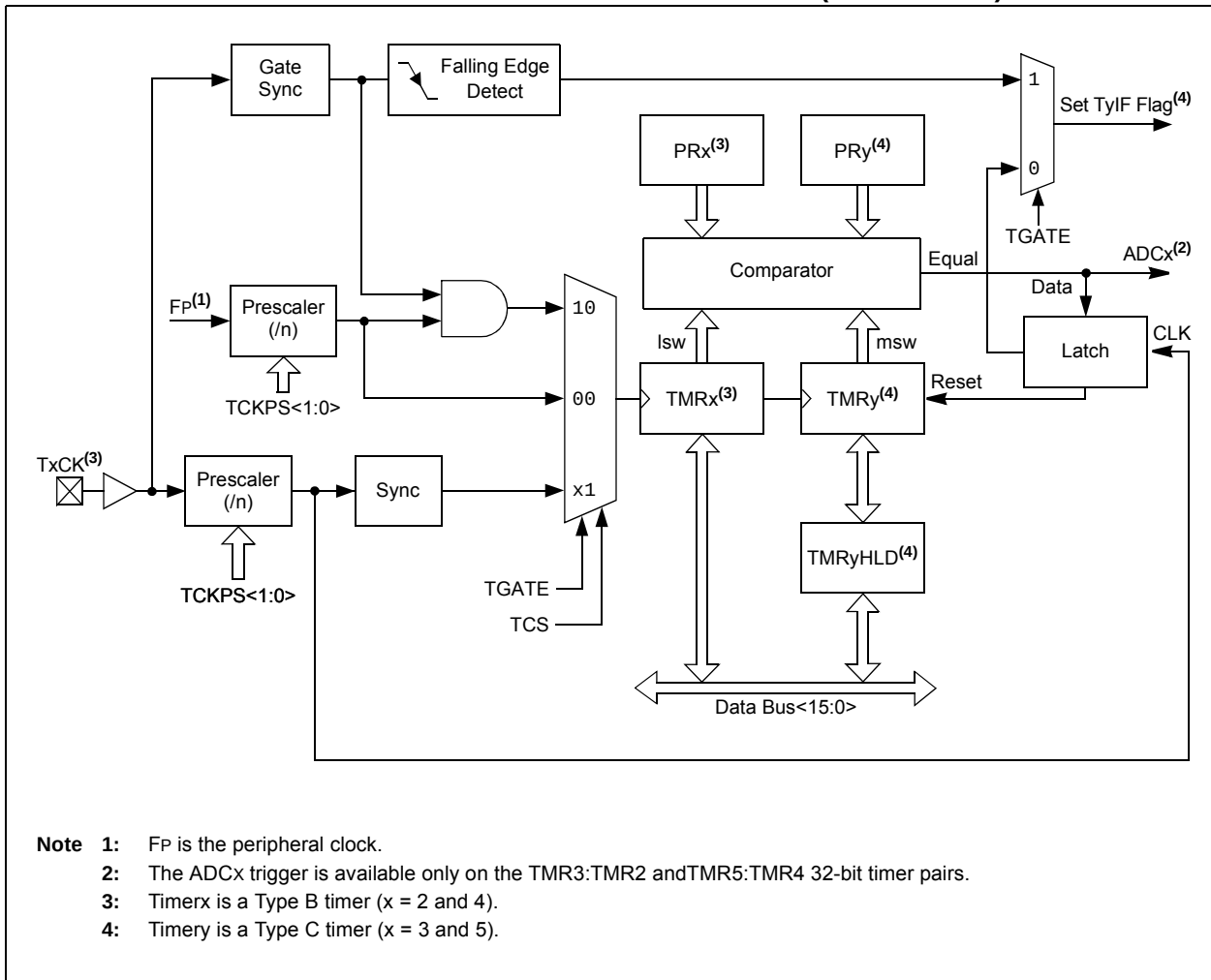
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0000001 = Input tied to CMP1

0000000 = Input tied to Vss

FIGURE 13-3: TYPE B/TIME C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)



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REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8

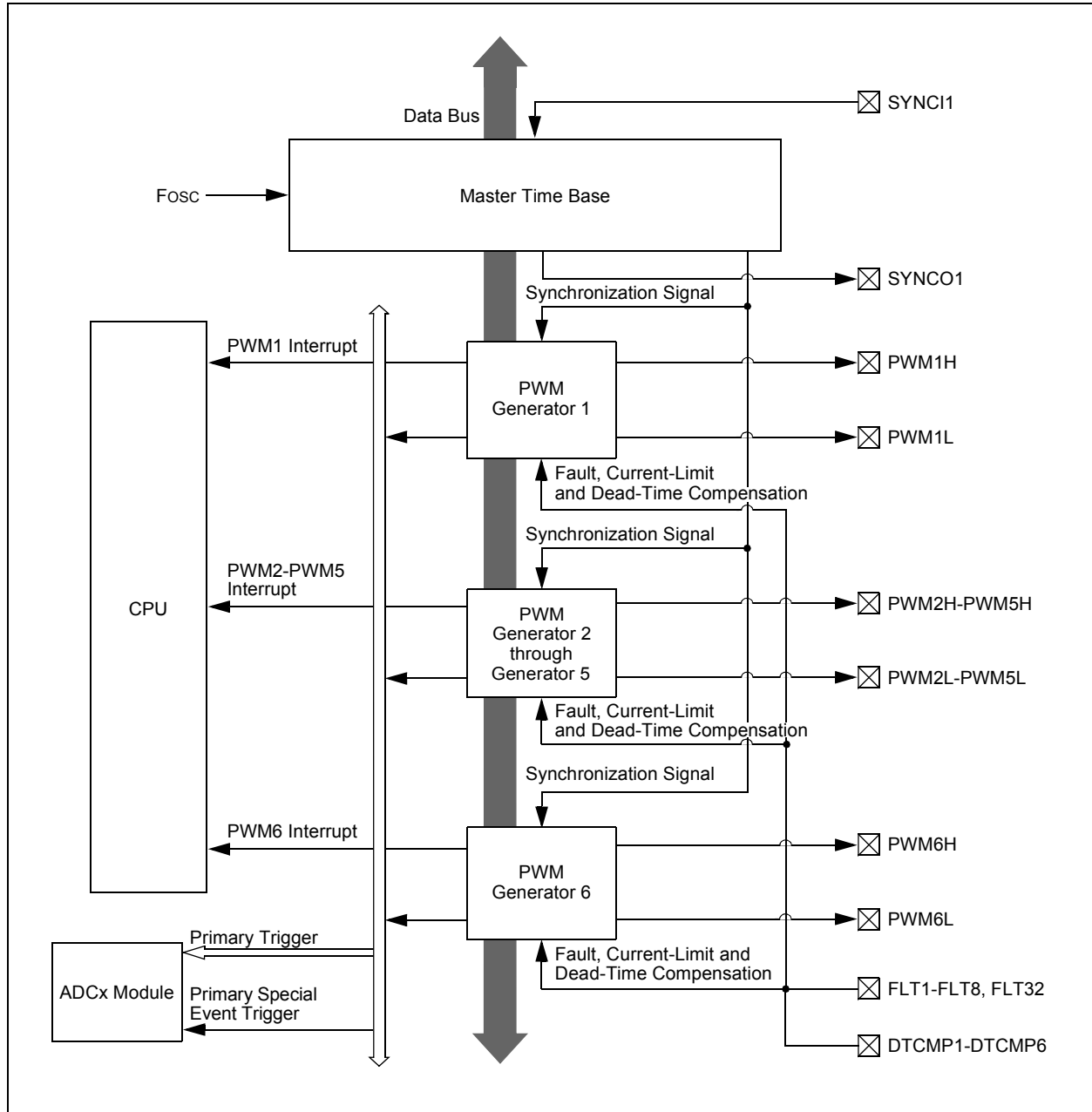
R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **FLTMD:** Fault Mode Select bit
1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts
- bit 14 **FLTOUT:** Fault Out bit
1 = PWM output is driven high on a Fault
0 = PWM output is driven low on a Fault
- bit 13 **FLTTRIEN:** Fault Output State Select bit
1 = OCx pin is tri-stated on a Fault condition
0 = OCx pin I/O state is defined by the FLTOUT bit on a Fault condition
- bit 12 **OCINV:** OCx Invert bit
1 = OCx output is inverted
0 = OCx output is not inverted
- bit 11-9 **Unimplemented:** Read as '0'
- bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)
1 = Cascade module operation is enabled
0 = Cascade module operation is disabled
- bit 7 **OCTRIG:** OCx Trigger/Sync Select bit
1 = Triggers OCx from source designated by the SYNCSELx bits
0 = Synchronizes OCx with source designated by the SYNCSELx bits
- bit 6 **TRIGSTAT:** Timer Trigger Status bit
1 = Timer source has been triggered and is running
0 = Timer source has not been triggered and is being held clear
- bit 5 **OCTRIIS:** OCx Output Pin Direction Select bit
1 = Output Compare x is tri-stated
0 = Output Compare x module drives the OCx pin

- Note 1:** Do not use the OCx module as its own synchronization or trigger source.
- Note 2:** When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.
- Note 3:** Each Output Compare x module (OCx) has one PTG Trigger/Sync source. See **Section 25.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
PTGO4 = OC1, OC5
PTGO5 = OC2, OC6
PTGO6 = OC3, OC7
PTGO7 = OC4, OC8

FIGURE 16-1: HIGH-SPEED PWMx MODULE ARCHITECTURAL OVERVIEW



REGISTER 17-3: QEIXSTAT: QEIX STATUS REGISTER

U-0	U-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
bit 15						bit 8	

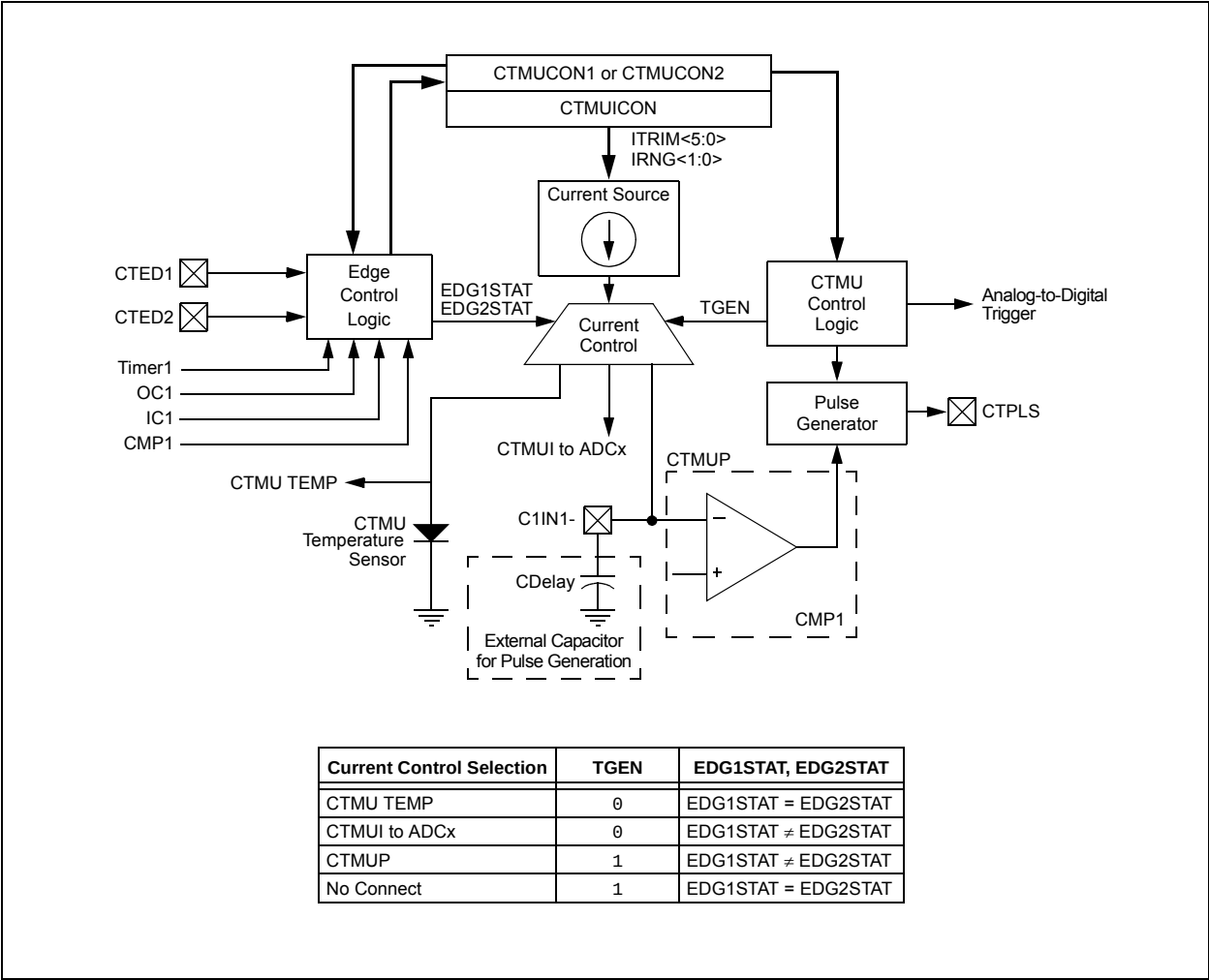
HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
PCIIIRQ ⁽¹⁾	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
bit 7						bit 0	

Legend:	HS = Hardware Settable bit	C = Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **PCHEQIRQ:** Position Counter Greater Than or Equal Compare Status bit
1 = POSxCNT ≥ QEIXGEC
0 = POSxCNT < QEIXGEC
- bit 12 **PCHEQIEN:** Position Counter Greater Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled
- bit 11 **PCLEQIRQ:** Position Counter Less Than or Equal Compare Status bit
1 = POSxCNT ≤ QEIXLEC
0 = POSxCNT > QEIXLEC
- bit 10 **PCLEQIEN:** Position Counter Less Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled
- bit 9 **POSOVIRQ:** Position Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred
- bit 8 **POSOVIEN:** Position Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled
- bit 7 **PCIIIRQ:** Position Counter (Homing) Initialization Process Complete Status bit⁽¹⁾
1 = POSxCNT was reinitialized
0 = POSxCNT was not reinitialized
- bit 6 **PCIIEN:** Position Counter (Homing) Initialization Process Complete interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled
- bit 5 **VELOVIRQ:** Velocity Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred
- bit 4 **VELOVIEN:** Velocity Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled
- bit 3 **HOMIRQ:** Status Flag for Home Event Status bit
1 = Home event has occurred
0 = No home event has occurred

Note 1: This status bit is only applicable to PIMOD<2:0> = 011 and 100 modes.

FIGURE 22-1: CTMU BLOCK DIAGRAM



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REGISTER 24-5: RSCON: DCI RECEIVE SLOT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **RSE<15:0>**: DCI Receive Slot Enable bits
1 = CSDI data is received during Individual Time Slot n
0 = CSDI data is ignored during Individual Time Slot n

REGISTER 24-6: TSCON: DCI TRANSMIT SLOT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **TSE<15:0>**: DCI Transmit Slot Enable Control bits
1 = Transmit buffer contents are sent during Individual Time Slot n
0 = CSDO pin is tri-stated or driven to logic '0' during the individual time slot, depending on the state of the CSDOM bit

26.3 Op Amp/Comparator Control Registers

REGISTER 26-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

R/W-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
PSIDL	—	—	C5EVT ⁽¹⁾	C4EVT ⁽¹⁾	C3EVT ⁽¹⁾	C2EVT ⁽¹⁾	C1EVT ⁽¹⁾
bit 15							bit 8

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	C5OUT ⁽²⁾	C4OUT ⁽²⁾	C3OUT ⁽²⁾	C2OUT ⁽²⁾	C1OUT ⁽²⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **PSIDL:** Op Amp/Comparator Stop in Idle Mode bit
 1 = Discontinues operation of all op amps/comparators when device enters Idle mode
 0 = Continues operation of all op amps/comparators in Idle mode

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **C5EVT:C1EVT:** Op Amp/Comparator 1-5 Event Status bit⁽¹⁾
 1 = Op amp/comparator event occurred
 0 = Op amp/comparator event did not occur

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **C5OUT:C1OUT:** Op Amp/Comparator 1-5 Output Status bit⁽²⁾
 When CPOL = 0:
 1 = VIN+ > VIN-
 0 = VIN+ < VIN-
 When CPOL = 1:
 1 = VIN+ < VIN-
 0 = VIN+ > VIN-

- Note 1:** Reflects the value of the CEVT bit in the respective Op Amp/Comparator x Control register, CMxCON<9>.
- 2:** Reflects the value of the COUT bit in the respective Op Amp/Comparator x Control register, CMxCON<8>.

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REGISTER 27-9: ALRMVAL (WHEN ALRMPTR<1:0> = 01): ALARM WEEKDAY AND HOURS VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15						bit 8	

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.
- bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 29-3: CRCXORH: CRC XOR POLYNOMIAL HIGH REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
X<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
X<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **X<31:16>**: XOR of Polynomial Term X^n Enable bits

REGISTER 29-4: CRCXORL: CRC XOR POLYNOMIAL LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
X<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
X<7:1>							—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-1 **X<15:1>**: XOR of Polynomial Term X^n Enable bits

bit 0 **Unimplemented**: Read as '0'

REGISTER 30-1: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
DEVID<23:16> ⁽¹⁾							
bit 23				bit 16			

R	R	R	R	R	R	R	R
DEVID<15:8> ⁽¹⁾							
bit 15				bit 8			

R	R	R	R	R	R	R	R
DEVID<7:0> ⁽¹⁾							
bit 7				bit 0			

Legend: R = Read-Only bit U = Unimplemented bit

bit 23-0 **DEVID<23:0>**: Device Identifier bits⁽¹⁾

Note 1: Refer to the “dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits” (DS70663) for the list of device ID values.

REGISTER 30-2: DEVREV: DEVICE REVISION REGISTER

R	R	R	R	R	R	R	R
DEVREV<23:16> ⁽¹⁾							
bit 23				bit 16			

R	R	R	R	R	R	R	R
DEVREV<15:8> ⁽¹⁾							
bit 15				bit 8			

R	R	R	R	R	R	R	R
DEVREV<7:0> ⁽¹⁾							
bit 7				bit 0			

Legend: R = Read-only bit U = Unimplemented bit

bit 23-0 **DEVREV<23:0>**: Device Revision bits⁽¹⁾

Note 1: Refer to the “dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits” (DS70663) for the list of device revision values.

TABLE 33-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DI60a	I _{ICL}	Input Low Injection Current	0	—	-5 ^(4,7)	mA	All pins except V _{DD} , V _{SS} , AV _{DD} , AV _{SS} , MCLR, V _{CAP} and RB7
DI60b	I _{ICH}	Input High Injection Current	0	—	+5 ^(5,6,7)	mA	All pins except V _{DD} , V _{SS} , AV _{DD} , AV _{SS} , MCLR, V _{CAP} , RB7 and all 5V tolerant pins ⁽⁶⁾
DI60c	ΣI_{ICT}	Total Input Injection Current (sum of all I/O and control pins)	-20 ⁽⁸⁾	—	+20 ⁽⁸⁾	mA	Absolute instantaneous sum of all $\pm$ input injection currents from all I/O pins: $(I_{ICL} + I_{ICH}) \leq \Sigma I_{ICT}$

- Note 1:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 2:** Negative current is defined as current sourced by the pin.
- 3:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.
- 4:** V_{IL} source < (V_{SS} – 0.3). Characterized but not tested.
- 5:** Non-5V tolerant pins V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins V_{IH} source > 5.5V. Characterized but not tested.
- 6:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.
- 7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 33-16: SPI2 AND SPI3 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS

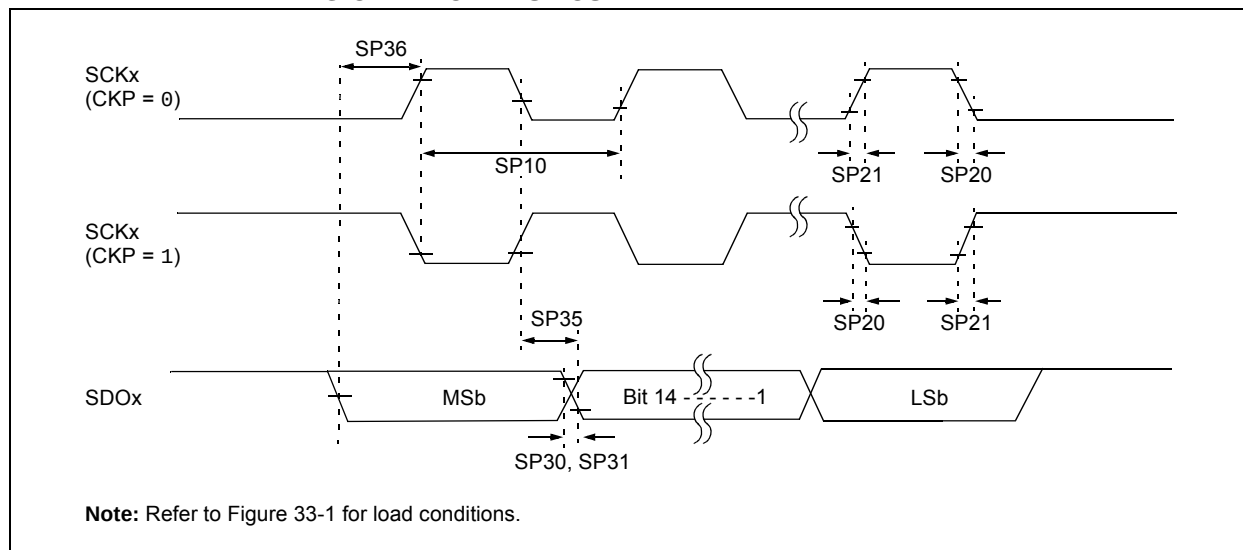


TABLE 33-33: SPI2 AND SPI3 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCKx Frequency	—	—	15	MHz	(Note 3)
SP20	TscF	SCKx Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCKx Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	

- Note 1:** These parameters are characterized, but are not tested in manufacturing.
- Note 2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
- Note 3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.
- Note 4:** Assumes 50 pF load on all SPIx pins.