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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm604-e-pt

dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN49	I	Analog	No	Analog Input Channels 0-49.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	I	ST/ CMOS	No	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	O	—	No	32.768 kHz low-power oscillator crystal output.
IC1-IC8	I	ST	Yes	Input Capture Inputs 1 through 8.
OCFA	I	ST	Yes	Output Compare Fault A input (for compare channels).
OCFB	I	ST	No	Output Compare Fault B input (for compare channels).
OC1-OC8	O	—	Yes	Output Compare 1 through 8.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
INT3	I	ST	No	External Interrupt 3.
INT4	I	ST	No	External Interrupt 4.
RA0-RA4, RA7-RA12, RA14-RA15	I/O	ST	Yes	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	Yes	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	Yes	PORTC is a bidirectional I/O port.
RD1-RD6, RD8, RD12-RD15	I/O	ST	Yes	PORTD is a bidirectional I/O port.
RE0-RE1, RE8-RE9, RE12-RE15	I/O	ST	Yes	PORTE is a bidirectional I/O port.
RF0-RF1, RF4-RF7, RF9-RF10, RF12-RF13	I/O	ST	No	PORTF is a bidirectional I/O port.
RG0-RG3, RG6-RG15	I/O	ST	Yes	PORTG is a bidirectional I/O port.
T1CK	I	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	No	Timer3 external clock input.
T4CK	I	ST	No	Timer4 external clock input.
T5CK	I	ST	No	Timer5 external clock input.
T6CK	I	ST	No	Timer6 external clock input.
T7CK	I	ST	No	Timer7 external clock input.
T8CK	I	ST	No	Timer8 external clock input.
T9CK	I	ST	No	Timer9 external clock input.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

Note 1: This pin is not available on all devices. For more information, see the “Pin Diagrams” section for pin availability.

2: AVDD must be connected at all times.

4.3 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
W0	0000	W0 (WREG)																xxxx	
W1	0002	W1																xxxx	
W2	0004	W2																xxxx	
W3	0006	W3																xxxx	
W4	0008	W4																xxxx	
W5	000A	W5																xxxx	
W6	000C	W6																xxxx	
W7	000E	W7																xxxx	
W8	0010	W8																xxxx	
W9	0012	W9																xxxx	
W10	0014	W10																xxxx	
W11	0016	W11																xxxx	
W12	0018	W12																xxxx	
W13	001A	W13																xxxx	
W14	001C	W14																xxxx	
W15	001E	W15																xxxx	
SPLIM	0020	SPLIM																0000	
ACCAL	0022	ACCAL																0000	
ACCAH	0024	ACCAH																0000	
ACCAU	0026	Sign Extension of ACCA<39>									ACCAU							0000	
ACCBL	0028	ACCBL																0000	
ACCBH	002A	ACCBH																0000	
ACCBU	002C	Sign Extension of ACCB<39>									ACCBU							0000	
PCL	002E	Program Counter Low Word Register																—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	Program Counter High Word Register							0000	
DSRPAG	0032	—	—	—	—	—	—	Data Space Read Page Register										0001	
DSWPAG	0034	—	—	—	—	—	—	—	Data Space Write Page Register										0001
RCOUNT	0036	REPEAT Loop Count Register																0000	
DCOUNT	0038	DCOUNT<15:0>																0000	
DOSTARTL	003A	DOSTARTL<15:1>																—	0000
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>					0000		
DOENDL	003E	DOENDL<15:1>																—	0000
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH<5:0>					0000		

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: CAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES⁽¹⁾ (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C2RXF11SID	056C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C2RXF11EID	056E	EID<15:0>																xxxx
C2RXF12SID	0570	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF12EID	0572	EID<15:0>																xxxx
C2RXF13SID	0574	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF13EID	0576	EID<15:0>																xxxx
C2RXF14SID	0578	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF14EID	057A	EID<15:0>																xxxx
C2RXF15SID	057C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF15EID	057E	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

TABLE 4-29: PROGRAMMABLE CRC REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CRCCON1	0640	CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0	CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—	0000
CRCCON2	0642	—	—	—	DWIDTH4	DWIDTH3	DWIDTH2	DWIDTH1	DWIDTH0	—	—	—	PLEN4	PLEN3	PLEN2	PLEN1	PLEN0	0000
CRCXORL	0644	X<15:1>																0000
CRCXORH	0646	X<31:16>																0000
CRCDATL	0648	CRC Data Input Low Word Register																0000
CRCDATL	064A	CRC Data Input High Word Register																0000
CRCWDATL	064C	CRC Result Low Word Register																0000
CRCWDATH	064E	CRC Result High Word Register																0000

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

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SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB<15:0>																DF9F
PORTB	0E12	RB<15:0>																xxxx
LATB	0E14	LATB<15:0>																xxxx
ODCB	0E16	ODCB<15:0>																0000
CNENB	0E18	CNIEB<15:0>																0000
CNPUB	0E1A	CNPUB<15:0>																0000
CNPDB	0E1C	CNPDB<15:0>																0000
ANSELB	0E1E	—	—	—	—	—	—	ANSB<9:7>			—	—	—	ANSB<3:0>				010F

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-51: PORTB REGISTER MAP FOR dsPIC33EPXXXGM304/604 DEVICES

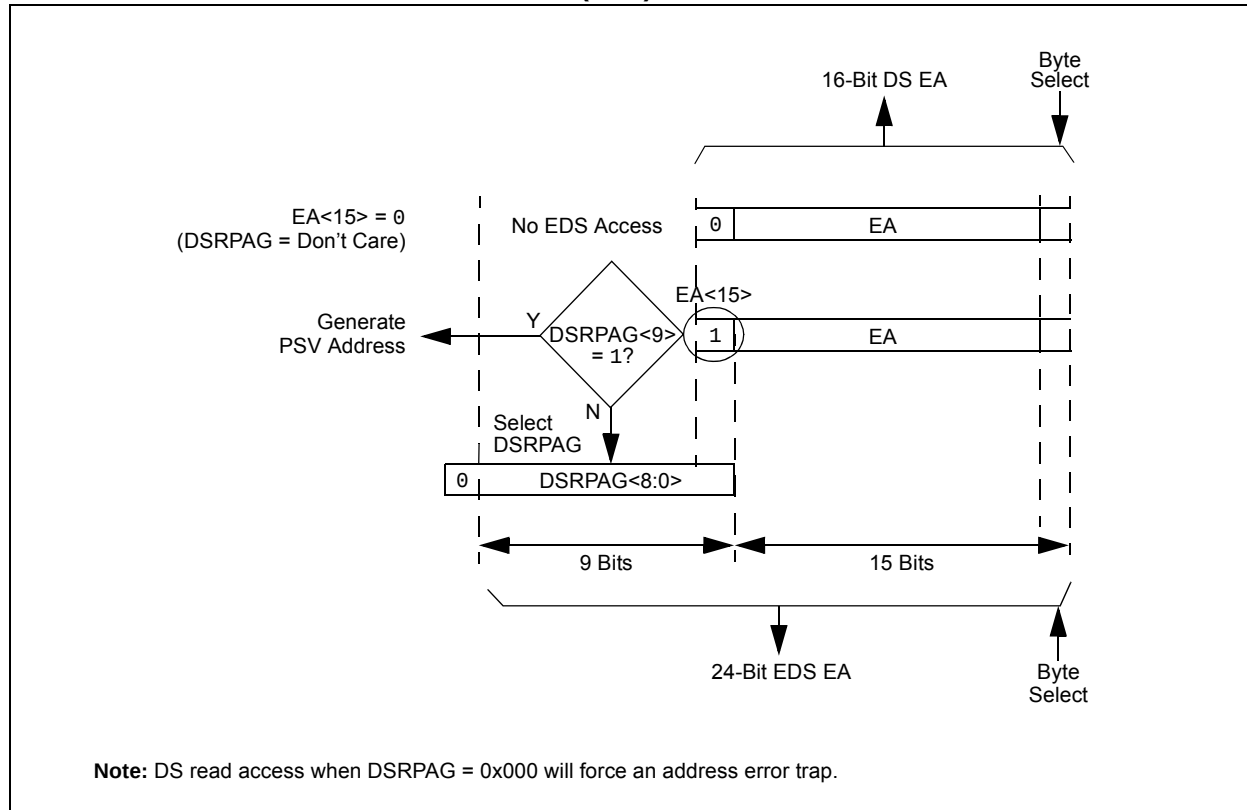
Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.3.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGM3XX/6XX/7XX architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre- and post-modified Effective Addresses (EA). The upper half of the Base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Data Space Read Page register (DSRPAG) or the 9-bit Data Space Write Page register (DSWPAG), to form an Extended Data Space (EDS) address, or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

Construction of the EDS address is shown in Figure 4-8. When DSRPAG<9> = 0 and the base address bit, EA<15> = 1, the DSRPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS read address. Similarly, when the base address bit, EA<15> = 1, the DSWPAG<8:0> bits are concatenated onto EA<14:0> to form the 24-bit EDS write address.

FIGURE 4-8: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION



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REGISTER 11-19: RPINR25: PERIPHERAL PIN SELECT INPUT REGISTER 25

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COFSR<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7

Unimplemented: Read as '0'

bit 6-0

COFSR<6:0>: Assign DCI Frame Sync Input (COFS) to the Corresponding RPN Pin bits
(see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•
•
•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-26: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP1R<6:0>						
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP1R<6:0>:** Assign PWM Dead-Time Compensation Input 1 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•

•

•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

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14.1 Input Capture Control Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7						bit 0	

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture x Stop in Idle Mode Control bit
 1 = Input Capture x halts in CPU Idle mode
 0 = Input Capture x continues to operate in CPU Idle mode

bit 12-10 **ICTSEL<2:0>:** Input Capture x Timer Select bits
 111 = Peripheral clock (FP) is the clock source of ICx
 110 = Reserved
 101 = Reserved
 100 = T1CLK is the clock source of ICx (only the synchronous clock is supported)
 011 = T5CLK is the clock source of ICx
 010 = T4CLK is the clock source of ICx
 001 = T2CLK is the clock source of ICx
 000 = T3CLK is the clock source of ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits
 (this field is not used if ICM<2:0> = 001 or 111)
 11 = Interrupts on every fourth capture event
 10 = Interrupts on every third capture event
 01 = Interrupts on every second capture event
 00 = Interrupts on every capture event

bit 4 **ICOV:** Input Capture x Overflow Status Flag bit (read-only)
 1 = Input Capture x buffer overflow occurred
 0 = No Input Capture x buffer overflow occurred

bit 3 **ICBNE:** Input Capture x Buffer Not Empty Status bit (read-only)
 1 = Input Capture x buffer is not empty, at least one more capture value can be read
 0 = Input Capture x buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture x Mode Select bits
 111 = Input Capture x functions as an interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
 110 = Unused (module disabled)
 101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
 100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
 011 = Capture mode, every rising edge (Simple Capture mode)
 010 = Capture mode, every falling edge (Simple Capture mode)
 001 = Capture mode, every edge, rising and falling (Edge Detect mode, ICI<1:0>), is not used in this mode)
 000 = Input Capture x module is turned off

REGISTER 16-18: TRGCONx: PWMx TRIGGER CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TRGSTRT5 ⁽¹⁾	TRGSTRT5 ⁽¹⁾	TRGSTRT5 ⁽¹⁾	TRGSTRT5 ⁽¹⁾	TRGSTRT5 ⁽¹⁾	TRGSTRT5 ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **TRGDIV<3:0>**: Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event
 1110 = Trigger output for every 15th trigger event
 1101 = Trigger output for every 14th trigger event
 1100 = Trigger output for every 13th trigger event
 1011 = Trigger output for every 12th trigger event
 1010 = Trigger output for every 11th trigger event
 1001 = Trigger output for every 10th trigger event
 1000 = Trigger output for every 9th trigger event
 0111 = Trigger output for every 8th trigger event
 0110 = Trigger output for every 7th trigger event
 0101 = Trigger output for every 6th trigger event
 0100 = Trigger output for every 5th trigger event
 0011 = Trigger output for every 4th trigger event
 0010 = Trigger output for every 3rd trigger event
 0001 = Trigger output for every 2nd trigger event
 0000 = Trigger output for every trigger event

bit 11-6 **Unimplemented**: Read as '0'

bit 5-0 **TRGSTRT<5:0>**: Trigger Postscaler Start Enable Select bits⁽¹⁾

111111 = Wait 63 PWM cycles before generating the first trigger event after the module is enabled
 •
 •
 •

000010 = Wait 2 PWM cycles before generating the first trigger event after the module is enabled

000001 = Wait 1 PWM cycle before generating the first trigger event after the module is enabled

000000 = Wait 0 PWM cycles before generating the first trigger event after the module is enabled

Note 1: The secondary PWM generator cannot generate PWM trigger interrupts.

21.4 CAN Message Buffers

CAN Message Buffers are part of RAM memory. They are not CAN Special Function Registers. The user application must directly write into the RAM area that is configured for CAN Message Buffers. The location and size of the buffer area is defined by the user application.

BUFFER 21-1: CANx MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'
 bit 12-2 **SID<10:0>:** Standard Identifier bits
 bit 1 **SRR:** Substitute Remote Request bit
 When IDE = 0:
 1 = Message will request remote transmission
 0 = Normal message
 When IDE = 1:
 The SRR bit must be set to '1'.
 bit 0 **IDE:** Extended Identifier bit
 1 = Message will transmit an Extended Identifier
 0 = Message will transmit a Standard Identifier

BUFFER 21-2: CANx MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	EID<17:14>			
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<13:6>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'
 bit 11-0 **EID<17:6>:** Extended Identifier bits

FIGURE 26-3: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM

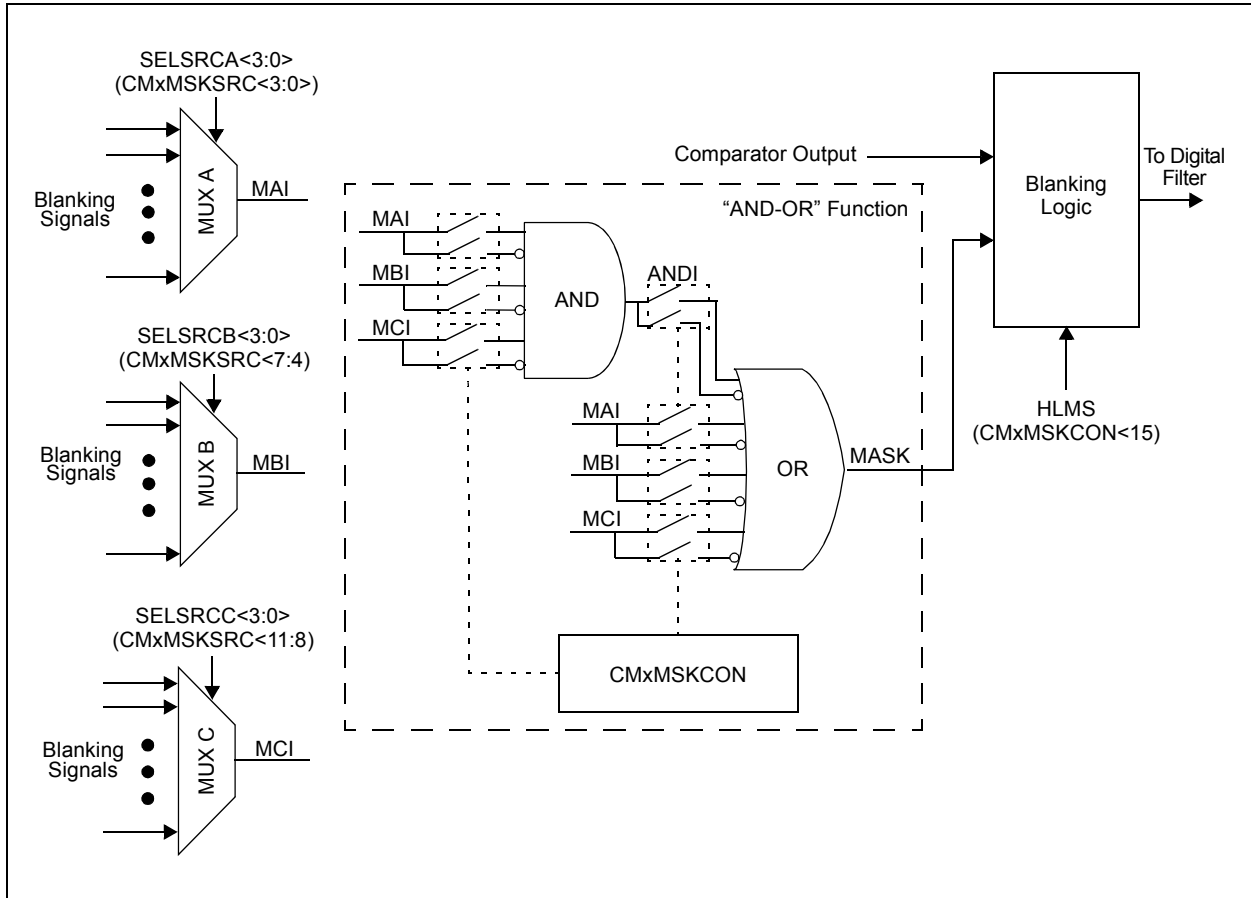
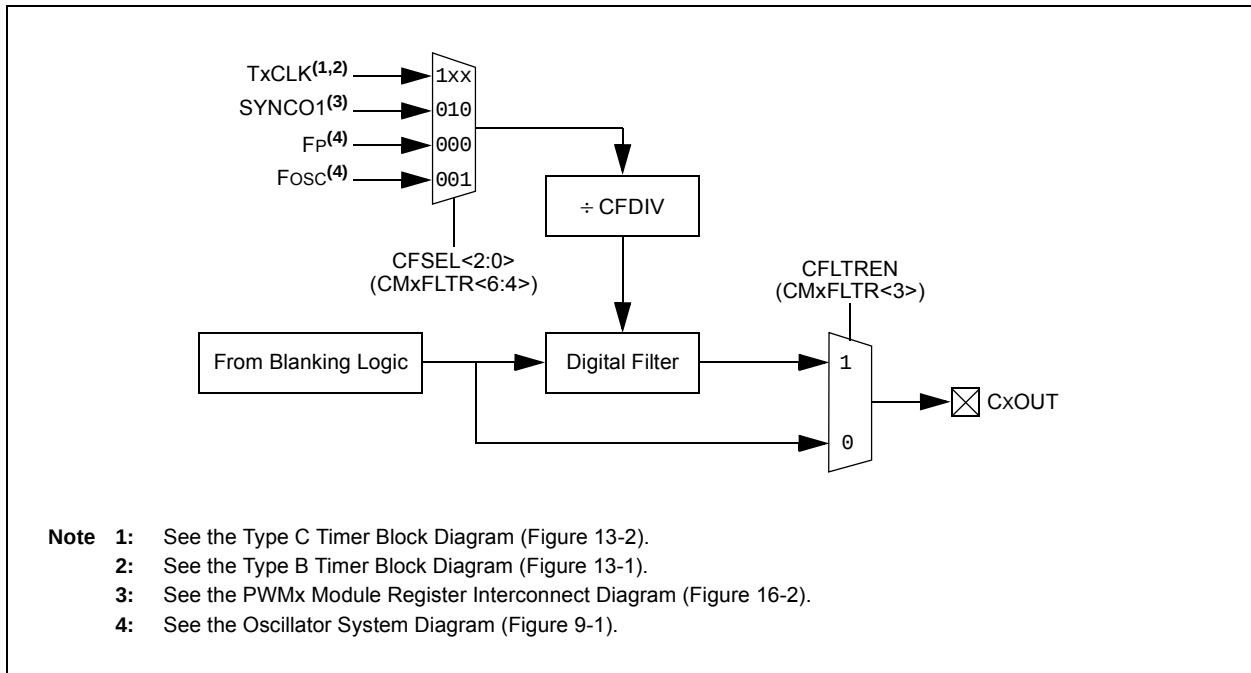


FIGURE 26-4: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM



REGISTER 27-2: PADCFG1: PAD CONFIGURATION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	RTSECSEL ⁽¹⁾	PMPTTL
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **RTSECSEL:** RTCC Seconds Clock Output Select bit⁽¹⁾

1 = RTCC seconds clock is selected for the RTCC pin

0 = RTCC alarm pulse is selected for the RTCC pin

bit 0 Not used by the RTCC module.

Note 1: To enable the actual RTCC output, the RTCOE bit (RCFGCAL<10>) must be set.

REGISTER 27-10: ALRMVAL (WHEN ALRMPTR<1:0> = 00): ALARM MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **MINTEN<2:0>:** Binary Coded Decimal Value of Minute's Tens Digit bits
Contains a value from 0 to 5.

bit 11-8 **MINONE<3:0>:** Binary Coded Decimal Value of Minute's Ones Digit bits
Contains a value from 0 to 9.

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **SECTEN<2:0>:** Binary Coded Decimal Value of Second's Tens Digit bits
Contains a value from 0 to 5.

bit 3-0 **SECONE<3:0>:** Binary Coded Decimal Value of Second's Ones Digit bits
Contains a value from 0 to 9.

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TABLE 30-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Description
WDTPRE	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1
WDTWIN<1:0>	Watchdog Timer Window Select bits 11 = WDT Window is 25% of WDT Period 10 = WDT Window is 37.5% of WDT Period 01 = WDT Window is 50% of WDT Period 00 = WDT Window is 75% of WDT Period
ALTI2C1	Alternate I2C1 Pins bit 1 = I2C1 is mapped to the SDA1/SCL1 pins 0 = I2C1 is mapped to the ASDA1/ASCL1 pins
ALTI2C2	Alternate I2C2 Pins bit 1 = I2C2 is mapped to the SDA2/SCL2 pins 0 = I2C2 is mapped to the ASDA2/ASCL2 pins
BOREN	Brown-out Reset (BOR) Detection Enable bit 1 = BOR is enabled 0 = BOR is disabled
JTAGEN	JTAG Enable bit 1 = JTAG is enabled 0 = JTAG is disabled
ICS<1:0>	ICD Communication Channel Select bits 11 = Communicates on PGEC1 and PGED1 10 = Communicates on PGEC2 and PGED2 01 = Communicates on PGEC3 and PGED3 00 = Reserved, do not use

Note 1: The Two-Speed Start-up is not enabled when EC mode is used since the EC clocks will be ready immediately.

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TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
25	DAW	DAW Wn	Wn = decimal adjust Wn	1	1	C
26	DEC	DEC f	$f = f - 1$	1	1	C,DC,N,OV,Z
		DEC f, WREG	WREG = $f - 1$	1	1	C,DC,N,OV,Z
		DEC Ws, Wd	Wd = $Ws - 1$	1	1	C,DC,N,OV,Z
27	DEC2	DEC2 f	$f = f - 2$	1	1	C,DC,N,OV,Z
		DEC2 f, WREG	WREG = $f - 2$	1	1	C,DC,N,OV,Z
		DEC2 Ws, Wd	Wd = $Ws - 2$	1	1	C,DC,N,OV,Z
28	DISI	DISI #lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S Wm, Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD Wm, Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U Wm, Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD Wm, Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF Wm, Wn	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO #lit15, Expr	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO Wn, Expr	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED Wm*Wm, Acc, Wx, Wy, Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB,SA,SB,SAB
33	EDAC	EDAC Wm*Wm, Acc, Wx, Wy, Wxd	Euclidean Distance	1	1	OA,OB,OAB,SA,SB,SAB
34	EXCH	EXCH Wns, Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL Ws, Wnd	Find Bit Change from Left (MSb) Side	1	1	C
36	FF1L	FF1L Ws, Wnd	Find First One from Left (MSb) Side	1	1	C
37	FF1R	FF1R Ws, Wnd	Find First One from Right (LSb) Side	1	1	C
38	GOTO	GOTO Expr	Go to address	2	4	None
		GOTO Wn	Go to indirect	1	4	None
		GOTO.L Wn	Go to indirect (long address)	1	4	None
39	INC	INC f	$f = f + 1$	1	1	C,DC,N,OV,Z
		INC f, WREG	WREG = $f + 1$	1	1	C,DC,N,OV,Z
		INC Ws, Wd	Wd = $Ws + 1$	1	1	C,DC,N,OV,Z
40	INC2	INC2 f	$f = f + 2$	1	1	C,DC,N,OV,Z
		INC2 f, WREG	WREG = $f + 2$	1	1	C,DC,N,OV,Z
		INC2 Ws, Wd	Wd = $Ws + 2$	1	1	C,DC,N,OV,Z
41	IOR	IOR f	$f = f . \text{IOR. WREG}$	1	1	N,Z
		IOR f, WREG	WREG = $f . \text{IOR. WREG}$	1	1	N,Z
		IOR #lit10, Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR Wb, Ws, Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR Wb, #lit5, Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC Ws0, #Slit4, Acc	Load Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
43	LNK	LNK #lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR f	$f = \text{Logical Right Shift } f$	1	1	C,N,OV,Z
		LSR f, WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR Ws, Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR Wb, Wns, Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR Wb, #lit5, Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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**TABLE 33-38: SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCKx Input Frequency	—	—	15	MHz	(Note 3)
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	(Note 4)
SP52	Tsch2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	1.5 TCY + 40	—	—	ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

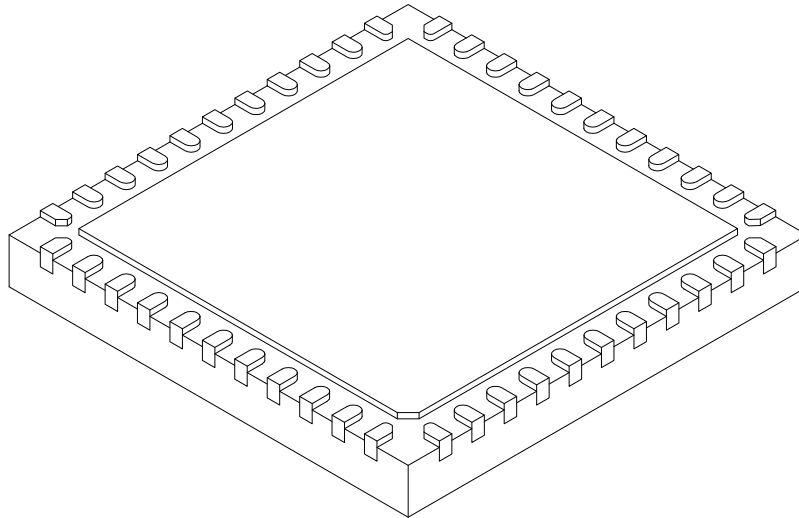
3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

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44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	44		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	8.00 BSC		
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension. usually without tolerance, for information purposes only.

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PMD2 (Peripheral Module Disable Control 2)	158	RPINR27 (Peripheral Pin Select Input 27).....	194
PMD3 (Peripheral Module Disable Control 3)	159	RPINR28 (Peripheral Pin Select Input 28).....	195
PMD4 (Peripheral Module Disable Control 4)	161	RPINR29 (Peripheral Pin Select Input 29).....	196
PMD6 (Peripheral Module Disable Control 6)	161	RPINR3 (Peripheral Pin Select Input 3).....	177
PMD7 (Peripheral Module Disable Control 7)	162	RPINR30 (Peripheral Pin Select Input 30).....	197
PMODE (Parallel Master Port Mode)	398	RPINR37 (Peripheral Pin Select Input 37).....	198
PMSTAT (Parallel Master Port Status)	402	RPINR38 (Peripheral Pin Select Input 38).....	199
POSxCNTH (Position Counter x High Word)	265	RPINR39 (Peripheral Pin Select Input 39).....	200
POSxCNTL (Position Counter x Low Word)	265	RPINR40 (Peripheral Pin Select Input 40).....	201
POSxHLD (Position Counter x Hold)	266	RPINR41 (Peripheral Pin Select Input 41).....	202
PTCON (PWMx Time Base Control)	233	RPINR7 (Peripheral Pin Select Input 7).....	178
PTCON2 (PWMx Primary Master Clock Divider Select 2)	235	RPINR8 (Peripheral Pin Select Input 8).....	179
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QEIXICL (QEIX Initialization/Capture Low Word)	268	RTCVAL (Month and Day Value, RTCPTR = 10)	389
QEIXIOC (QEIX I/O Control)	261	RTCVAL (Weekday and Hours Value, RTCPTR = 01)	390
QEIXLECH (QEIX Less Than or Equal Compare High Word)	269	RTCVAL (Year Value, RTCPTR = 11)	389
QEIXLECL (QEIX Less Than or Equal Compare Low Word)	269	SDCx (PWMx Secondary Duty Cycle)	244
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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

dsPIC 33 EP 512 GM7 10 T - I / PT XXX Microchip Trademark _____ Architecture _____ Core Family _____ Program Memory Size (Kbytes) _____ Product Group _____ Pin Count _____ Tape and Reel Flag (if applicable) _____ Temperature Range _____ Package _____ Pattern _____		Example: dsPIC33EP512GM710-I/PT: dsPIC33, Enhanced Performance, 512-Kbyte program memory, 100-pin, Industrial temperature, TQFP package.
Architecture: 33 = 16-Bit Digital Signal Controller Family: EP = Enhanced Performance Product Group: GM7 = General Purpose plus Motor Control Family Pin Count: 04 = 44-pin 06 = 64-pin 10 = 100/124-pin Temperature Range: I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended) Package: BG = Plastic Thin Profile Ball Grid Array - (121-pin) 10x10 mm body (TFBGA) ML = Plastic Quad, No Lead Package - (44-pin) 8x8 mm body (QFN) MR = Plastic Quad, No Lead Package - (64-pin) 9x9 mm body (QFN) PT = Plastic Thin Quad Flatpack - (44-pin) 10x10 mm body (TQFP) PT = Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) PT = Thin Quad Flatpack - (100-pin) 12x12x1 mm body (TQFP) PF = Thin Quad Flatpack - (100-pin) 14x14x1 mm body (TQFP)		