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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	-
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 30x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm706-h-mr

dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP256GM3XX/6XX/7XX DEVICES⁽¹⁾

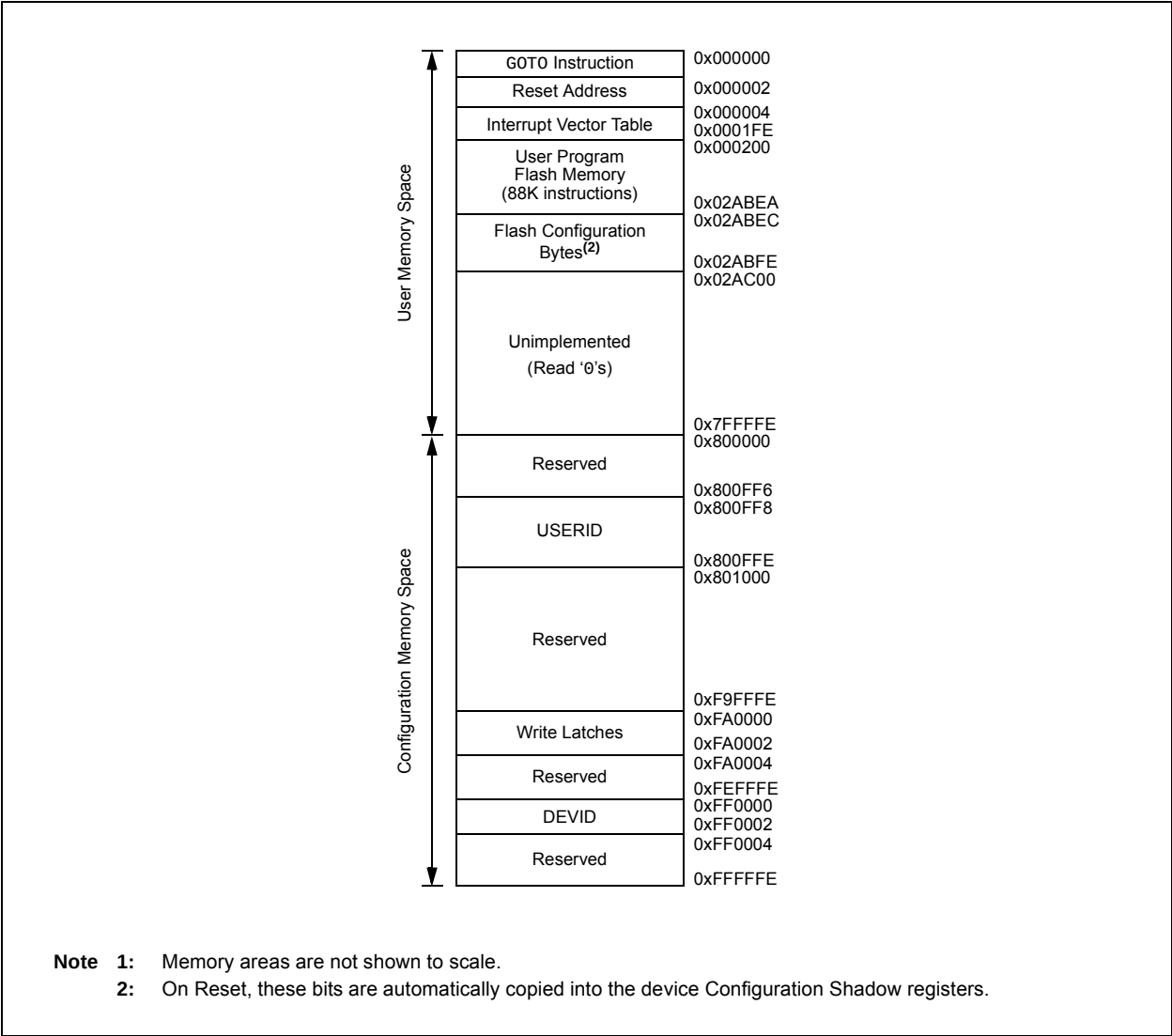


TABLE 4-4: TIMERS REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																0000
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register																0000
TMR3HLD	0108	Timer3 Holding Register (For 32-bit timer operations only)																xxxx
TMR3	010A	Timer3 Register																0000
PR2	010C	Period Register 2																FFFF
PR3	010E	Period Register 3																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR4	0114	Timer4 Register																0000
TMR5HLD	0116	Timer5 Holding Register (For 32-bit timer operations only)																xxxx
TMR5	0118	Timer5 Register																0000
PR4	011A	Period Register 4																FFFF
PR5	011C	Period Register 5																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR6	0122	Timer6 Register																0000
TMR7HLD	0124	Timer7 Holding Register (For 32-bit timer operations only)																xxxx
TMR7	0126	Timer7 Register																0000
PR6	0128	Period Register 6																FFFF
PR7	012A	Period Register 7																FFFF
T6CON	012C	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T7CON	012E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR8	0130	Timer8 Register																0000
TMR9HLD	0132	Timer9 Holding Register (For 32-bit timer operations only)																xxxx
TMR9	0134	Timer9 Register																0000
PR8	0136	Period Register 8																FFFF
PR9	0138	Period Register 9																FFFF
T8CON	013A	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T9CON	013C	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES⁽¹⁾

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400-041E	See definition when WIN = x																
C1BUFPNT1	0420	F3BP3	F3BP2	F3BP1	F3BP0	F2BP3	F2BP2	F2BP1	F2BP0	F1BP3	F1BP2	F1BP1	F1BP0	F0BP3	F0BP2	F0BP1	F0BP0	0000
C1BUFPNT2	0422	F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0	F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0	0000
C1BUFPNT3	0424	F11BP3	F11BP2	F11BP1	F11BP0	F10BP3	F10BP2	F10BP1	F10BP0	F9BP3	F9BP2	F9BP1	F9BP0	F8BP3	F8BP2	F8BP1	F8BP0	0000
C1BUFPNT4	0426	F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0	F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0	0000
C1RXM0SID	0430	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C1RXM0EID	0432	EID<15:0>																xxxx
C1RXM1SID	0434	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C1RXM1EID	0436	EID<15:0>																xxxx
C1RXM2SID	0438	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C1RXM2EID	043A	EID<15:0>																xxxx
C1RXF0SID	0440	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF0EID	0442	EID<15:0>																xxxx
C1RXF1SID	0444	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF1EID	0446	EID<15:0>																xxxx
C1RXF2SID	0448	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF2EID	044A	EID<15:0>																xxxx
C1RXF3SID	044C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF3EID	044E	EID<15:0>																xxxx
C1RXF4SID	0450	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF4EID	0452	EID<15:0>																xxxx
C1RXF5SID	0454	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF5EID	0456	EID<15:0>																xxxx
C1RXF6SID	0458	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF6EID	045A	EID<15:0>																xxxx
C1RXF7SID	045C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF7EID	045E	EID<15:0>																xxxx
C1RXF8SID	0460	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF8EID	0462	EID<15:0>																xxxx
C1RXF9SID	0464	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF9EID	0466	EID<15:0>																xxxx
C1RXF10SID	0468	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF10EID	046A	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses an EDS or PSV page
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing. However, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSxPAG register is incremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-64 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

TABLE 4-64: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS AND PSV SPACE BOUNDARIES^(2,3,4)

O/U, R/W	Operation	Before			After		
		DSxPAG	DS EA<15>	Page Description	DSxPAG	DS EA<15>	Page Description
O, Read	[++Wn] or [Wn++]	DSRPAG = 0x1FF	1	EDS: Last Page	DSRPAG = 0x1FF	0	See Note 1
O, Read		DSRPAG = 0x2FF	1	PSV: Last lsw Page	DSRPAG = 0x300	1	PSV: First MSB Page
O, Read		DSRPAG = 0x3FF	1	PSV: Last MSB Page	DSRPAG = 0x3FF	0	See Note 1
O, Write		DSWPAG = 0x1FF	1	EDS: Last Page	DSWPAG = 0x1FF	0	See Note 1
U, Read	[- -Wn] or [Wn - -]	DSRPAG = 0x001	1	PSV Page	DSRPAG = 0x001	0	See Note 1
U, Read		DSRPAG = 0x200	1	PSV: First lsw Page	DSRPAG = 0x200	0	See Note 1
U, Read		DSRPAG = 0x300	1	PSV: First MSB Page	DSRPAG = 0x2FF	1	PSV: Last lsw Page

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the Base Data Space (0x0000-0x8000).

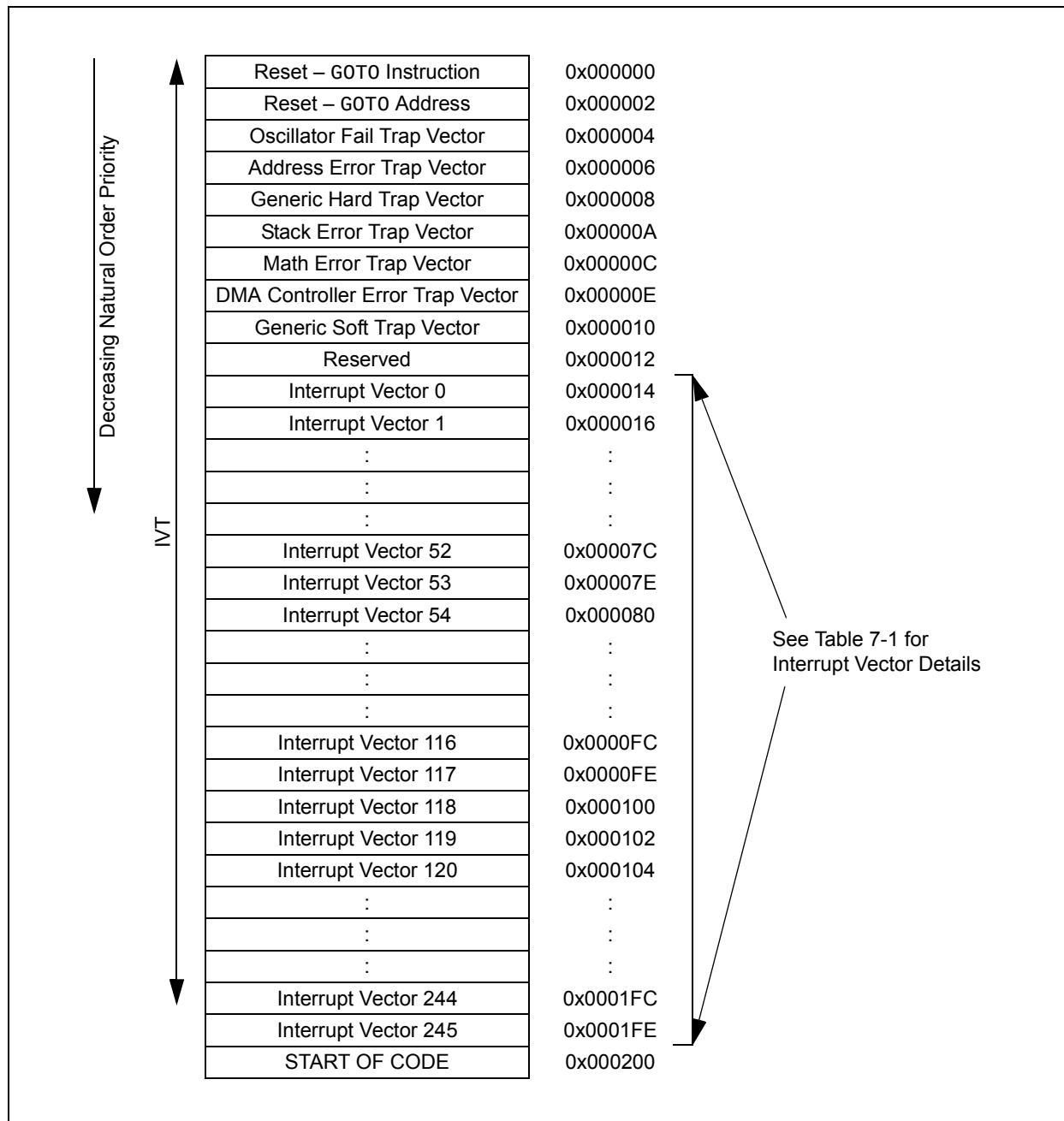
2: An EDS access with DSxPAG = 0x000 will generate an address error trap.

3: Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.

4: Pseudo Linear Addressing is not supported for large offsets.

dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 7-1: dsPIC33EPXXXGM3XX/6XX/7XX INTERRUPT VECTOR TABLE



dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER⁽²⁾

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE2 ⁽³⁾	DOZE1 ⁽³⁾	DOZE0 ⁽³⁾	DOZEN ^(1,4)	FRCDIV2	FRCDIV1	FRCDIV0
bit 15							bit 8

R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOST1	PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **ROI:** Recover on Interrupt bit
 1 = Interrupts will clear the DOZEN bit
 0 = Interrupts will have no effect on the DOZEN bit
- bit 14-12 **DOZE<2:0>:** Processor Clock Reduction Select bits⁽³⁾
 111 = Fcy divided by 128
 110 = Fcy divided by 64
 101 = Fcy divided by 32
 100 = Fcy divided by 16
 011 = Fcy divided by 8 (default)
 010 = Fcy divided by 4
 001 = Fcy divided by 2
 000 = Fcy divided by 1
- bit 11 **DOZEN:** Doze Mode Enable bit^(1,4)
 1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks
 0 = Processor clock and peripheral clock ratio are forced to 1:1
- bit 10-8 **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits
 111 = FRC divided by 256
 110 = FRC divided by 64
 101 = FRC divided by 32
 100 = FRC divided by 16
 011 = FRC divided by 8
 010 = FRC divided by 4
 001 = FRC divided by 2
 000 = FRC divided by 1 (default)
- bit 7-6 **PLLPOST<1:0>:** PLL VCO Output Divider Select bits (also denoted as 'N2', PLL postscaler)
 11 = Output divided by 8
 10 = Reserved
 01 = Output divided by 4 (default)
 00 = Output divided by 2
- bit 5 **Unimplemented:** Read as '0'

- Note 1:** This bit is cleared when the ROI bit is set and an interrupt occurs.
Note 2: This register resets only on a Power-on Reset (POR).
Note 3: The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
Note 4: The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 10-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
—	—	—	DMA0MD ⁽¹⁾	PTGMD	—	—	—
			DMA1MD ⁽¹⁾				
			DMA2MD ⁽¹⁾				
			DMA3MD ⁽¹⁾				
bit 7			bit 0				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-5 **Unimplemented:** Read as '0'
- bit 4 **DMA0MD:** DMA0 Module Disable bit⁽¹⁾
 1 = DMA0 module is disabled
 0 = DMA0 module is enabled
- DMA1MD:** DMA1 Module Disable bit⁽¹⁾
 1 = DMA1 module is disabled
 0 = DMA1 module is enabled
- DMA2MD:** DMA2 Module Disable bit⁽¹⁾
 1 = DMA2 module is disabled
 0 = DMA2 module is enabled
- DMA3MD:** DMA3 Module Disable bit⁽¹⁾
 1 = DMA3 module is disabled
 0 = DMA3 module is enabled
- bit 3 **PTGMD:** PTG Module Disable bit
 1 = PTG module is disabled
 0 = PTG module is enabled
- bit 2-0 **Unimplemented:** Read as '0'

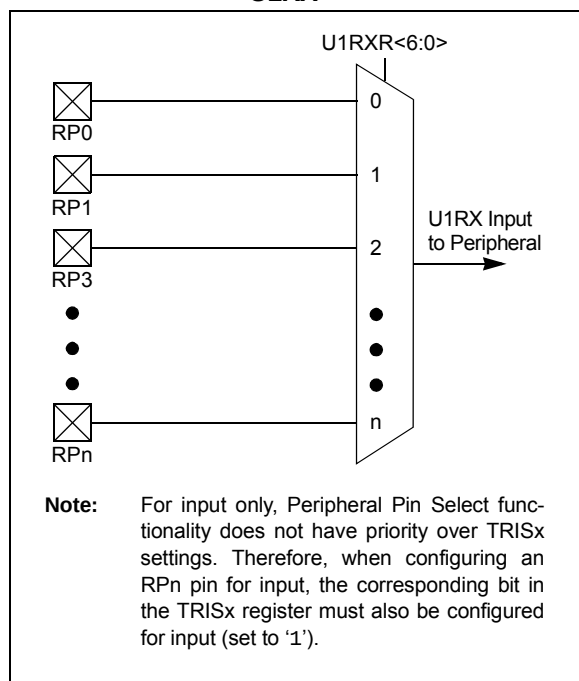
Note 1: This single bit enables and disables all four DMA channels.

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINR_x registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-29). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RP_n pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



11.4.4.1 Virtual Connections

dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 26-1 in **Section 26.0 “Op Amp/Comparator Module”**) and the PTG module (see **Section 25.0 “Peripheral Trigger Generator (PTG) Module”**).

In addition, dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual connections to the filtered QE_Ix module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 “Quadrature Encoder Interface (QEI) Module”**).

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of 'b0000001', the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QE_Ix module allows peripherals to be connected to the QE_Ix digital filter input. To utilize this filter, the QE_Ix module must be enabled and its inputs must be connected to a physical RP_n pin. Example 11-2 illustrates how the input capture module can be connected to the QE_Ix digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QE1 DIGITAL FILTER INPUT ON PIN 43

```
RPINR15 = 0x2500;    /* Connect the QE1 HOME1 input to RP37 (pin 43) */
RPINR7  = 0x009;     /* Connect the IC1 input to the digital filter on the FHOME1 input */

QE1I1OC = 0x4000;    /* Enable the QE1 digital filter */
QE1I1CON = 0x8000;    /* Enable the QE1 module */
```

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 16-21: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL ⁽¹⁾	CLMOD
bit 15						bit 8	

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL ⁽¹⁾	FLTMOD1	FLTMOD0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **IFLTMOD:** Independent Fault Mode Enable bit

1 = Independent Fault mode is enabled

0 = Independent Fault mode is disabled

bit 14-10 **CLSRC<4:0>:** Current-Limit Control Signal Source Select for the PWMx Generator # bits

11111 = Fault 32

11110 = Reserved

•

•

•

01100 = Op Amp/Comparator 5

01011 = Comparator 4

01010 = Op Amp/Comparator 3

01001 = Op Amp/Comparator 2

01000 = Op Amp/Comparator 1

00111 = Fault 8

00110 = Fault 7

00101 = Fault 6

00100 = Fault 5

00011 = Fault 4

00010 = Fault 3

00001 = Fault 2

00000 = Fault 1

bit 9 **CLPOL:** Current-Limit Polarity for PWMx Generator # bit⁽¹⁾

1 = The selected current-limit source is active-low

0 = The selected current-limit source is active-high

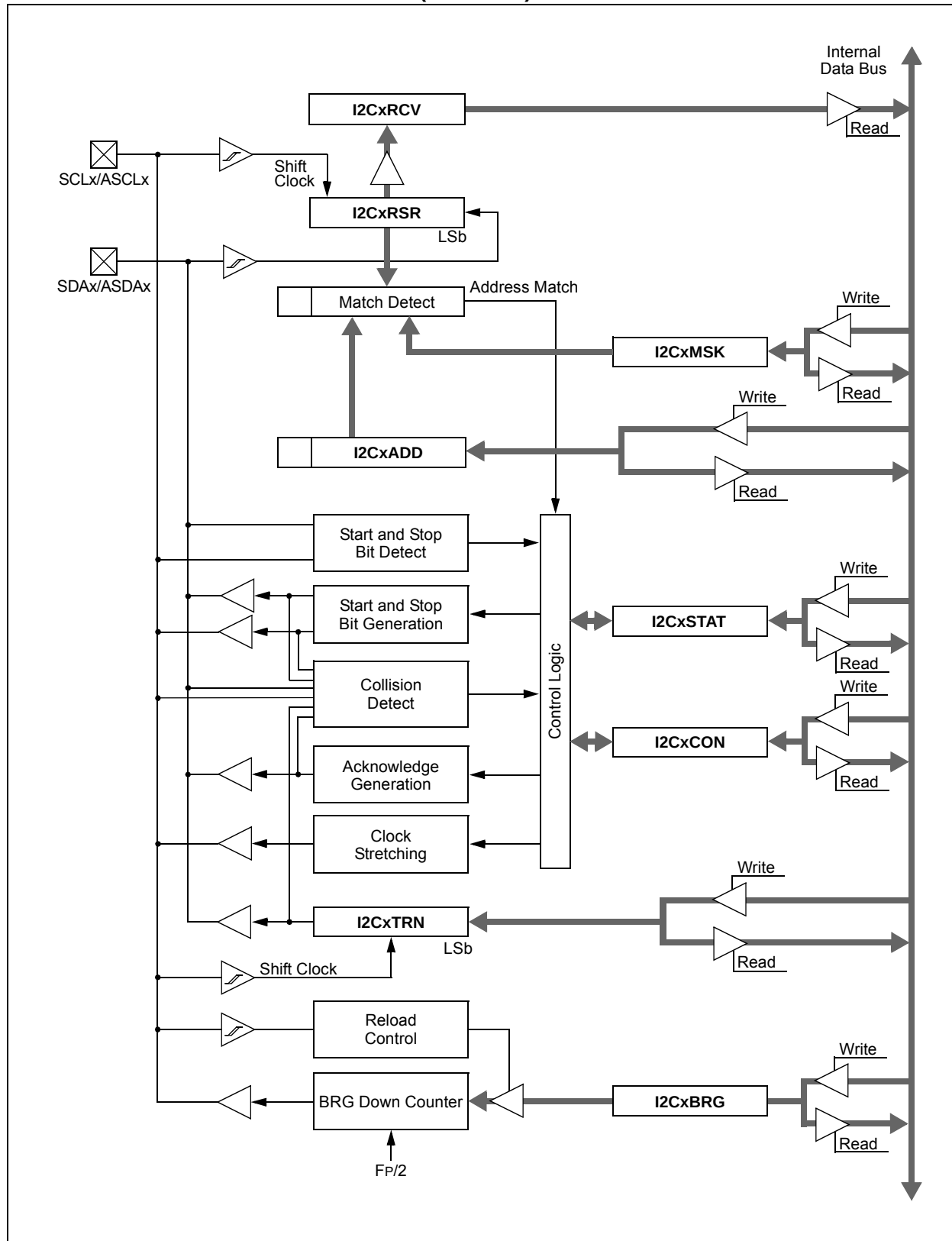
bit 8 **CLMOD:** Current-Limit Mode Enable for PWMx Generator # bit

1 = Current-Limit mode is enabled

0 = Current-Limit mode is disabled

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

FIGURE 19-1: I2Cx BLOCK DIAGRAM (x = 1 OR 2)



REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	AMSK<9:8>	
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AMSK<7:0>							
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10

Unimplemented: Read as '0'

bit 9-0

AMSK<9:0>: Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit, Ax, of incoming message address; bit match is not required in this position

0 = Disables masking for bit, Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK<6:0> only):

1 = Enables masking for bit, Ax + 1, of incoming message address; bit match is not required in this position

0 = Disables masking for bit, Ax + 1; bit match is required in this position

REGISTER 23-8: ADxCSSL: ADCx INPUT SCAN SELECT REGISTER LOW^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **CSS<15:0>**: ADCx Input Scan Selection bits

1 = Selects ANx for input scan

0 = Skips ANx for input scan

Note 1: On devices with less than 16 analog inputs, all bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

2: CSSx = ANx, where 'x' = 0-15.

27.3 RTCC Registers

REGISTER 27-1: RCFGAL: RTCC CALIBRATION AND CONFIGURATION REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
RTCEN ⁽²⁾	—	RTCWREN	RTCSYNC	HALFSEC ⁽³⁾	RTCOE	RTCPTR1	RTCPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **RTCEN:** RTCC Enable bit⁽²⁾
1 = RTCC module is enabled
0 = RTCC module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **RTCWREN:** RTCC Value Register Write Enable bit
1 = RTCVAL register can be written to by the user application
0 = RTCVAL register is locked out from being written to by the user application
- bit 12 **RTCSYNC:** RTCC Value Register Read Synchronization bit
1 = A rollover is about to occur in 32 clock edges (approximately 1 ms)
0 = A rollover will not occur
- bit 11 **HALFSEC:** Half-Second Status bit⁽³⁾
1 = Second half period of a second
0 = First half period of a second
- bit 10 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is disabled
- bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Pointer bits
Points to the corresponding RTCC Value register when reading the RTCVAL register; the RTCPTR<1:0> value decrements on every access of the RTCVAL register until it reaches '00'.
- bit 7-0 **CAL<7:0>:** RTCC Drift Calibration bits
01111111 = Maximum positive adjustment; adds 508 RTCC clock pulses every one minute
.
.
.
00000001 = Minimum positive adjustment; adds 4 RTCC clock pulses every one minute
00000000 = No adjustment
11111111 = Minimum negative adjustment; subtracts 4 RTCC clock pulses every one minute
.
.
.
10000000 = Maximum negative adjustment; subtracts 512 RTCC clock pulses every one minute

- Note 1:** The RCFGAL register is only affected by a POR.
2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
3: This bit is read-only. It is cleared when the lower half of the MINSEC register is written.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 27-9: ALRMVAL (WHEN ALRMPTR<1:0> = 01): ALARM WEEKDAY AND HOURS VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15						bit 8	

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-11 **Unimplemented:** Read as '0'
- bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.
- bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

29.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33/PIC24 Family Reference Manual”, “32-Bit Programmable Cyclic Redundancy Check (CRC)” (DS70346), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

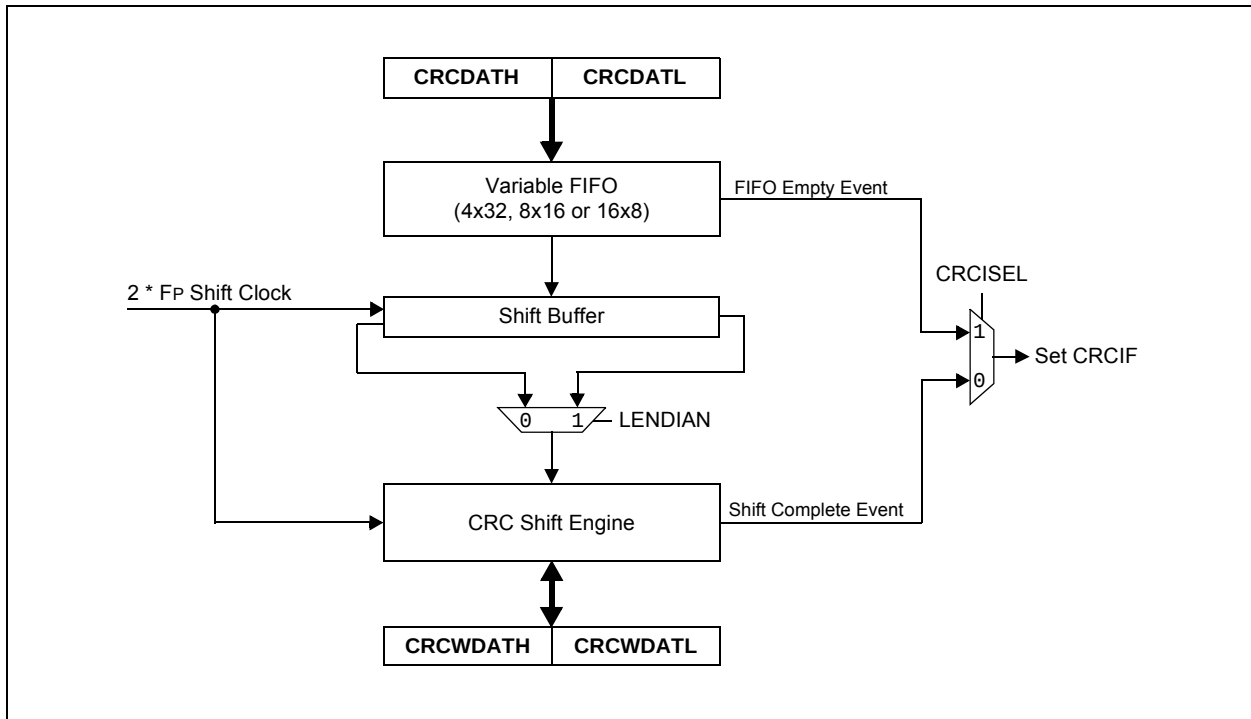
- User-Programmable (up to 32nd order) polynomial CRC equation
- Interrupt Output
- Data FIFO

The programmable CRC generator provides a hardware-implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 29-1. A simple version of the CRC shift engine is shown in Figure 29-2.

FIGURE 29-1: CRC BLOCK DIAGRAM



30.6 JTAG Interface

dsPIC33EPXXXGM3XX/6XX/7XX devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface is provided in future revisions of the document.

Note: Refer to the “dsPIC33/PIC24 Family Reference Manual”, “**Programming and Diagnostics**” (DS70608) for further information on usage, configuration and operation of the JTAG interface.

30.7 In-Circuit Serial Programming

The dsPIC33EPXXXGM3XX/6XX/7XX devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the “dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits” (DS70663) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

30.8 In-Circuit Debugger

When MPLAB® ICD 3 or the REAL ICE™ in-circuit emulator is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB X IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to MCLR, VDD, VSS and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins (PGECx and PGEDx).

30.9 Code Protection and CodeGuard™ Security

The dsPIC33EPXXXGM3XX/6XX/7XX devices offer basic implementation of CodeGuard Security that supports only General Segment (GS) security. This feature helps protect individual Intellectual Property.

Note: Refer to the “dsPIC33/PIC24 Family Reference Manual”, “**CodeGuard™ Security**” (DS70634) for further information on usage, configuration and operation of CodeGuard Security.

FIGURE 33-31: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

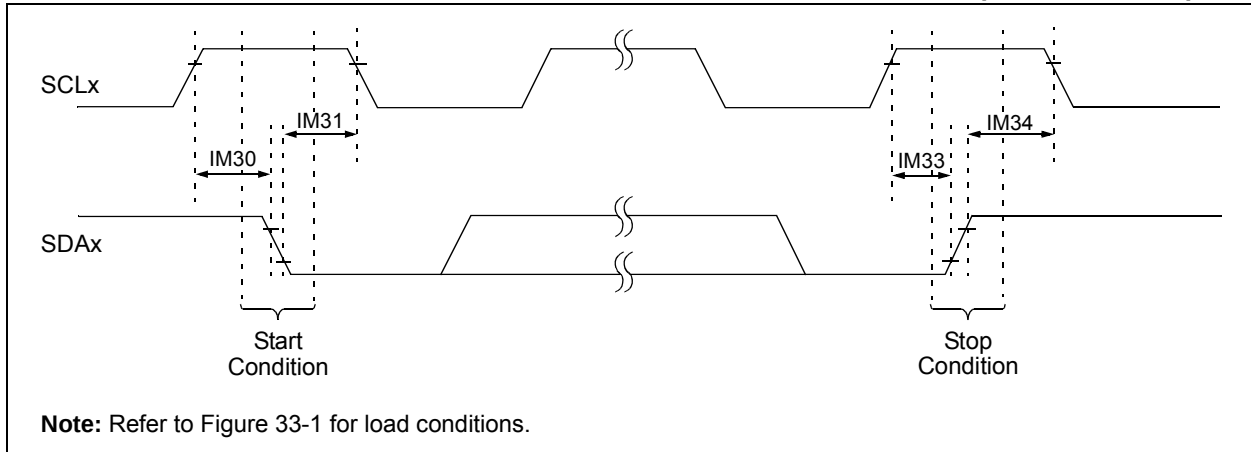
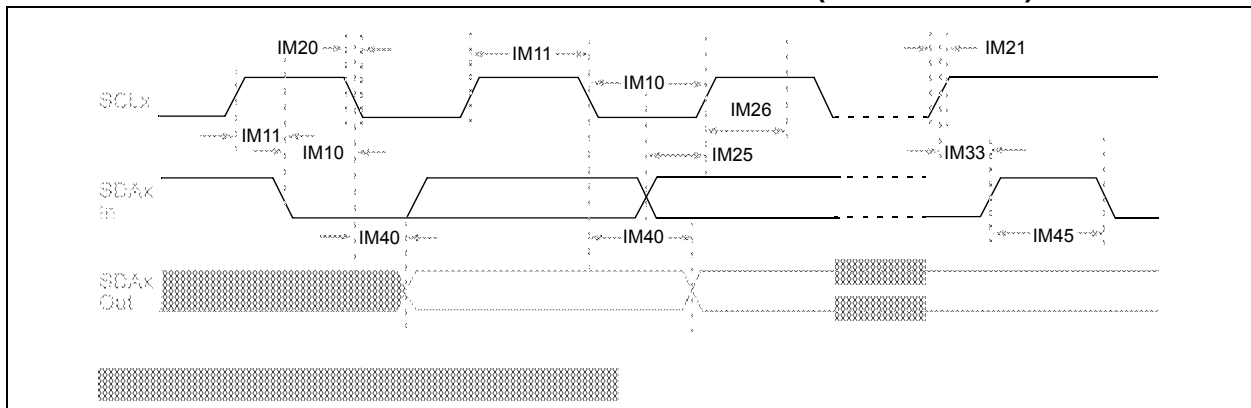


FIGURE 33-32: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 33-49: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	Symbol	Characteristic ⁽³⁾		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽¹⁾	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽¹⁾	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽¹⁾	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽¹⁾	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.25	—	μs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.25	—	μs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.6	—	μs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4	—	μs	
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.25	—	μs	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode ⁽¹⁾	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS50	CB	Bus Capacitive Loading		—	400	pF	
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	(Note 2)

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

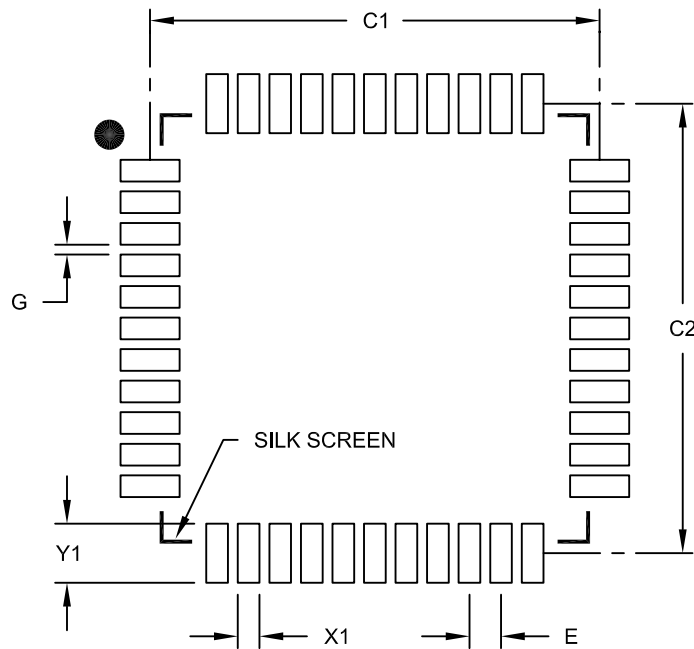
2: The Typical value for this parameter is 130 ns.

3: These parameters are characterized, but not tested in manufacturing.

dsPIC33EPXXXGM3XX/6XX/7XX

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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