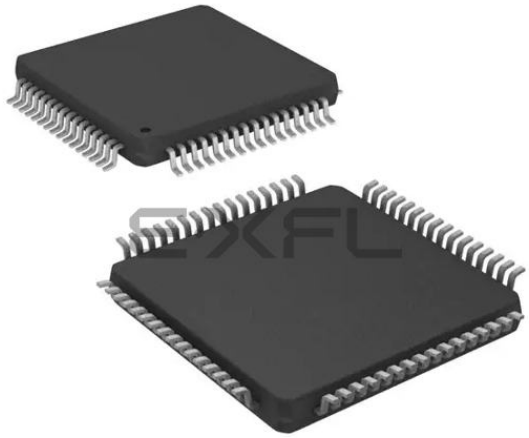

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	-
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 30x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm706-h-pt

Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com). These documents should be considered as the general reference for the operation of a particular module or device feature.

- **"Introduction"** (DS70573)
- **"CPU"** (DS70359)
- **"Data Memory"** (DS70595)
- **"Program Memory"** (DS70613)
- **"Flash Programming"** (DS70609)
- **"Interrupts"** (DS70000600)
- **"Oscillator"** (DS70580)
- **"Reset"** (DS70602)
- **"Watchdog Timer and Power-Saving Modes"** (DS70615)
- **"I/O Ports"** (DS70000598)
- **"Timers"** (DS70362)
- **"Input Capture"** (DS70000352)
- **"Output Compare"** (DS70005157)
- **"High-Speed PWM"** (DS70645)
- **"Quadrature Encoder Interface (QEI)"** (DS70601)
- **"Analog-to-Digital Converter (ADC)"** (DS70621)
- **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582)
- **"Serial Peripheral Interface (SPI)"** (DS70005185)
- **"Inter-Integrated Circuit™ (I^2C™)"** (DS70000195)
- **"Data Converter Interface (DCI) Module"** (DS70356)
- **"Enhanced Controller Area Network (ECAN™)"** (DS70353)
- **"Direct Memory Access (DMA)"** (DS70348)
- **"Programming and Diagnostics"** (DS70608)
- **"Op Amp/Comparator"** (DS70000357)
- **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS70346)
- **"Parallel Master Port (PMP)"** (DS70576)
- **"Device Configuration"** (DS70000618)
- **"Peripheral Trigger Generator (PTG)"** (DS70669)
- **"Charge Time Measurement Unit (CTMU)"** (DS70661)

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com)

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGM3XX/6XX/7XX family requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used)
  (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP
  (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

TABLE 4-6: OUTPUT COMPARE REGISTER MAP (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC7CON1	093C	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC7CON2	093E	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC7RS	0940	Output Compare 7 Secondary Register																xxxx
OC7R	0942	Output Compare 7 Register																xxxx
OC7TMR	0944	Output Compare 7 Timer Value Register																xxxx
OC8CON1	0946	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC8CON2	0948	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC8RS	094A	Output Compare 8 Secondary Register																xxxx
OC8R	094C	Output Compare 8 Register																xxxx
OC8TMR	094E	Output Compare 8 Timer Value Register																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-27: CAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 FOR dsPIC33EPXXXGM60X/7XX DEVICES(1)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0500-051E	See definition when WIN = x																
C2RXFUL1	0520	RXFUL<15:0>																0000
C2RXFUL2	0522	RXFUL<31:16>																0000
C2RXOVF1	0528	RXOVF<15:0>																0000
C2RXOVF2	052A	RXOVF<31:16>																0000
C2TR01CON	0530	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PRI1	TX1PRI0	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PRI1	TX0PRI0	0000
C2TR23CON	0532	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PRI1	TX3PRI0	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PRI1	TX2PRI0	0000
C2TR45CON	0534	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PRI1	TX5PRI0	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PRI1	TX4PRI0	0000
C2TR67CON	0536	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PRI1	TX7PRI0	TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PRI1	TX6PRI0	xxxx
C2RXD	0540	CAN2 Receive Data Word Register																xxxx
C2TXD	0542	CAN2 Transmit Data Word Register																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	**IPL3(2)**	SFA	RND	IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing latency is enabled
0 = Fixed exception processing latency is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see Register 3-2.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as '0'

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

bit 3 **U3MD:** UART3 Module Disable bit
1 = UART3 module is disabled
0 = UART3 module is enabled

bit 2 **I2C3MD:** I2C3 Module Disable bit
1 = I2C3 module is disabled
0 = I2C3 module is enabled

bit 1 **I2C2MD:** I2C2 Module Disable bit
1 = I2C2 module is disabled
0 = I2C2 module is enabled

bit 0 **ADC2MD:** ADC2 Module Disable bit
1 = ADC2 module is disabled
0 = ADC2 module is enabled

Note 1: The RTCCMD bit is not available on 44-pin devices.

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR<5:0>	Output Name
Default Port	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U2TX	000011	RPn tied to UART2 Transmit
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
$\overline{SS2}$	001010	RPn tied to SPI2 Slave Select
CSDO	001011	RPn tied to DCI Data Output
CSCK	001100	RPn tied to DCI Clock Output
COFS	001101	RPn tied to DCI Frame Sync
C1TX	001110	RPn tied to CAN1 Transmit
C2TX	001111	RPn tied to CAN2 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
OC5	010100	RPn tied to Output Compare 5 Output
OC6	010101	RPn tied to Output Compare 6 Output
OC7	010110	RPn tied to Output Compare 7 Output
OC8	010111	RPn tied to Output Compare 8 Output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
U3TX	011011	RPn tied to UART3 Transmit
$\overline{U3RTS}$	011100	RPn tied to UART3 Ready-to-Send
U4TX	011101	RPn tied to UART4 Transmit
$\overline{U4RTS}$	011110	RPn tied to UART4 Ready-to-Send
SDO3	011111	RPn tied to SPI3 Slave Output
SCK3	100000	RPn tied to SPI3 Clock Output
$\overline{SS3}$	100001	RPn tied to SPI3 Slave Select
SYNCO1	101101	RPn tied to PWM Primary Time Base Sync Output
SYNCO2	101110	RPn tied to PWM Secondary Time Base Sync Output
QEI1CCMP	101111	RPn tied to QEI1 Counter Comparator Output
QEI2CCMP	110000	RPn tied to QEI2 Counter Comparator Output
REFCLKO	110001	RPn tied to Reference Clock Output
C4OUT	110010	RPn tied to Comparator Output 4
C5OUT	110011	RPn tied to Comparator Output 5

REGISTER 11-6: RPINR9: PERIPHERAL PIN SELECT INPUT REGISTER 9

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC6R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC5R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **IC6R<6:0>:** Assign Input Capture 6 (IC6) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **IC5R<6:0>:** Assign Input Capture 5 (IC5) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

14.1 Input Capture Control Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture x Stop in Idle Mode Control bit
1 = Input Capture x halts in CPU Idle mode
0 = Input Capture x continues to operate in CPU Idle mode

bit 12-10 **ICTSEL<2:0>:** Input Capture x Timer Select bits
111 = Peripheral clock (FP) is the clock source of ICx
110 = Reserved
101 = Reserved
100 = T1CLK is the clock source of ICx (only the synchronous clock is supported)
011 = T5CLK is the clock source of ICx
010 = T4CLK is the clock source of ICx
001 = T2CLK is the clock source of ICx
000 = T3CLK is the clock source of ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits
(this field is not used if ICM<2:0> = 001 or 111)
11 = Interrupts on every fourth capture event
10 = Interrupts on every third capture event
01 = Interrupts on every second capture event
00 = Interrupts on every capture event

bit 4 **ICOV:** Input Capture x Overflow Status Flag bit (read-only)
1 = Input Capture x buffer overflow occurred
0 = No Input Capture x buffer overflow occurred

bit 3 **ICBNE:** Input Capture x Buffer Not Empty Status bit (read-only)
1 = Input Capture x buffer is not empty, at least one more capture value can be read
0 = Input Capture x buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture x Mode Select bits
111 = Input Capture x functions as an interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
110 = Unused (module disabled)
101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
011 = Capture mode, every rising edge (Simple Capture mode)
010 = Capture mode, every falling edge (Simple Capture mode)
001 = Capture mode, every edge, rising and falling (Edge Detect mode, ICI<1:0>), is not used in this mode)
000 = Input Capture x module is turned off

REGISTER 16-5: STCON: PWMx SECONDARY TIME BASE CONTROL REGISTER

U-0	U-0	U-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	SESTAT	SEIEN	EIPU(1)	SYNCPOL(1)	SYNCOEN(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN(1)	SYNCSRC2(1)	SYNCSRC1(1)	SYNCSRC0(1)	SEVTPS3(1)	SEVTPS2(1)	SEVTPS1(1)	SEVTPS0(1)
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit(1)
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWM cycle boundaries

bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit(1)
1 = SYNCI2/SYNCO2 polarity is inverted (active-low)
0 = SYNCI2/SYNCO2 is active-high

bit 8 **SYNCOEN:** Primary Time Base Sync Enable bit(1)
1 = SYNCO2 output is enabled
0 = SYNCO2 output is disabled

bit 7 **SYNCEN:** External Time Base Synchronization Enable bit(1)
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

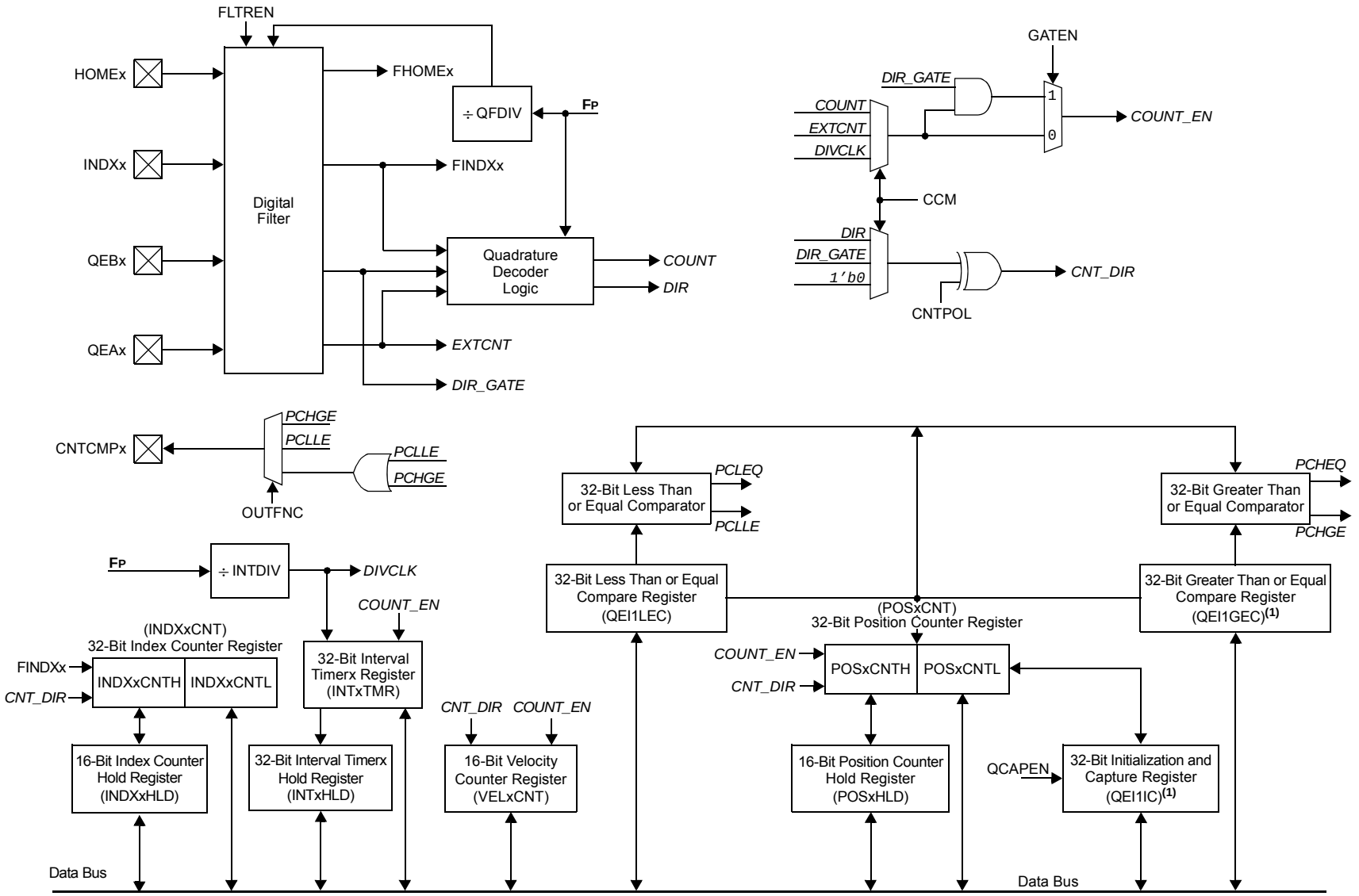
bit 6-4 **SYNCSRC<2:0>:** Synchronous Source Selection bits(1)
111 = Reserved
•
•
•
100 = Reserved
011 = PTGO17(2)
010 = PTGO16(2)
001 = Reserved
000 = SYNCI1

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

2: See **Section 25.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.

NOTES:

FIGURE 17-1: QEIx BLOCK DIAGRAM



Note 1: These registers map to the same memory location.

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected

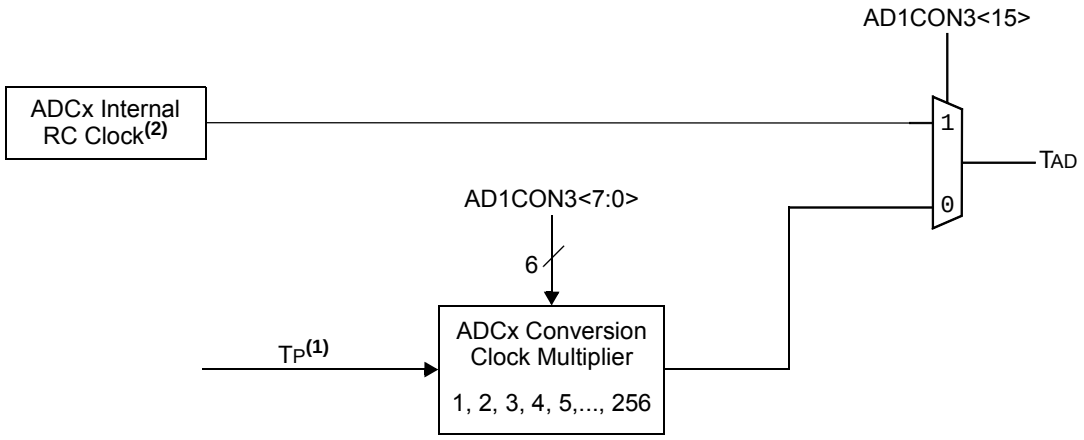
bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receive buffer and the UxRSR to the empty state

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Note 1: Refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) for information on enabling the UART module for transmit operation.

FIGURE 23-2: ADCx CONVERSION CLOCK PERIOD BLOCK DIAGRAM



Note 1: TP = 1/FP.

2: See the ADCx electrical specifications in **Section 33.0 "Electrical Characteristics"** for the exact RC clock value.

REGISTER 23-7: ADxCSSH: ADCx INPUT SCAN SELECT REGISTER HIGH(2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS31	CSS30	CSS29	CSS28	CSS27	CSS26(1)	CSS25(1)	CSS24(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS23	CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CSS31:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 14 **CSS30:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 13 **CSS29:** ADCx Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 12 **CSS28:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 11 **CSS27:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 10 **CSS26:** ADCx Input Scan Selection bit(1)
1 = Selects OA3/AN6 for input scan
0 = Skips OA3/AN6 for input scan

bit 9 **CSS25:** ADCx Input Scan Selection bit(1)
1 = Selects OA2/AN0 for input scan
0 = Skips OA2/AN0 for input scan

bit 8 **CSS24:** ADCx Input Scan Selection bit(1)
1 = Selects OA1/AN3 for input scan
0 = Skips OA1/AN3 for input scan

bit 7 **CSS23:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 6 **CSS22:** ADCx Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 5 **CSS21:** ADCx Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

Note 1: If the op amp is selected (OPMODE bit (CMxCON<10>) = 1), the OAx input is used; otherwise, the ANx input is used.

2: All bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

REGISTER 25-2: PTGCON: PTG CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-13 **PTGCLK<2:0>:** Select PTG Module Clock Source bits
111 = Reserved
110 = Reserved
101 = PTG module clock source will be T3CLK
100 = PTG module clock source will be T2CLK
011 = PTG module clock source will be T1CLK
010 = PTG module clock source will be TAD
001 = PTG module clock source will be FOSC
000 = PTG module clock source will be FP

bit 12-8 **PTGDIV<4:0>:** PTG Module Clock Prescaler (divider) bits
11111 = Divide-by-32
11110 = Divide-by-31
•
•
•
00001 = Divide-by-2
00000 = Divide-by-1

bit 7-4 **PTGPWD<3:0>:** PTG Trigger Output Pulse-Width bits
1111 = All trigger outputs are 16 PTG clock cycles wide
1110 = All trigger outputs are 15 PTG clock cycles wide
•
•
•
0001 = All trigger outputs are 2 PTG clock cycles wide
0000 = All trigger outputs are 1 PTG clock cycle wide

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **PTGWDT<2:0>:** Select PTG Watchdog Timer Time-out Count Value bits
111 = Watchdog Timer will time-out after 512 PTG clocks
110 = Watchdog Timer will time-out after 256 PTG clocks
101 = Watchdog Timer will time-out after 128 PTG clocks
100 = Watchdog Timer will time-out after 64 PTG clocks
011 = Watchdog Timer will time-out after 32 PTG clocks
010 = Watchdog Timer will time-out after 16 PTG clocks
001 = Watchdog Timer will time-out after 8 PTG clocks
000 = Watchdog Timer is disabled

TABLE 33-21: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SY00	TPU	Power-up Period	—	400	600	µs	
SY10	TOST	Oscillator Start-up Time	—	1024 TOSC	—	—	TOSC = OSC1 period
SY12	TWDT	Watchdog Timer Time-out Period	0.85	—	1.15	ms	WDTPRE = 0, WDTPOST<3:0> = 0000, Using LPRC tolerances indicated in F21 (see Table 33-19) at +85°C
			3.4	—	4.6	ms	WDTPRE = 1, WDTPOST<3:0> = 0000, Using LPRC tolerances indicated in F21 (see Table 33-19) at +85°C
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	µs	
SY20	TMCLR	MCLR Pulse Width (low)	2	—	—	µs	
SY30	TBOR	BOR Pulse Width (low)	1	—	—	µs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	µs	-40°C to +85°C
SY36	TVREG	Voltage Regulator Standby-to-Active Mode Transition Time	—	—	30	µs	
SY37	TOSCDFRC	FRC Oscillator Start-up Delay	—	—	29	µs	
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	—	—	70	µs	

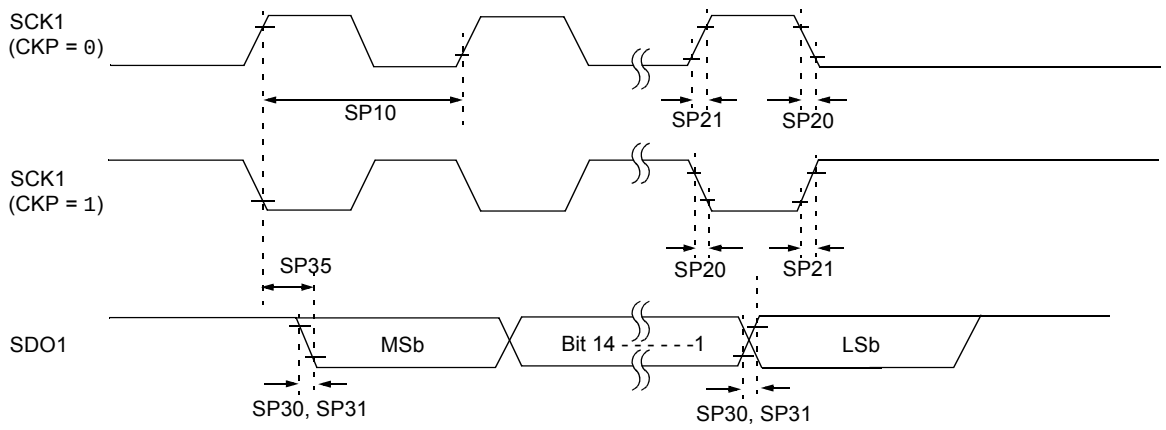
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

TABLE 33-40: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	**Master Transmit Only (Half-Duplex)**	**Master Transmit/Receive (Full-Duplex)**	**Slave Transmit/Receive (Full-Duplex)**	**CKE**	**CKP**	**SMP**
25 MHz	Table 33-41	—	—	0,1	0,1	0,1
25 MHz	—	Table 33-42	—	1	0,1	1
25 MHz	—	Table 33-43	—	0	0,1	1
25 MHz	—	—	Table 33-44	1	0	0
25 MHz	—	—	Table 33-45	1	1	0
25 MHz	—	—	Table 33-46	0	1	0
25 MHz	—	—	Table 33-47	0	0	0

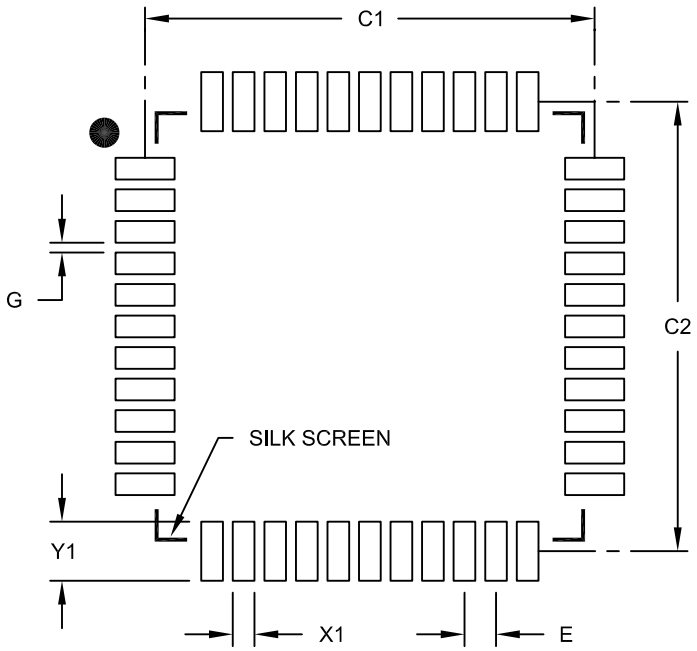
FIGURE 33-23: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 33-1 for load conditions.

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B