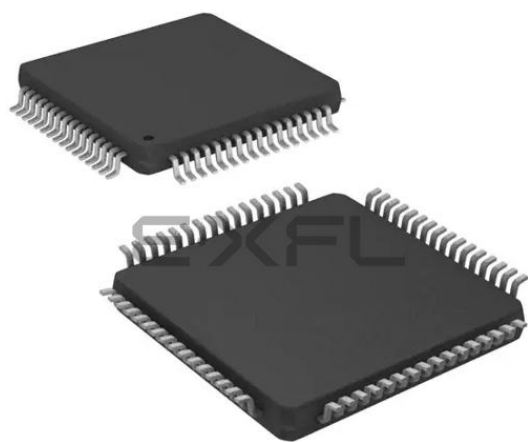




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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 30x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm706-i-pt

dsPIC33EPXXXGM3XX/6XX/7XX

dsPIC33EPXXXGM3XX/6XX/7XX PRODUCT FAMILY

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. Their pinout diagrams appear on the following pages.

TABLE 1: dsPIC33EPXXXGM3XX/6XX/7XX FAMILY DEVICES

Device	Program Flash Memory (Kbytes)	RAM (Kbytes)	Remappable Peripherals									I ² C™	CRC Generator	ADC	10-Bit/12-Bit ADC (Channels)	Op Amps/Comparators	CTMU	PTG	PMP	RTCC	I/O Pins	Pins	Packages	
			CAN	16-Bit/32-Bit Timers	Input Capture	Output Compare	Motor Control PWM (Channels)	QEI	UART	SPI ⁽¹⁾	DCI													External Interrupts ⁽²⁾
dsPIC33EP128GM304	128	16	0	9/4	8	8	12	2	4	3	1	5	2	1	2	18	4/5	1	Yes	No	No	35	44	TQFP, QFN
dsPIC33EP128GM604			2																					
dsPIC33EP256GM304	256	32	0																					
dsPIC33EP256GM604			2																					
dsPIC33EP512GM304	512	48	0	9/4	8	8	12	2	4	3	1	5	2	1	2	30	4/5	1	Yes	Yes	Yes	53	64	TQFP, QFN
dsPIC33EP512GM604			2																					
dsPIC33EP128GM306	128	16	0																					
dsPIC33EP128GM706			2																					
dsPIC33EP256GM306	256	32	0	9/4	8	8	12	2	4	3	1	5	2	1	2	49	4/5	1	Yes	Yes	Yes	85	100/121	TQFP, TFBGA
dsPIC33EP256GM706			2																					
dsPIC33EP512GM306	512	48	0																					
dsPIC33EP512GM706			2																					
dsPIC33EP128GM310	128	16	0	9/4	8	8	12	2	4	3	1	5	2	1	2	49	4/5	1	Yes	Yes	Yes	85	100/121	TQFP, TFBGA
dsPIC33EP128GM710			2																					
dsPIC33EP256GM310	256	32	0																					
dsPIC33EP256GM710			2																					
dsPIC33EP512GM310	512	48	0	9/4	8	8	12	2	4	3	1	5	2	1	2	49	4/5	1	Yes	Yes	Yes	85	100/121	TQFP, TFBGA
dsPIC33EP512GM710			2																					

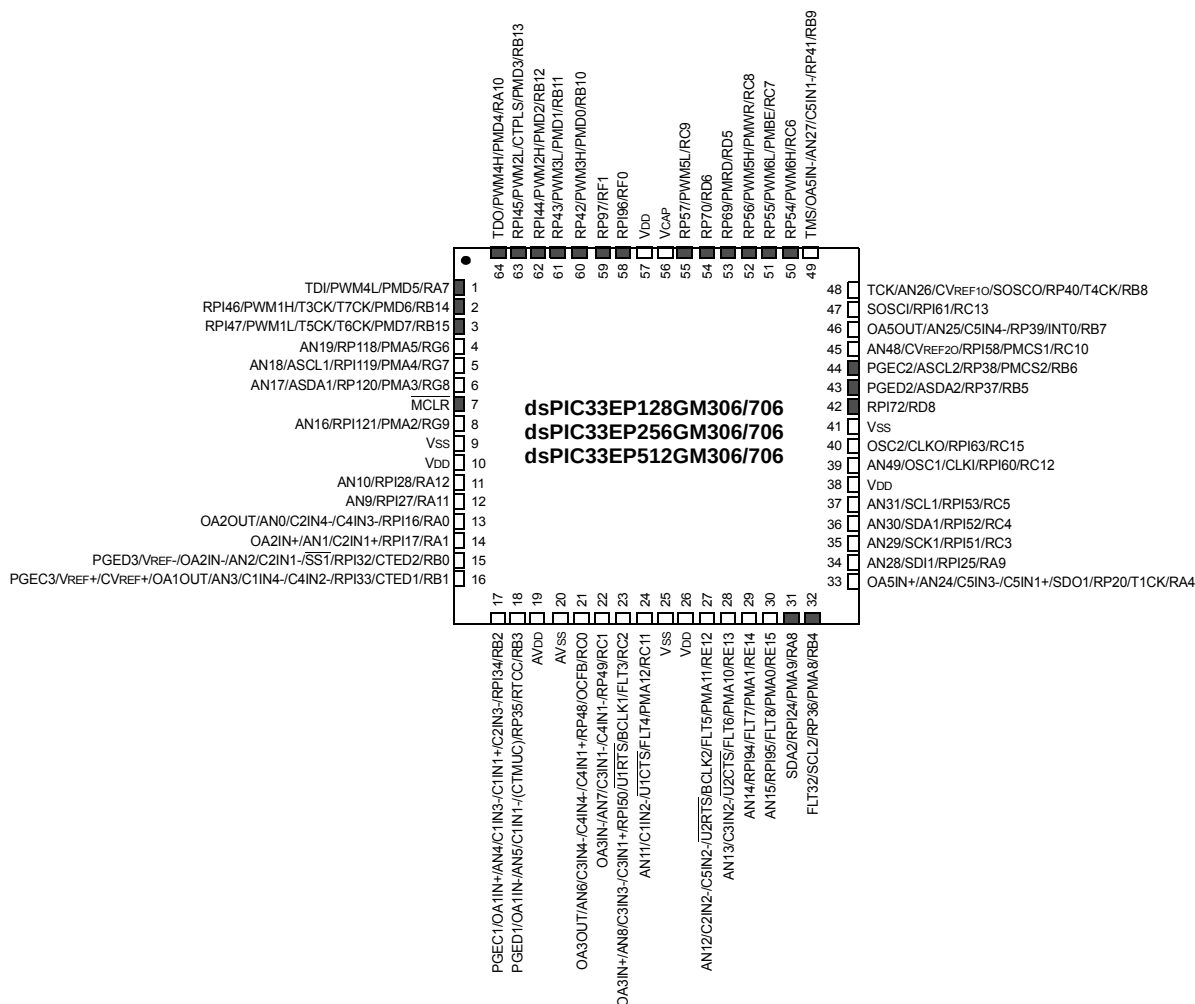
Note 1: Only SPI2 and SPI3 are remappable.
2: INT0 is not remappable.

dsPIC33EPXXXGM3XX/6XX/7XX

Pin Diagrams (Continued)

64-Pin QFN^(1,2,3,4)

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
 - 3: This pin is not available as an input when OPMODE (CMxCON<10>) = 1.
 - 4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
U1CTS	I	ST	Yes	UART1 Clear-to-Send.
U1RTS	O	—	Yes	UART1 Ready-to-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
U2CTS	I	ST	Yes	UART2 Clear-to-Send.
U2RTS	O	—	Yes	UART2 Ready-to-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
U3CTS	I	ST	Yes	UART3 Clear-to-Send.
U3RTS	O	—	Yes	UART3 Ready-to-Send.
U3RX	I	ST	Yes	UART3 receive.
U3TX	O	—	Yes	UART3 transmit.
U4CTS	I	ST	Yes	UART4 Clear-to-Send.
U4RTS	O	—	Yes	UART4 Ready-to-Send.
U4RX	I	ST	Yes	UART4 receive.
U4TX	O	—	Yes	UART4 transmit.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCK3	I/O	ST	Yes	Synchronous serial clock input/output for SPI3.
SDI3	I	ST	Yes	SPI3 data in.
SDO3	O	—	Yes	SPI3 data out.
SS3	I/O	ST	Yes	SPI3 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

- Note 1:** This pin is not available on all devices. For more information, see the “Pin Diagrams” section for pin availability.
- 2:** AVDD must be connected at all times.

FIGURE 2-7: INTERLEAVED PFC

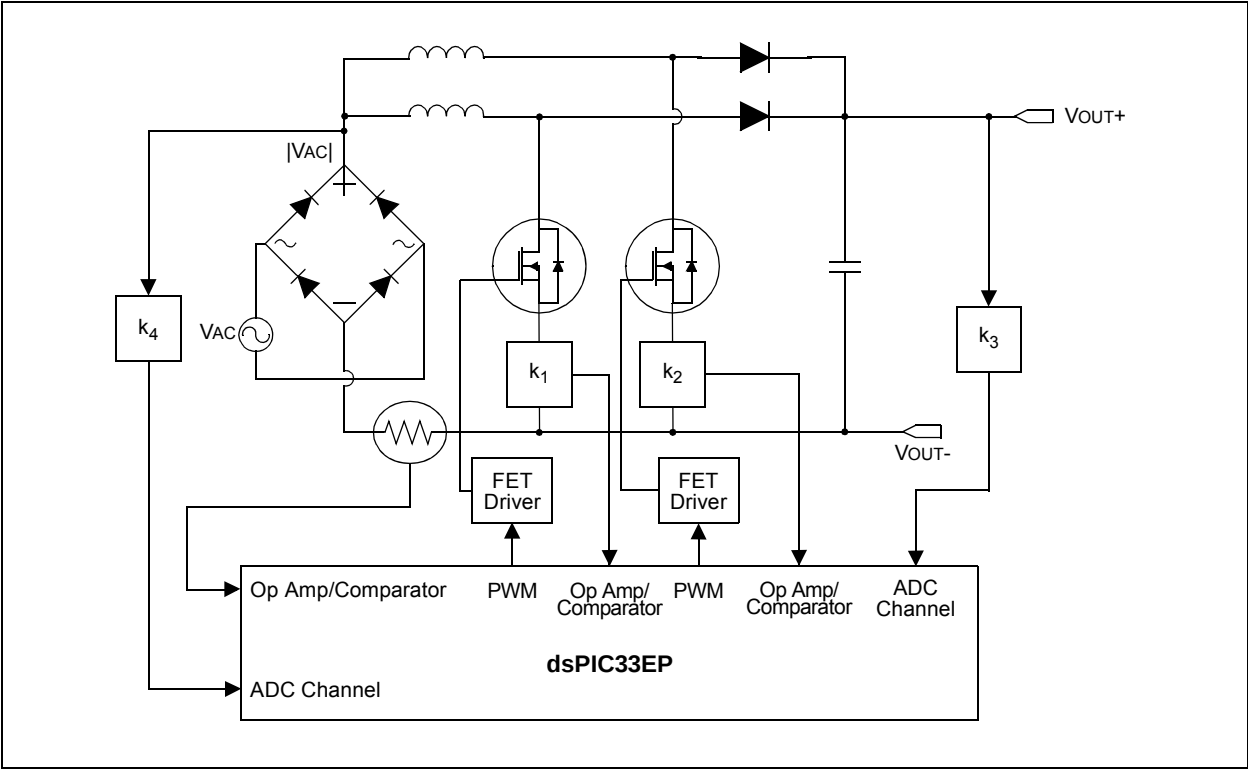


FIGURE 2-8: BEMF VOLTAGE MEASURED USING THE ADC MODULE

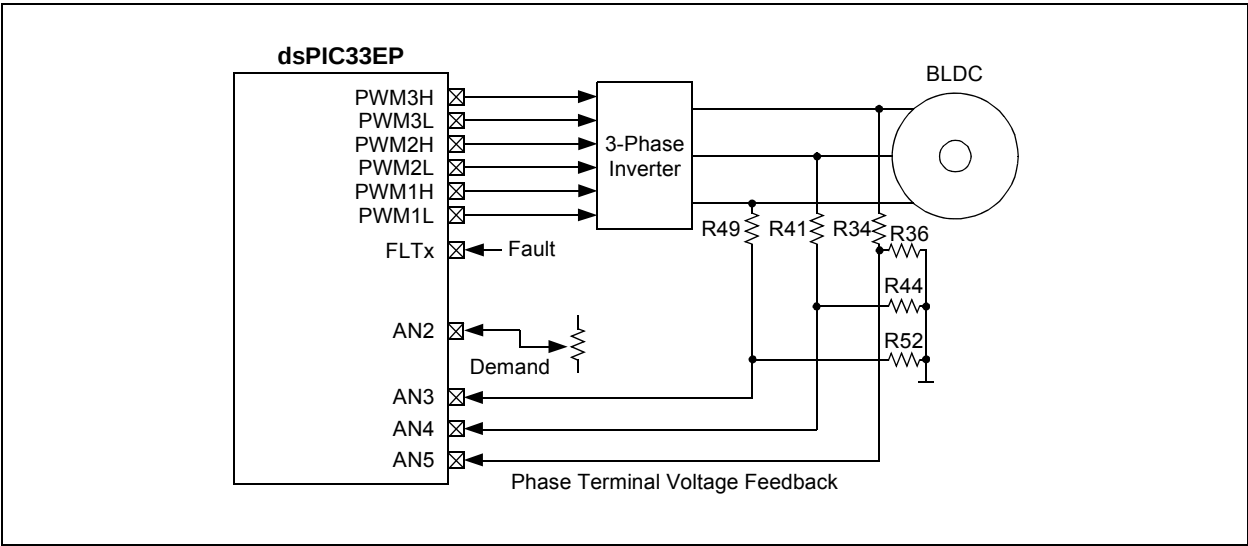




TABLE 4-41: OP AMP/COMPARATOR REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	PSIDL	—	—	C5EVT	C4EVT	C3EVT	C2EVT	C1EVT	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT	0000
CVR1CON	0A82	—	—	—	—	CVRR1	VREFSEL	—	—	CVREN	CVROE	CVRR0	CVRSS	CVR3	CVR2	CVR1	CVR0	0000
CM1CON	0A84	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM1MSKSR	0A86	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM2CON	0A8C	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM2MSKSR	0A8E	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM3CON	0A94	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM3MSKSR	0A96	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM3MSKCON	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR	0A9A	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM4CON	0A9C	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM4MSKSR	0A9E	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM4MSKCON	0AA0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM4FLTR	0AA2	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM5CON	0AA4	CON	COE	CPOL	—	—	OPMODE	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM5MSKSR	0AA6	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM5MSKCON	0AA8	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM5FLTR	0AAA	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CVR2CON	0AB4	—	—	—	—	CVRR1	VREFSEL	—	—	CVREN	CVROE	CVRR0	CVRSS	CVR3	CVR2	CVR1	CVR0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-42: CTMU REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON1	033A	CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	—	—	—	—	—	—	0000
CTMUCON2	033C	EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—	0000
CTMUICON	033E	ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-43: JTAG INTERFACE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
JDATAH	0FF0	—	—	—	—	JDATAH<27:16>												xxxx
JDATAL	0FF2	JDATAL<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-44: REAL-TIME CLOCK AND CALENDAR REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ALRMVAL	0620	Alarm Value Register Window Based on ALRMPTR<1:0>																xxxx
ALCFGRPT	0622	ALRMEN	CHIME	AMASK3	AMASK2	AMASK1	AMASK0	ALRMPTR1	ALRMPTR0	ARPT7	ARPT6	ARPT5	ARPT4	ARPT3	ARPT2	ARPT1	ARPT0	0000
RTCVAL	0624	RTCC Value Register Window Based on RTCPTR<1:0>																xxxx
RCFGCAL	0626	RTCEN	—	RTCWREN	RTCSYNC	HALFSEC	RTCOE	RTCPTTR1	RTCPTTR0	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-52: PORTC REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	TRISC15	—	TRISC<13:0>														BFFF
PORTC	0E22	RC15	—	RC<13:0>														xxxx
LATC	0E24	LATC15	—	LATC<13:0>														xxxx
ODCC	0E26	ODCC15	—	ODCC<13:0>														0000
CNENC	0E28	CNIEC15	—	CNIEC<13:0>														0000
CNPUC	0E2A	CNPUC15	—	CNPUC<13:0>														0000
CNPDC	0E2C	CNPDC15	—	CNPDC<13:0>														0000
ANSEL	0E2E	—	—	—	ANSC<12:10>			—	—	—	—	ANSC<5:0>						0807

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-53: PORTC REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	TRISC15	—	TRISC<13:0>														BFFF
PORTC	0E22	RC15	—	RC<13:0>														xxxx
LATC	0E24	LATC15	—	LATC<13:0>														xxxx
ODCC	0E26	ODCC15	—	ODCC<13:0>														0000
CNENC	0E28	CNIEC15	—	CNIEC<13:0>														0000
CNPUC	0E2A	CNPUC15	—	CNPUC<13:0>														0000
CNPDC	0E2C	CNPDC15	—	CNPDC<13:0>														0000
ANSEL	0E2E	—	—	—				—	—	—	—	ANSC<5:0>						0807

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: PORTC REGISTER MAP FOR dsPIC33EPXXXGM304/604 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E20	—	—	—	—	—	—	TRISC<9:0>										BFFF
PORTC	0E22	—	—	—	—	—	—	RC<9:0>										xxxx
LATC	0E24	—	—	—	—	—	—	LATC<9:0>										xxxx
ODCC	0E26	—	—	—	—	—	—	ODCC<9:0>										0000
CNENC	0E28	—	—	—	—	—	—	CNIEC<9:0>										0000
CNPUC	0E2A	—	—	—	—	—	—	CNPUC<9:0>										0000
CNPDC	0E2C	—	—	—	—	—	—	CNPDC<9>										0000
ANSEL	0E2E	—	—	—	—	—	—	—	—	—	—	ANSC<5:0>						0807

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **TRAPR:** Trap Reset Flag bit
 1 = A Trap Conflict Reset has occurred
 0 = A Trap Conflict Reset has not occurred
- bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
 1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
 0 = An illegal opcode or Uninitialized W Register Reset has not occurred
- bit 13-12 **Unimplemented:** Read as '0'
- bit 11 **VREGSF:** Flash Voltage Regulator Standby During Sleep bit
 1 = Flash Voltage regulator is active during Sleep
 0 = Flash Voltage regulator goes into Standby mode during Sleep
- bit 10 **Unimplemented:** Read as '0'
- bit 9 **CM:** Configuration Mismatch Flag bit
 1 = A Configuration Mismatch Reset has occurred.
 0 = A Configuration Mismatch Reset has NOT occurred
- bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
 1 = Voltage regulator is active during Sleep
 0 = Voltage regulator goes into Standby mode during Sleep
- bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
 1 = A Master Clear (pin) Reset has occurred
 0 = A Master Clear (pin) Reset has not occurred
- bit 6 **SWR:** Software RESET (Instruction) Flag bit
 1 = A RESET instruction has been executed
 0 = A RESET instruction has not been executed
- bit 5 **SWDTEN:** Software Enable/Disable of WDT bit⁽²⁾
 1 = WDT is enabled
 0 = WDT is disabled
- bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
 1 = WDT time-out has occurred
 0 = WDT time-out has not occurred

- Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T5MD	T4MD	T3MD	T2MD	T1MD	QE11MD	PWMMD	DC1MD
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD ⁽¹⁾	C1MD ⁽¹⁾	AD1MD
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **T5MD:** Timer5 Module Disable bit
1 = Timer5 module is disabled
0 = Timer5 module is enabled
- bit 14 **T4MD:** Timer4 Module Disable bit
1 = Timer4 module is disabled
0 = Timer4 module is enabled
- bit 13 **T3MD:** Timer3 Module Disable bit
1 = Timer3 module is disabled
0 = Timer3 module is enabled
- bit 12 **T2MD:** Timer2 Module Disable bit
1 = Timer2 module is disabled
0 = Timer2 module is enabled
- bit 11 **T1MD:** Timer1 Module Disable bit
1 = Timer1 module is disabled
0 = Timer1 module is enabled
- bit 10 **QE11MD:** QE11 Module Disable bit
1 = QE11 module is disabled
0 = QE11 module is enabled
- bit 9 **PWMMD:** PWM Module Disable bit
1 = PWM module is disabled
0 = PWM module is enabled
- bit 8 **DC1MD:** DC1 Module Disable bit
1 = DC1 module is disabled
0 = DC1 module is enabled
- bit 7 **I2C1MD:** I2C1 Module Disable bit
1 = I2C1 module is disabled
0 = I2C1 module is enabled
- bit 6 **U2MD:** UART2 Module Disable bit
1 = UART2 module is disabled
0 = UART2 module is enabled
- bit 5 **U1MD:** UART1 Module Disable bit
1 = UART1 module is disabled
0 = UART1 module is enabled

Note 1: These bits are available on dsPIC33EPXXXGM6XX/7XX devices only.

16.0 HIGH-SPEED PWM MODULE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33/PIC24 Family Reference Manual”, “High-Speed PWM” (DS70645), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX devices support a dedicated Pulse-Width Modulation (PWM) module with up to 12 outputs.

The high-speed PWMx module consists of the following major features:

- Six PWM generators
- Two PWM outputs per PWM generator
- Individual period and duty cycle for each PWM pair
- Duty cycle, dead time, phase shift and a frequency resolution of 7.14 ns
- Independent Fault and current-limit inputs for six PWM outputs
- Redundant output
- Center-Aligned PWM mode
- Output override control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for input clock
- PWMxL and PWMxH output pin swapping
- Independent PWM frequency, duty cycle and phase-shift changes for each PWM generator
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB) functionality
- Frequency resolution enhancement
- PWM capture functionality

Note: In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 7.14 ns.

The high-speed PWMx module contains up to six PWM generators. Each PWMx generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known “safe” state.

Each PWMx can generate a trigger to the ADCx module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADCx module, based on either of the two master time bases.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNC11 and SYNC12 input pins that utilize PPS, can synchronize the high-speed PWMx module with an external signal. The SYNCO1 and SYNCO2 pins are output pins that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

16.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs, which include FLT1 and FLT2. The inputs are remappable using the PPS feature. FLT3 is available on 44-pin, 64-pin and 100-pin packages; FLT4 through FLT8 are available on specific pins on 64-pin and 100-pin packages, and FLT32, which has been implemented with Class B safety features, and is available on a fixed pin on all devices.

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

16.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the high-speed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled high externally or the internal pull-up resistor in the CNPUX register can be enabled.

Note: The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCONx<1:0>), regardless of the state of FLT32.

REGISTER 16-19: IOCONx: PWMx I/O CONTROL REGISTER⁽²⁾ (CONTINUED)

- bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
 1 = PWMxH output signal is connected to the PWMxL pins; PWMxL output signal is connected to the PWMxH pins
 0 = PWMxH and PWMxL pins are mapped to their respective pins
- bit 0 **OSYNC:** Output Override Synchronization bit
 1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWM time base
 0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).

2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 16-20: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **TRGCMP<15:0>:** Trigger Control Value bits

When the primary PWMx functions in the local time base, this register contains the compare values that can trigger the ADCx module.

24.2 DCI Control Registers

REGISTER 24-1: DCICON1: DCI CONTROL REGISTER 1

R/W-0	r-0	R/W-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0
DCIEN	r	DCISIDL	r	DLOOP	CCKD	CCKE	COFSD
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	r-0	r-0	r-0	R/W-0	R/W-0
UNFM	CSDOM	DJST	r	r	r	COFSM1	COFSM0
bit 7				bit 0			

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **DCIEN:** DCI Module Enable bit
1 = DCI module is enabled
0 = DCI module is disabled
- bit 14 **Reserved:** Read as '0'
- bit 13 **DCISIDL:** DCI Stop in Idle Control bit
1 = Module will halt in CPU Idle mode
0 = Module will continue to operate in CPU Idle mode
- bit 12 **Reserved:** Read as '0'
- bit 11 **DLOOP:** Digital Loopback Mode Control bit
1 = Digital Loopback mode is enabled; CSDI and CSDO pins are internally connected
0 = Digital Loopback mode is disabled
- bit 10 **CCKD:** Sample Clock Direction Control bit
1 = CCK pin is an input when DCI module is enabled
0 = CCK pin is an output when DCI module is enabled
- bit 9 **CCKE:** Sample Clock Edge Control bit
1 = Data changes on serial clock falling edge, sampled on serial clock rising edge
0 = Data changes on serial clock rising edge, sampled on serial clock falling edge
- bit 8 **COFSD:** Frame Synchronization Direction Control bit
1 = COFS pin is an input when DCI module is enabled
0 = COFS pin is an output when DCI module is enabled
- bit 7 **UNFM:** Underflow Mode bit
1 = Transmits last value written to the Transmit registers on a transmit underflow
0 = Transmits '0's on a transmit underflow
- bit 6 **CSDOM:** Serial Data Output Mode bit
1 = CSDO pin will be tri-stated during disabled transmit time slots
0 = CSDO pin drives '0's during disabled transmit time slots
- bit 5 **DJST:** DCI Data Justification Control bit
1 = Data transmission/reception is begun during the same serial clock cycle as the frame synchronization pulse
0 = Data transmission/reception is begun one serial clock cycle after the frame synchronization pulse
- bit 4-2 **Reserved:** Read as '0'
- bit 1-0 **COFSM<1:0>:** Frame Sync Mode bits
11 = 20-Bit AC-Link mode
10 = 16-Bit AC-Link mode
01 = I²S Frame Sync mode
00 = Multi-Channel Frame Sync mode

REGISTER 26-3: CM4CON: OP AMP/COMPARATOR 4 CONTROL REGISTER (CONTINUED)

- bit 7-6 **EVPOL<1:0>**: Trigger/Event/Interrupt Polarity Select bits⁽²⁾
- 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
 - 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
 - If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.
 - If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output.
 - 01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)
 - If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.
 - If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output.
 - 00 = Trigger/event/interrupt generation is disabled
- bit 5 **Unimplemented**: Read as '0'
- bit 4 **CREF**: Comparator Reference Select bit (VIN+ input)⁽¹⁾
- 1 = VIN+ input connects to internal CVREFIN voltage
 - 0 = VIN+ input connects to C4IN1+ pin
- bit 3-2 **Unimplemented**: Read as '0'
- bit 1-0 **CCH<1:0>**: Comparator Channel Select bits⁽¹⁾
- 11 = VIN- input of comparator connects to OA3/AN6
 - 10 = VIN- input of comparator connects to OA2/AN0
 - 01 = VIN- input of comparator connects to OA1/AN3
 - 00 = VIN- input of comparator connects to C4IN1-

- Note 1:** Inputs that are selected and not available will be tied to VSS. See the “Pin Diagrams” section for available inputs for each package.
- 2:** After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the Comparator Event bit, CEVT (CMxCON<9>), and the Comparator Combined Interrupt Flag, CMPIF (IFS1<2>), **must be cleared** before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

NOTES:

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28.1 PMP Control Registers

REGISTER 28-1: PMCON: PARALLEL MASTER PORT CONTROL REGISTER⁽³⁾

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0 ⁽¹⁾	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP	CS2P	CS1P	BEP	WRSP	RDSP
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at Reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **PMPEN:** Parallel Master Port Enable bit
 1 = PMP module is enabled
 0 = PMP module is disabled, no off-chip access is performed
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **PSIDL:** PMP Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
 11 = Reserved
 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
 01 = Lower eight bits of address are multiplexed on PMD<7:0> pins, upper eight bits are on PMA<15:8>
 00 = Address and data appear on separate pins
- bit 10 **PTBEEN:** Byte Enable Port Enable bit (16-Bit Master mode)
 1 = PMBE port is enabled
 0 = PMBE port is disabled
- bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
 1 = PMWR/PMENB port is enabled
 0 = PMWR/PMENB port is disabled
- bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
 1 = PMRD/PMWR port is enabled
 0 = PMRD/PMWR port is disabled
- bit 7-6 **CSF<1:0>:** Chip Select Function bits
 11 = Reserved
 10 = PMCS1 and PMCS2 function as Chip Select
 01 = PMCS2 functions as Chip Select, PMCS1 functions as Address Bit 14
 00 = PMCS1 and PMCS2 function as Address Bits 15 and 14
- bit 5 **ALP:** Address Latch Polarity bit⁽¹⁾
 1 = Active-high (PMALL and PMALH)
 0 = Active-low (PMALL and PMALH)
- bit 4 **CS2P:** Chip Select 1 Polarity bit⁽¹⁾
 1 = Active-high (PMCS2)
 0 = Active-low (PMCS2)

- Note 1:** These bits have no effect when their corresponding pins are used as address lines.
2: PMCS1 applies to Master mode and PMCS applies to Slave mode.
3: This register is not available on 44-pin devices.

TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
46	MOV	MOV f, Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV f, WREG	Move f to WREG	1	1	None
		MOV #lit16, Wn	Move 16-bit literal to Wn	1	1	None
		MOV.b #lit8, Wn	Move 8-bit literal to Wn	1	1	None
		MOV Wn, f	Move Wn to f	1	1	None
		MOV Wso, Wdo	Move Ws to Wd	1	1	None
		MOV WREG, f	Move WREG to f	1	1	None
		MOV.D Wns, Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws, Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
47	MOVPAG	MOVPAG #lit10, DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG #lit9, DSWPAG	Move 9-bit literal to DSWPAG	1	1	None
		MOVPAG #lit8, TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAGW Ws, DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAGW Ws, DSWPAG	Move Ws<8:0> to DSWPAG	1	1	None
		MOVPAGW Ws, TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
48	MOVSAC	MOVSAC Acc, Wx, Wxd, Wy, Wyd, AWB	Prefetch and store accumulator	1	1	None
49	MPY	MPY Wm*Wn, Acc, Wx, Wxd, Wy, Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		MPY Wm*Wm, Acc, Wx, Wxd, Wy, Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
50	MPY.N	MPY.N Wm*Wn, Acc, Wx, Wxd, Wy, Wyd	-(Multiply Wm by Wn) to Accumulator	1	1	None
51	MSC	MSC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd, AWB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
52	MUL	MUL.SS Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS Wb, Ws, Acc	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, Ws, Acc	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, #lit5, Acc	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US Wb, Ws, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US Wb, Ws, Acc	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU Wb, Ws, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU Wb, #lit5, Acc	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, Ws, Acc	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS Wb, Ws, Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU Wb, Ws, Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US Wb, Ws, Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU Wb, Ws, Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, #lit5, Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU Wb, #lit5, Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, #lit5, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, #lit5, Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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FIGURE 33-8: OUTPUT COMPARE x (OCx) TIMING CHARACTERISTICS

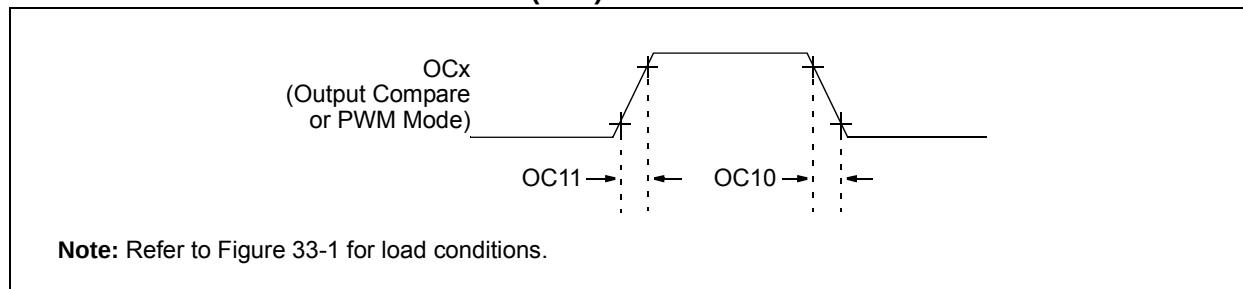


TABLE 33-26: OUTPUT COMPARE x (OCx) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 33-9: OCx/PWMx MODULE TIMING CHARACTERISTICS

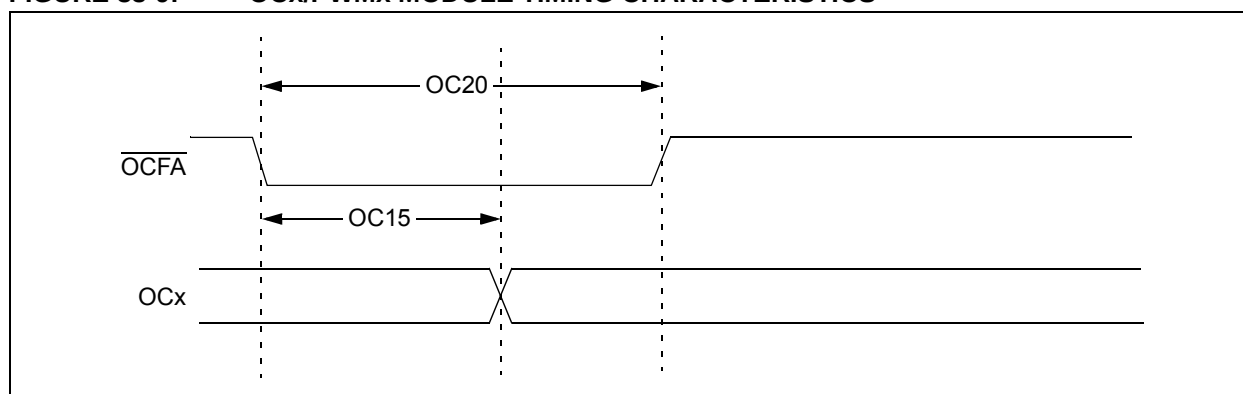


TABLE 33-27: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC15	TFD	Fault Input to PWMx I/O Change	—	—	Tcy + 20	ns	
OC20	TFLT	Fault Input Pulse Width	Tcy + 20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

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TABLE 33-52: OP AMP/COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
Comparator AC Characteristics							
CM10	TRESP	Response Time	—	19	—	ns	V+ input step of 100 mV, V- input held at VDD/2
CM11	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	μs	
Comparator DC Characteristics							
CM30	VOFFSET	Comparator Offset Voltage	—	±20	±75	mV	
CM31	VHYST	Input Hysteresis Voltage	—	30	—	mV	
CM32	TRISE/ TFALL	Comparator Output Rise/Fall Time	—	20	—	ns	1 pF load capacitance on input
CM33	VGAIN	Open-Loop Voltage Gain	—	90	—	db	
CM34	VICM	Input Common-Mode Voltage	AVSS	—	AVDD	V	
Op Amp AC Characteristics							
CM20	SR	Slew Rate	—	9	—	V/μs	10 pF load
CM21a	PM	Phase Margin	—	68	—	Degree	G = 100V/V; 10 pF load
CM22	GM	Gain Margin	—	20	—	db	G = 100V/V; 10 pF load
CM23a	GBW	Gain Bandwidth	—	10	—	MHz	10 pF load
Op Amp DC Characteristics							
CM40	VCMR	Common-Mode Input Voltage Range	AVSS	—	AVDD	V	
CM41	CMRR	Common-Mode Rejection Ratio	—	40	—	db	VCM = AVDD/2
CM42	VOFFSET	Op Amp Offset Voltage	—	±20	±70	mV	
CM43	VGAIN	Open-Loop Voltage Gain	—	90	—	db	
CM44	IOS	Input Offset Current	—	—	—	—	See pad leakage currents in Table 33-10
CM45	IB	Input Bias Current	—	—	—	—	See pad leakage currents in Table 33-10
CM46	IOUT	Output Current	—	—	420	μA	With minimum value of RFEEDBACK (CM48)
CM48	RFEEDBACK	Feedback Resistance Value	8	—	—	kΩ	(Note 2)
CM49a	VOUT	Output Voltage	AVSS + 0.075	—	AVDD – 0.075	V	IOUT = 420 μA

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

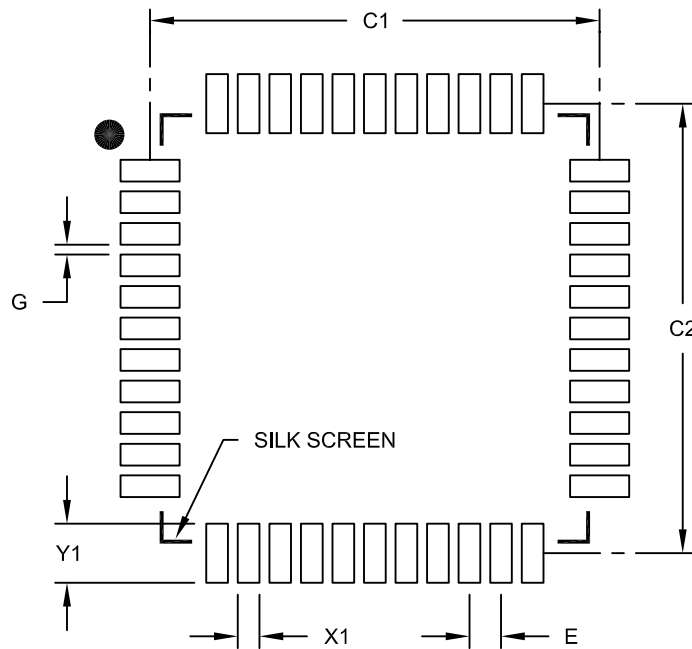
2: Resistances can vary by ±10% between op amps.

3: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

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44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B