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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 30x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm706t-i-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin #	Full Pin Name	Pin #	Full Pin Name
E1	PWM6H/T8CK/RD4	J8	No Connect
E2	PWM6L/T9CK/RD3	J9	No Connect
E3	AN19/RP118/PMA5/RG6	J10	AN41/RP81/RE1
E4	PWM5H/RD2	J11	AN30/SDA1/RPI52/RC4
E5	No Connect	K1	PGED3/OA2IN-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
E6	RP113/RG1	K2	PGEC3/CVREF+/OA1OUT/AN3/C1IN4-/C4IN2-/RPI33/ CTED1/RB1
E7	No Connect	К3	VREF+/AN34/PMA7/RF10
K4	OA3OUT/AN6/C3IN4-/C4IN4-/C4IN1+/RP48/OCFB/RC0	L3	AVss
K5	No Connect	L4	OA3IN-/AN7/C3IN1-/C4IN1-/RP49/RC1
K6	AN37/RF12	L5	OA3IN+/AN8/C3IN3-/C3IN1+/RPI50/U1RTS/BCLK1/FLT3/ PMA13/RC2
K7	AN14/RPI94/FLT7/PMA1/RE14	L6	AN36/RF13
K8	VDD	L7	AN13/C3IN2-/U2CTS/FLT6/PMA10/RE13
K9	AN39/RD15	L8	AN15/RPI95/FLT8/PMA0/RE15
K10	OA5IN+/AN24/C5IN3-/C5IN1+/SDO1/RP20/T1CK/RA4	L9	AN38/RD14
K11	AN40/RPI80/RE0	L10	SDA2/RPI24/PMA9/RA8
L1	PGEC1/OA1IN+/AN4/C1IN3-/C1IN1+/C2IN3-/RPI34/RB2	L11	FLT32/SCL2/RP36/PMA8/RB4
12			

TABLE 2:PIN NAMES: dsPIC33EP128/256/512GM310/710 DEVICES^(1,2,3) (CONTINUED)

Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See Section 11.4 "Peripheral Pin Select (PPS)" for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See Section 11.0 "I/O Ports" for more information.

3: The availability of I²C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See Section 30.0 "Special Features" for more information.

TABLE 4-6:	OUTPUT COMPARE REGISTER MAP (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC7CON1	093C	_	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	_	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC7CON2	093E	FLTMD	FLTOUT	FLTTRIEN	OCINV		—		OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC7RS	0940	Output Compare 7 Secondary Register												xxxx				
OC7R	0942	Output Compare 7 Register											xxxx					
OC7TMR	0944							Out	put Compa	are 7 Time	r Value Regis	ster						xxxx
OC8CON1	0946		—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0		ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC8CON2	0948	FLTMD	FLTOUT	FLTTRIEN	OCINV		_		OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC8RS	094A							Ou	tput Comp	are 8 Seco	ondary Regis	ter						xxxx
OC8R	094C								Output	Compare 8	8 Register							xxxx
OC8TMR	094E							Out	put Compa	are 8 Time	r Value Regis	ster						xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	0300								ADC1 Da	ta Buffer	0							xxxx
ADC1BUF1	0302								ADC1 Da	ita Buffer	1							xxxx
ADC1BUF2	0304								ADC1 Da	ita Buffer	2							xxxx
ADC1BUF3	0306								ADC1 Da	ita Buffer	3							xxxx
ADC1BUF4	0308								ADC1 Da	ta Buffer	4							xxxx
ADC1BUF5	030A								ADC1 Da	ta Buffer	5							xxxx
ADC1BUF6	030C								ADC1 Da	ta Buffer	6							xxxx
ADC1BUF7	030E		ADC1 Data Buffer 7 xxxx															
ADC1BUF8	0310		ADC1 Data Buffer 8 xxxx															
ADC1BUF9	0312		ADC1 Data Buffer 9 xxxx															
ADC1BUFA	0314		ADC1 Data Buffer 10 xxxx															
ADC1BUFB	0316								ADC1 Dat	ta Buffer '	11							xxxx
ADC1BUFC	0318								ADC1 Dat	ta Buffer '	12							xxxx
ADC1BUFD	031A								ADC1 Dat	ta Buffer '	13							xxxx
ADC1BUFE	031C								ADC1 Dat	ta Buffer '	14							xxxx
ADC1BUFF	031E		-	-	-	_		_	ADC1 Dat	ta Buffer '	15		-	-		-		xxxx
AD1CON1	0320	ADON		ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0	SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE	0000
AD1CON2	0322	VCFG2	VCFG1	VCFG0	OFFCAL	—	CSCNA	CHPS1	CHPS0	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	0324	ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS123	0326	_	—	—	CH123SB2	CH123SB1	CH123NB1	CH123NB0	CH123SB0	—	—	_	CH123SA2	CH123SA1	CH123NA1	CH123NA0	CH123SA0	0000
AD1CHS0	0328	CH0NB		CH0SB5	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA	—	CH0SA5	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1CSSH	032E								CSS<	31:16>								0000
AD1CSSL	0330								CSS	<15:0>								0000
AD1CON4	0332	_		_	_	—	_	—	ADDMAEN	_	—	_	—	_	DMABL2	DMABL1	DMABL0	0000
ADC2BUF0	0340								ADC2 Da	ata Buffer	0							xxxx
ADC2BUF1	0342								ADC2 Da	ata Buffer	1							xxxx
ADC2BUF2	0344								ADC2 Da	ata Buffer	2							xxxx
ADC2BUF3	0346								ADC2 Da	ta Buffer	3							xxxx
ADC2BUF4	0348								ADC2 Da	ta Buffer	4							xxxx
ADC2BUF5	034A								ADC2 Da	ta Buffer	5							xxxx
ADC2BUF6	034C								ADC2 Da	ta Buffer	6							xxxx
ADC2BUF7	034E								ADC2 Da	ta Buffer	7							xxxx
ADC2BUF8	0350								ADC2 Da	ta Buffer	8							xxxx

TABLE 4-22: ADC1 AND ADC2 REGISTER MAP

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Bits 13 and bit 5 are reserved in the AD2CHS0 register, unlike the AD1CHS0 register.

Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses an EDS or PSV page
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing. However, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSxPAG register is incremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-64 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- · Bit-Reversed Addressing

TABLE 4-64:OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS AND
PSV SPACE BOUNDARIES^(2,3,4)

0/11			Before		After				
0/0, R/W	Operation	DSxPAG	DS EA<15>	Page Description	DSxPAG	DS EA<15>	Page Description		
O, Read		DSRPAG = 0x1FF	1	EDS: Last Page	DSRPAG = 0x1FF	0	See Note 1		
O, Read	[++Wn]	DSRPAG = 0x2FF	1	PSV: Last Isw Page	DSRPAG = 0x300	1	PSV: First MSB Page		
O, Read	[Wn++]	DSRPAG = 0x3FF	1	PSV: Last MSB Page	DSRPAG = 0x3FF	0	See Note 1		
O, Write		DSWPAG = 0x1FF	1	EDS: Last Page	DSWPAG = 0x1FF	0	See Note 1		
U, Read	r	DSRPAG = 0x001	1	PSV Page	DSRPAG = 0x001	0	See Note 1		
U, Read	[Wn] Or [Wn]	DSRPAG = 0x200	1	PSV: First lsw Page	DSRPAG = 0x200	0	See Note 1		
U, Read	[111]	DSRPAG = 0x300	1	PSV: First MSB Page	DSRPAG = 0x2FF	1	PSV: Last Isw Page		

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the Base Data Space (0x0000-0x8000).

2: An EDS access with DSxPAG = 0x000 will generate an address error trap.

- **3:** Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.
- 4: Pseudo Linear Addressing is not supported for large offsets.

REGISTER 5-6: NVMSRCADRL: NONVOLATILE DATA MEMORY LOWER ADDRESS REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x			
			NVMSRC/	ADRL<15:8>						
bit 15							bit 8			
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	r-0			
NVMSRCADRL<7:1>										
bit 7							bit 0			
Legend:		r = Reserved	bit							
R = Readable bit W = Writable bit				U = Unimplemented bit, read as '0'						
-n = Value at POR '1' = Bit is set				'0' = Bit is cleared x = Bit is unknown						

bit 15-1 NVMSRCADRL<15:1>: Nonvolatile Data Memory Lower Address bits

bit 0 Reserved: Maintain as '0'

REGISTER 8-9:	DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

	11.0	11.0	11.0	11.0	11.0	11.0	11.0
U-0	0-0	U-0	U-0	0-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSADR	<23:16>			
bit 7							bit 0
Legend:							
D - Deedeble b	:.		4		a a wha al la it was al	aa (0)	

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 15-8 Unimplemented: Read as '0'

bit 7-0 DSADR<23:16>: Most Recent DMA Address Accessed by DMA bits

REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0				
			DSAD)R<15:8>							
bit 15							bit 8				
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0				
	DSADR<7:0>										
bit 7							bit 0				
Legend:											
R = Readable b	oit	W = Writable bit	t	U = Unimplemen	ted bit, rea	id as '0'					
-n = Value at POR (1' = Bit is set 0' = Bit is cleared x = Bit is unknown											

bit 15-0 DSADR<15:0>: Most Recent DMA Address Accessed by DMA bits

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Secondary (Timer1) Oscillator (SOSC)	Secondary	xx	100	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	1
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

10.0 POWER-SAVING FEATURES

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To _complement the information in this data sheet, refer to the "dsPIC33/PIC24 Family Reference Manual", "Watchdog Timer and Power-Saving Modes" (DS70615), which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

The dsPIC33EPXXXGM3XX/6XX/7XX devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- · Software-Controlled Doze mode
- · Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

PWRSAV #SLEEP_MODE ; Put the device into Sleep mode
PWRSAV #IDLE_MODE ; Put the device into Idle mode

10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGM3XX/6XX/7XX devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGM3XX/6XX/7XX devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the Assembler Include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

REGISTER 11-30: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
_	—		RP35R<5:0>						
bit 15							bit 8		
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—				RP20	R<5:0>				
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimplem	Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set				'0' = Bit is clea	ared	x = Bit is unkr	nown		
bit 15-14	Unimpleme	nted: Read as '	0'						
bit 13-8	RP35R<5:0>: Peripheral Output Function is Assigned to RP35 Output Pin bits								

	(see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP20R<5:0>: Peripheral Output Function is Assigned to RP20 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-31: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	_		RP37R<5:0>						
bit 15							bit 8		
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	_			RP36R<	<5:0>				
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'					
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown						
							,		
bit 15-14	Unimpleme	nted: Read as '	0'						

bit 13-8 **RP37R<5:0>:** Peripheral Output Function is Assigned to RP37 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **RP36R<5:0>:** Peripheral Output Function is Assigned to RP36 Output Pin bits (see Table 11-3 for peripheral function numbers)

R/W-0 R/W-0 R/W-0 R/W-0 U-0 U-0 U-0 R/W-0 **FLTMD FLTOUT FLTTRIEN** OCINV ___ OC32 ____ ____ bit 15 bit 8 R/W-0 R/W-0, HS R/W-0 R/W-0 R/W-1 R/W-1 R/W-0 R/W-0 OCTRIG OCTRIS SYNCSEL4 SYNCSEL2 TRIGSTAT SYNCSEL3 SYNCSEL1 SYNCSEL0 bit 7 bit 0 Legend: HS = Hardware Settable bit R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 FLTMD: Fault Mode Select bit 1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts 0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts bit 14 FLTOUT: Fault Out bit 1 = PWM output is driven high on a Fault 0 = PWM output is driven low on a Fault bit 13 FLTTRIEN: Fault Output State Select bit 1 = OCx pin is tri-stated on a Fault condition 0 = OCx pin I/O state is defined by the FLTOUT bit on a Fault condition bit 12 OCINV: OCx Invert bit 1 = OCx output is inverted 0 = OCx output is not inverted bit 11-9 Unimplemented: Read as '0' bit 8 OC32: Cascade Two OCx Modules Enable bit (32-bit operation) 1 = Cascade module operation is enabled 0 = Cascade module operation is disabled bit 7 OCTRIG: OCx Trigger/Sync Select bit 1 = Triggers OCx from source designated by the SYNCSELx bits 0 = Synchronizes OCx with source designated by the SYNCSELx bits bit 6 **TRIGSTAT:** Timer Trigger Status bit 1 = Timer source has been triggered and is running 0 = Timer source has not been triggered and is being held clear bit 5 OCTRIS: OCx Output Pin Direction Select bit 1 = Output Compare x is tri-stated 0 = Output Compare x module drives the OCx pin **Note 1:** Do not use the OCx module as its own synchronization or trigger source. 2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it. 3: Each Output Compare x module (OCx) has one PTG Trigger/Sync source. See Section 25.0 "Peripheral Trigger Generator (PTG) Module" for more information. PTGO4 = OC1, OC5PTGO5 = OC2, OC6PTGO6 = OC3, OC7 PTGO7 = OC4, OC8

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

REGISTER 18-2: SPIXCON1: SPIX CONTROL REGISTER 1 (CONTINUED)

- bit 4-2 SPRE<2:0>: Secondary Prescale bits (Master mode)⁽³⁾ 111 = Secondary prescale 1:1
 - 110 = Secondary prescale 2:1

 - 000 = Secondary prescale 8:1
- bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)⁽³⁾
 - 11 = Primary prescale 1:1
 - 10 = Primary prescale 4:1
 - 01 = Primary prescale 16:1
 - 00 = Primary prescale 64:1
- Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
 - 2: This bit must be cleared when FRMEN = 1.
 - **3:** Do not set both primary and secondary prescalers to the value of 1:1.

CM4CON: OP AMP/COMPARATOR 4 CONTROL REGISTER (CONTINUED) REGISTER 26-3: EVPOL<1:0>: Trigger/Event/Interrupt Polarity Select bits⁽²⁾ bit 7-6 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0) 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0) If CPOL = 1 (inverted polarity): Low-to-high transition of the comparator output. If CPOL = 0 (non-inverted polarity): High-to-low transition of the comparator output. 01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0) If CPOL = 1 (inverted polarity): High-to-low transition of the comparator output. If CPOL = 0 (non-inverted polarity): Low-to-high transition of the comparator output. 00 = Trigger/event/interrupt generation is disabled Unimplemented: Read as '0' bit 5 CREF: Comparator Reference Select bit (VIN+ input)⁽¹⁾ bit 4 1 = VIN+ input connects to internal CVREFIN voltage 0 = VIN+ input connects to C4IN1+ pin bit 3-2 Unimplemented: Read as '0' CCH<1:0>: Comparator Channel Select bits⁽¹⁾ bit 1-0 11 = VIN- input of comparator connects to OA3/AN6 10 = VIN- input of comparator connects to OA2/AN0 01 = VIN- input of comparator connects to OA1/AN3 00 = VIN- input of comparator connects to C4IN1-Note 1: Inputs that are selected and not available will be tied to Vss. See the "Pin Diagrams" section for available inputs for each package.

2: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the Comparator Event bit, CEVT (CMxCON<9>), and the Comparator Combined Interrupt Flag, CMPIF (IFS1<2>), **must be cleared** before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

REGISTER 27-9: ALRMVAL (WHEN ALRMPTR<1:0> = 01): ALARM WEEKDAY AND HOURS VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11	Unimplemented: Read as '0'
-----------	----------------------------

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits Contains a value from 0 to 6.

bit 7-6 Unimplemented: Read as '0'

- bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits Contains a value from 0 to 2.
- bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

29.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33/PIC24 Family Reference Manual", "32-Bit Programmable Cyclic Redundancy Check (CRC)" (DS70346), which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-Programmable (up to 32nd order) polynomial CRC equation
- Interrupt Output
- Data FIFO

The programmable CRC generator provides a hardware-implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- · Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 29-1. A simple version of the CRC shift engine is shown in Figure 29-2.



FIGURE 29-1: CRC BLOCK DIAGRAM



AC CHARACTERISTICS			Standard Ope (unless other Operating tem	rating C wise stat perature	onditions: 3.0V to 3.6V ted) $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended			
Param No.	Symb	Characteristic	Min.	Min. Typ. ⁽¹⁾		Units	Conditions	
OS10 FIN		External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	_	60	MHz	EC	
		Oscillator Crystal Frequency	3.5 10 32.4	 32.768	10 25 33.1	MHz MHz kHz	XT HS SOSC	
OS20	Tosc	Tosc = 1/Fosc	8.33	_	DC	ns	TA = +125°C	
		Tosc = 1/Fosc	7.14	—	DC	ns	TA = +85°C	
OS25	Тсү	Instruction Cycle Time ⁽²⁾	16.67	—	DC	ns	TA = +125°C	
			14.28		DC	ns	TA = +85°C	
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.375 x Tosc	_	0.625 x Tosc	ns	EC	
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time		_	20	ns	EC	
OS40	TckR	CLKO Rise Time ⁽³⁾	—	5.2	—	ns		
OS41	TckF	CLKO Fall Time ⁽³⁾	—	5.2	_	ns		
OS42	Gм	External Oscillator Transconductance ⁽⁴⁾		12		mA/V	HS, VDD = 3.3V, TA = +25°C	
			_	6	_	mA/V	XT, VDD = 3.3V, TA = +25°C	

TABLE 33-16: EXTERNAL CLOCK TIMING REQUIREMENTS

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

- 2: Instruction cycle period (Tcr) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.
- 3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.
- 4: This parameter is characterized, but not tested in manufacturing.

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FIGURE 33-8: OUTPUT COMPARE x (OCx) TIMING CHARACTERISTICS



TABLE 33-26: OUTPUT COMPARE x (OCx) TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions	
OC10	TccF	OCx Output Fall Time	_	_		ns	See Parameter DO32	
OC11	TccR	OCx Output Rise Time	—	—		ns	See Parameter DO31	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 33-9: OCx/PWMx MODULE TIMING CHARACTERISTICS



TABLE 33-27: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Min. Typ. Max. Units			
OC15	Tfd	Fault Input to PWMx I/O Change	—	_	Tcy + 20	ns	
OC20	TFLT	Fault Input Pulse Width	Tcy + 20	_	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.



FIGURE 33-21: SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



FIGURE 33-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

TABLE 33-52: OP AMP/COMPARATOR SPECIFICATIONS

DC CHARACTERISTICS			Standard Op (unless othe Operating ter	Standard Operating Conditions (see Note 3): 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended			
Param No.	Symbol	Characteristic	Min.	Тур. ⁽¹⁾	Max.	Units	Conditions
Compa	rator AC Ch	aracteristics					
CM10	TRESP	Response Time	—	19	—	ns	V+ input step of 100 mV, V- input held at VDD/2
CM11	Тмс2о∨	Comparator Mode Change to Output Valid	—	—	10	μs	
Compa	rator DC Ch	naracteristics					
CM30	VOFFSET	Comparator Offset Voltage	_	±20	±75	mV	
CM31	VHYST	Input Hysteresis Voltage	—	30	—	mV	
CM32	Trise/ Tfall	Comparator Output Rise/Fall Time	—	20	—	ns	1 pF load capacitance on input
CM33	Vgain	Open-Loop Voltage Gain	—	90	—	db	
CM34	VICM	Input Common-Mode Voltage	AVss	—	AVDD	V	
Op Am	p AC Chara	cteristics					
CM20	SR	Slew Rate		9		V/µs	10 pF load
CM21a	Рм	Phase Margin	_	68	—	Degree	G = 100V/V; 10 pF load
CM22	Gм	Gain Margin	—	20	—	db	G = 100V/V; 10 pF load
CM23a	GBW	Gain Bandwidth	—	10	—	MHz	10 pF load
Op Am	p DC Chara	cteristics					
CM40	VCMR	Common-Mode Input Voltage Range	AVss	-	AVDD	V	
CM41	CMRR	Common-Mode Rejection Ratio	—	40	—	db	Vcm = AVdd/2
CM42	VOFFSET	Op Amp Offset Voltage	—	±20	±70	mV	
CM43	Vgain	Open-Loop Voltage Gain	_	90	_	db	
CM44	los	Input Offset Current	—	_	—	_	See pad leakage currents in Table 33-10
CM45	Ів	Input Bias Current	—	_	—	_	See pad leakage currents in Table 33-10
CM46	Ιουτ	Output Current	—		420	μA	With minimum value of RFEEDBACK (CM48)
CM48	RFEEDBACK	Feedback Resistance Value	8	_		kΩ	(Note 2)
CM49a	Vout	Output Voltage	AVss + 0.075	_	AVDD - 0.075	V	Ιουτ = 420 μΑ

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

2: Resistances can vary by ±10% between op amps.

3: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B