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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

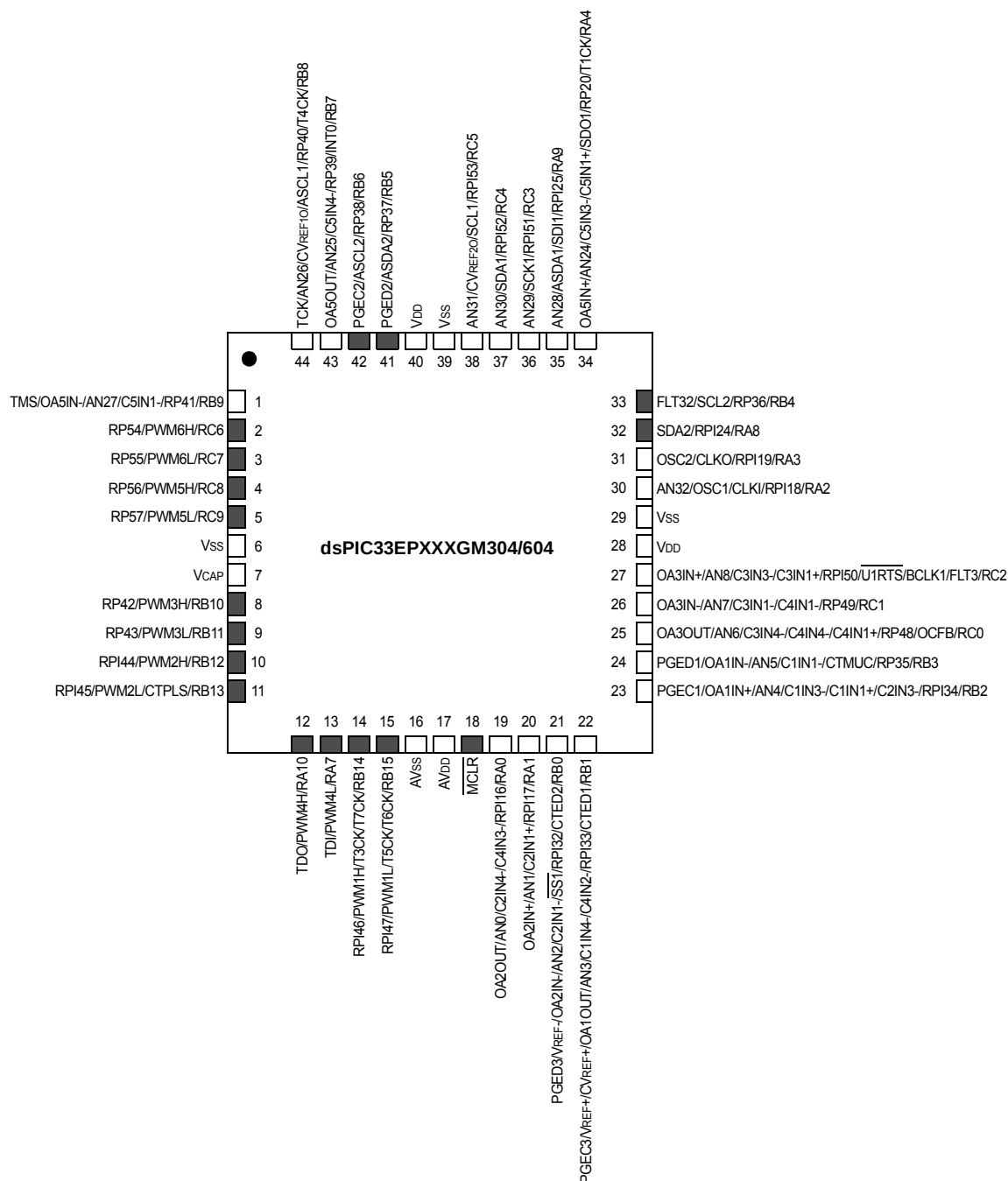
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 30x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm706t-i-pt

dsPIC33EPXXXGM3XX/6XX/7XX

Pin Diagrams (Continued)

44-Pin QFN^(1,2,3)

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

dsPIC33EPXXXGM3XX/6XX/7XX

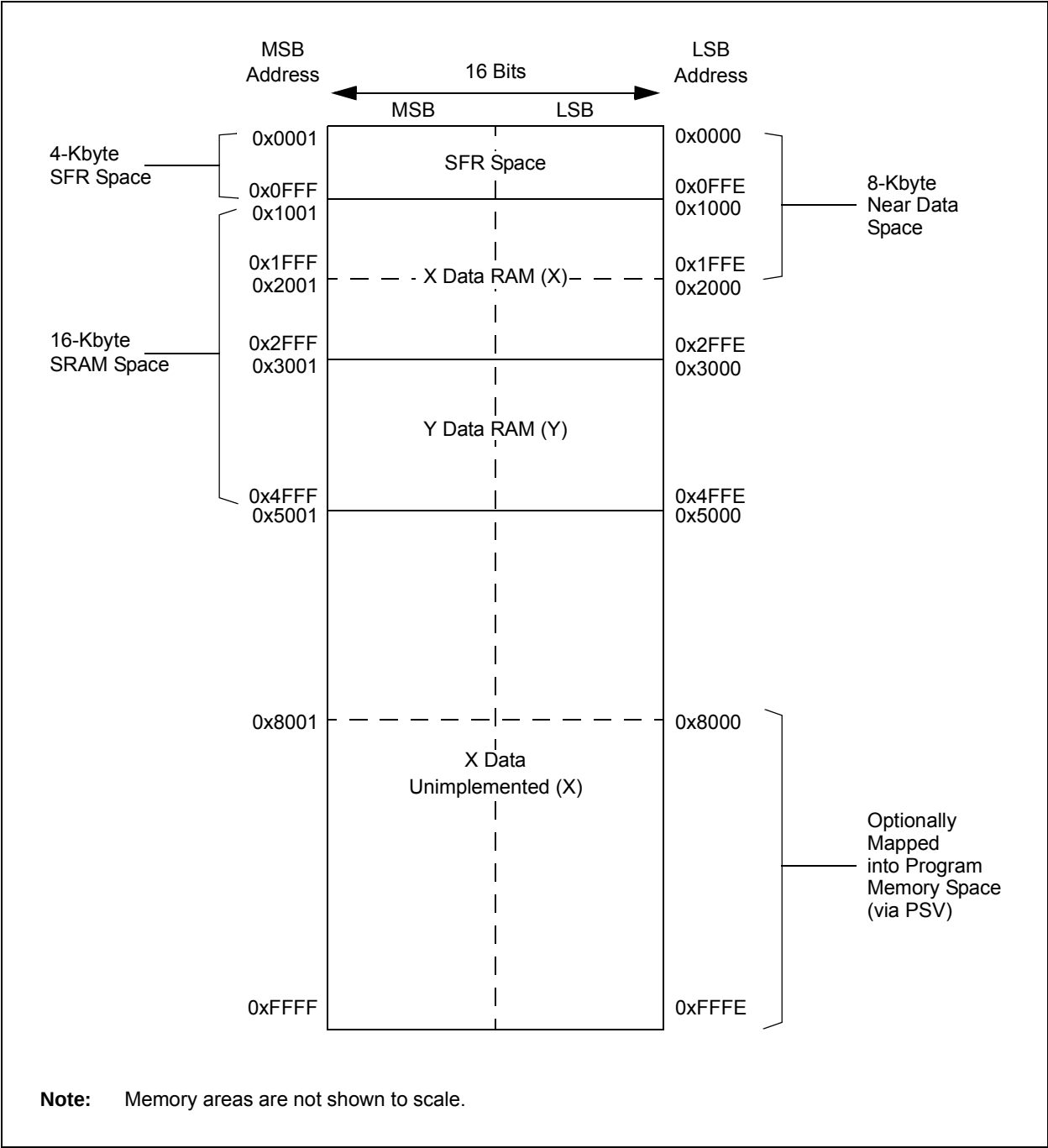
TABLE 2: PIN NAMES: dsPIC33EP128/256/512GM310/710 DEVICES^(1,2,3) (CONTINUED)

Pin #	Full Pin Name	Pin #	Full Pin Name
E1	PWM6H/T8CK/RD4	J8	No Connect
E2	PWM6L/T9CK/RD3	J9	No Connect
E3	AN19/RP118/PMA5/RG6	J10	AN41/RP81/RE1
E4	PWM5H/RD2	J11	AN30/SDA1/RPI52/RC4
E5	No Connect	K1	PGED3/OA2IN-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
E6	RP113/RG1	K2	PGEC3/CVREF+/OA1OUT/AN3/C1IN4-/C4IN2-/RPI33/CTED1/RB1
E7	No Connect	K3	VREF+/AN34/PMA7/RF10
K4	OA3OUT/AN6/C3IN4-/C4IN4-/C4IN1+/RP48/OCFB/RC0	L3	AVss
K5	No Connect	L4	OA3IN-/AN7/C3IN1-/C4IN1-/RP49/RC1
K6	AN37/RF12	L5	OA3IN+/AN8/C3IN3-/C3IN1+/RPI50/U1RTS/BCLK1/FLT3/PMA13/RC2
K7	AN14/RPI94/FLT7/PMA1/RE14	L6	AN36/RF13
K8	VDD	L7	AN13/C3IN2-/U2CTS/FLT6/PMA10/RE13
K9	AN39/RD15	L8	AN15/RPI95/FLT8/PMA0/RE15
K10	OA5IN+/AN24/C5IN3-/C5IN1+/SDO1/RP20/T1CK/RA4	L9	AN38/RD14
K11	AN40/RPI80/RE0	L10	SDA2/RPI24/PMA9/RA8
L1	PGEC1/OA1IN+/AN4/C1IN3-/C1IN1+/C2IN3-/RPI34/RB2	L11	FLT32/SCL2/RP36/PMA8/RB4
L2	VREF-/AN33/PMA6/RF9		

- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- 3:** The availability of I²C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5.4>). See **Section 30.0 “Special Features”** for more information.

dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 4-5: DATA MEMORY MAP FOR 128-KBYTE DEVICES



dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 4-7: DATA MEMORY MAP FOR 512-KBYTE DEVICES

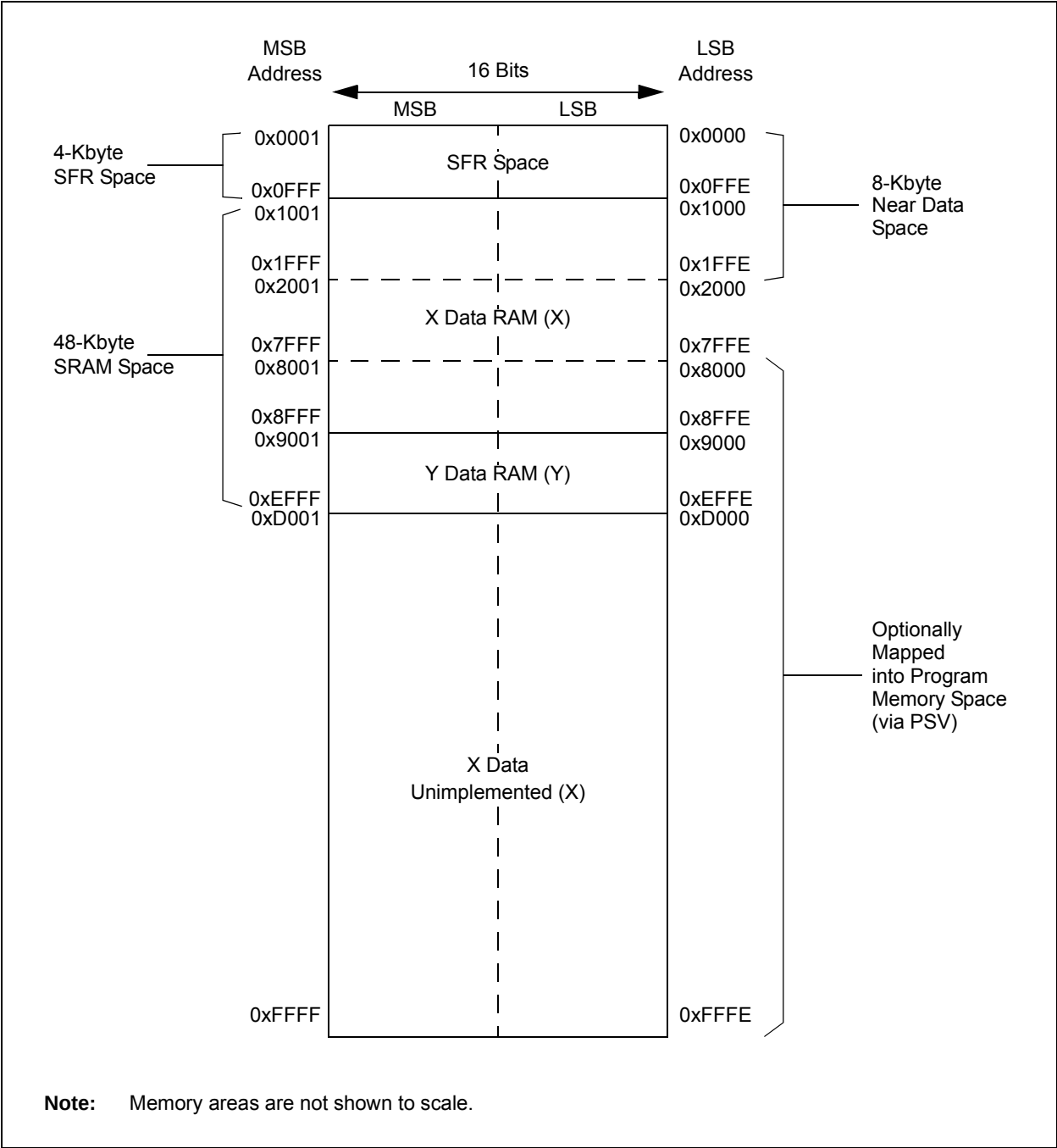


TABLE 4-7: PTG REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTGCST	0AC0	PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT	PTGSSEN	PTGIVIS	PTGSTRT	PTGWDTO	—	—	—	—	PTGITM1	PTGITM0	0000
PTGCON	0AC2	PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0	PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0	0000
PTGBTE	0AC4	ADCTS4	ADCTS3	ADCTS2	ADCTS1	IC4TSS	IC3TSS	IC2TSS	IC1TSS	OC4CS	OC3CS	OC2CS	OC1CS	OC4TSS	OC3TSS	OC2TSS	OC1TSS	0000
PTGHOLD	0AC6	PTGHOLD<15:0>																0000
PTGTOLIM	0AC8	PTGTOLIM<15:0>																0000
PTGT1LIM	0ACA	PTGT1LIM<15:0>																0000
PTGSDLIM	0ACC	PTGSDLIM<15:0>																0000
PTGC0LIM	0ACE	PTGC0LIM<15:0>																0000
PTGC1LIM	0AD0	PTGC1LIM<15:0>																0000
PTGADJ	0AD2	PTGADJ<15:0>																0000
PTGL0	0AD4	PTGL0<15:0>																0000
PTGQPTR	0AD6	—	—	—	—	—	—	—	—	—	—	—	PTGQPTR<4:0>					0000
PTGQUE0	0AD8	STEP1<7:0>								STEP0<7:0>								0000
PTGQUE1	0ADA	STEP3<7:0>								STEP2<7:0>								0000
PTGQUE2	0ADC	STEP5<7:0>								STEP4<7:0>								0000
PTGQUE3	0ADE	STEP7<7:0>								STEP6<7:0>								0000
PTGQUE4	0AE0	STEP9<7:0>								STEP8<7:0>								0000
PTGQUE5	0AE2	STEP11<7:0>								STEP10<7:0>								0000
PTGQUE6	0AE4	STEP13<7:0>								STEP12<7:0>								0000
PTGQUE7	0AE6	STEP15<7:0>								STEP14<7:0>								0000
PTGQUE8	0x0AE8	STEP17<7:0>								STEP16<7:0>								0000
PTGQUE9	0x0AEA	STEP19<7:0>								STEP18<7:0>								0000
PTGQUE10	0x0AEC	STEP21<7:0>								STEP20<7:0>								0000
PTGQUE11	0x0AEE	STEP23<7:0>								STEP22<7:0>								0000
PTGQUE12	0x0AF0	STEP25<7:0>								STEP24<7:0>								0000
PTGQUE13	0x0AF2	STEP27<7:0>								STEP26<7:0>								0000
PTGQUE14	0x0AF4	STEP29<7:0>								STEP28<7:0>								0000
PTGQUE15	0x0AF6	STEP31<7:0>								STEP30<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-15: QE1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
QE1CON	01C0	QEIEN	—	QEISIDL	PIMOD2	PIMOD1	PIMOD0	IMV1	IMV0	—	INTDIV2	INTDIV1	INTDIV0	CNTPOL	GATEN	CCM1	CCM0	0000
QE1IOC	01C2	QCAPEN	FLTREN	QFDIV2	QFDIV1	QFDIV0	OUTFNC1	OUTFNC0	SWPAB	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA	000x
QE1STAT	01C4	—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN	PCIIRQ	PCIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN	0000
POS1CNTL	01C6	POSCNT<15:0>																0000
POS1CNTH	01C8	POSCNT<31:16>																0000
POS1HLD	01CA	POSHLD<15:0>																0000
VEL1CNT	01CC	VELCNT<15:0>																0000
INT1TMRL	01CE	INTTMR<15:0>																0000
INT1TMRH	01D0	INTTMR<31:16>																0000
INT1HLDL	01D2	INTHLD<15:0>																0000
INT1HLDH	01D4	INTHLD<31:16>																0000
INDX1CNTL	01D6	INDXCNT<15:0>																0000
INDX1CNTH	01D8	INDXCNT<31:16>																0000
INDX1HLD	01DA	INDXHLD<15:0>																0000
QE1GECL	01DC	QEIGEC<15:0>																0000
QE1ICL	01DC	QEIIC<15:0>																0000
QE1GECH	01DE	QEIGEC<31:16>																0000
QE1ICH	01DE	QEIIC<31:16>																0000
QE1LECL	01E0	QEILEC<15:0>																0000
QE1LECH	01E2	QEILEC<31:16>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Secondary (Timer1) Oscillator (SOSC)	Secondary	xx	100	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	1
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER⁽²⁾ (CONTINUED)

bit 4-0 **PLLPRE<4:0>**: PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)
11111 = Input divided by 33
•
•
•
00001 = Input divided by 3
00000 = Input divided by 2 (default)

- Note 1:** This bit is cleared when the ROI bit is set and an interrupt occurs.
- 2:** This register resets only on a Power-on Reset (POR).
- 3:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
- 4:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

bit 4	SPI2MD: SPI2 Module Disable bit 1 = SPI2 module is disabled 0 = SPI2 module is enabled
bit 3	SPI1MD: SPI1 Module Disable bit 1 = SPI1 module is disabled 0 = SPI1 module is enabled
bit 2	C2MD: CAN2 Module Disable bit ⁽¹⁾ 1 = CAN2 module is disabled 0 = CAN2 module is enabled
bit 1	C1MD: CAN1 Module Disable bit ⁽¹⁾ 1 = CAN1 module is disabled 0 = CAN1 module is enabled
bit 0	AD1MD: ADC1 Module Disable bit 1 = ADC1 module is disabled 0 = ADC1 module is enabled

Note 1: These bits are available on dsPIC33EPXXXGM6XX/7XX devices only.

11.7 Peripheral Pin Select Registers

REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT1R<6:0>						
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **INT1R<6:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•
•
•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 11-29: RPINR41: PERIPHERAL PIN SELECT INPUT REGISTER 41

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	DTCMP6R<6:0>							
bit 7								bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7

Unimplemented: Read as '0'

bit 6-0

DTCMP6R<6:0>: Assign PWM Dead-Time Compensation Input 6 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•
•
•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-30: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP35R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP35R<5:0>**: Peripheral Output Function is Assigned to RP35 Output Pin bits
(see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP20R<5:0>**: Peripheral Output Function is Assigned to RP20 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 11-31: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP37R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP36R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP37R<5:0>**: Peripheral Output Function is Assigned to RP37 Output Pin bits
(see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP36R<5:0>**: Peripheral Output Function is Assigned to RP36 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)

- bit 3 **TRIGMODE:** Trigger Status Mode Select bit
1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
0 = TRIGSTAT is cleared only by software
- bit 2-0 **OCM<2:0>:** Output Compare x Mode Select bits
111 = Center-Aligned PWM mode: Output sets high when OCxTMR = OCxR and sets low when OCxTMR = OCxRS⁽¹⁾
110 = Edge-Aligned PWM mode: Output sets high when OCxTMR = 0 and sets low when OCxTMR = OCxR⁽¹⁾
101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS
100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle
011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin
010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low
001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high
000 = Output compare channel is disabled

Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

- 2:** Each Output Compare x module (OCx) has one PTG clock source. See **Section 25.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
PTGO4 = OC1, OC5
PTGO5 = OC2, OC6
PTGO6 = OC3, OC7
PTGO7 = OC4, OC8

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 17-15: QEIXGEC: QEIX GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<31:24>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **QEIGEC<31:16>**: High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEIXGEC) bits

REGISTER 17-16: QEIXGECL: QEIX GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIGEC<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

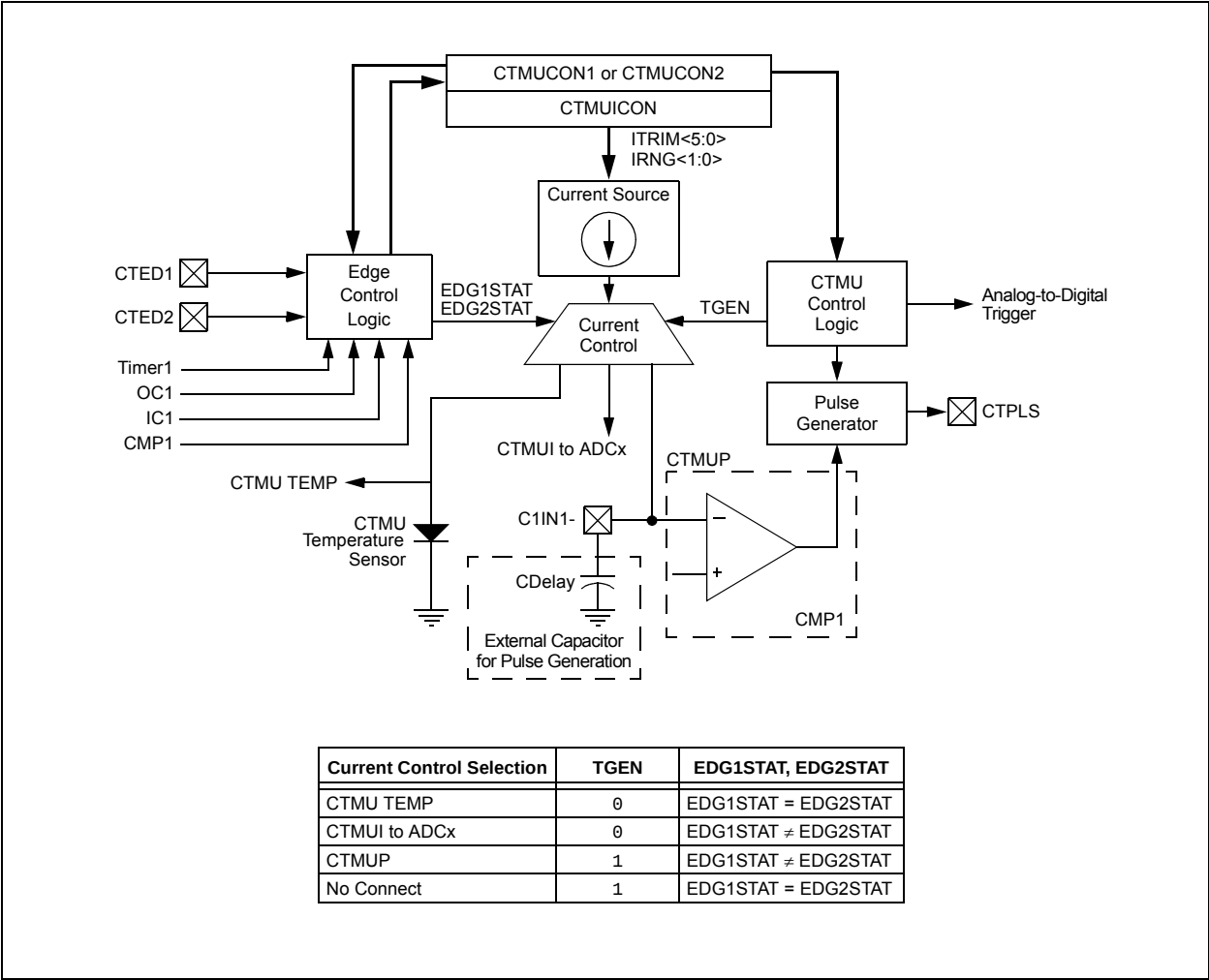
'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **QEIGEC<15:0>**: Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEIXGEC) bits

FIGURE 22-1: CTMU BLOCK DIAGRAM



REGISTER 25-10: PTGADJ: PTG ADJUST REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGADJ<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGADJ<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PTGADJ<15:0>**: PTG Adjust Register bits
This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 register with the PTGADD command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 25-11: PTGL0: PTG LITERAL 0 REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGL0<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGL0<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PTGL0<15:0>**: PTG Literal 0 Register bits
This register holds the 16-bit value to be written to the AD1CHS0 register with the PTGCTRL Step command.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 26-4: CMxMSKSRG: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **SELSRCC<3:0>:** Mask C Input Select bits

1111 = FLT4
 1110 = FLT2
 1101 = PTGO19
 1100 = PTGO18
 1011 = PWM6H
 1010 = PWM6L
 1001 = PWM5H
 1000 = PWM5L
 0111 = PWM4H
 0110 = PWM4L
 0101 = PWM3H
 0100 = PWM3L
 0011 = PWM2H
 0010 = PWM2L
 0001 = PWM1H
 0000 = PWM1L

bit 7-4 **SELSRCB<3:0>:** Mask B Input Select bits

1111 = FLT4
 1110 = FLT2
 1101 = PTGO19
 1100 = PTGO18
 1011 = PWM6H
 1010 = PWM6L
 1001 = PWM5H
 1000 = PWM5L
 0111 = PWM4H
 0110 = PWM4L
 0101 = PWM3H
 0100 = PWM3L
 0011 = PWM2H
 0010 = PWM2L
 0001 = PWM1H
 0000 = PWM1L

REGISTER 28-4: PMAEN: PARALLEL MASTER PORT ADDRESS ENABLE REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN15	PTEN14	PTEN<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN<7:2>						PTEN<1:0>	
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at Reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **PTEN15:** PMCS2 Strobe Enable bit
 1 = PMA15 functions as either PMA<15> or PMCS2
 0 = PMA15 functions as port I/O
- bit 14 **PTEN14:** PMCS1 Strobe Enable bit
 1 = PMA14 functions as either PMA<14> or PMCS1
 0 = PMA14 functions as port I/O
- bit 13-2 **PTEN<13:2>:** PMP Address Port Enable bits
 1 = PMA<13:2> function as PMP address lines
 0 = PMA<13:2> function as port I/Os
- bit 1-0 **PTEN<1:0>:** PMALH/PMALL Strobe Enable bits
 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL
 0 = PMA1 and PMA0 function as port I/Os

Note 1: This register is not available on 44-pin devices.

FIGURE 33-39: ADC1 CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS
(CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)

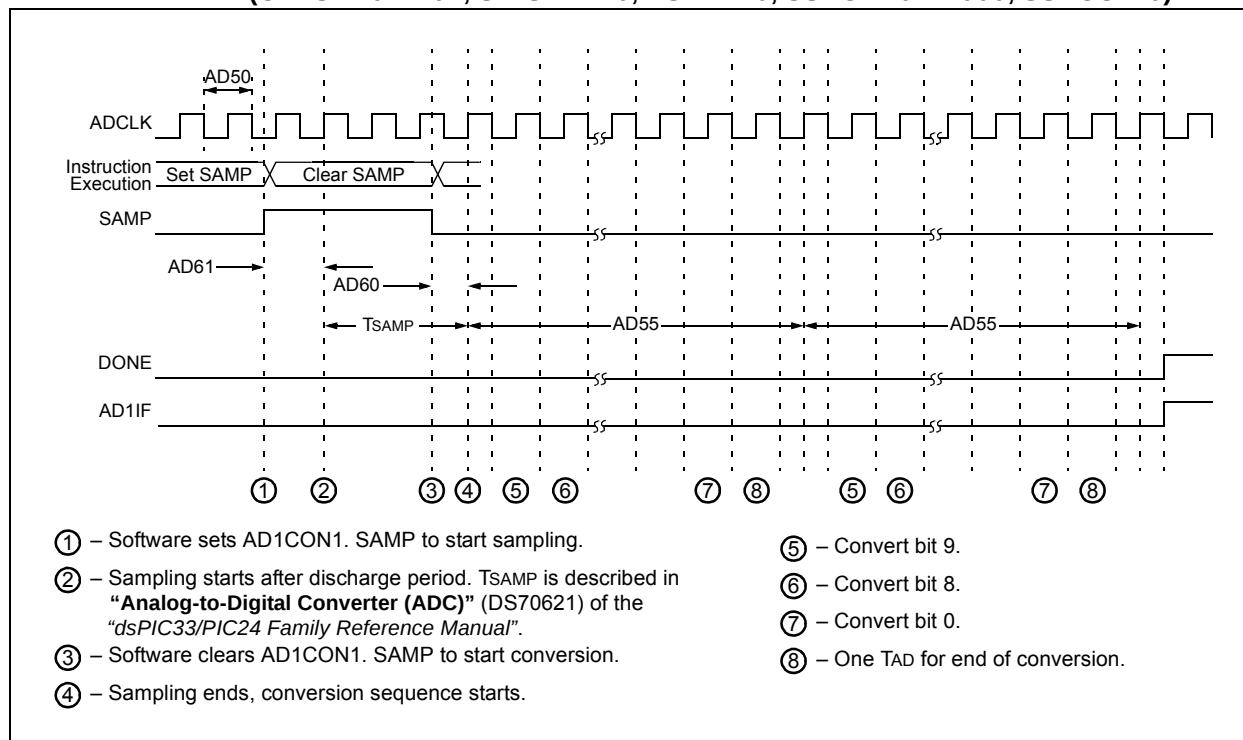
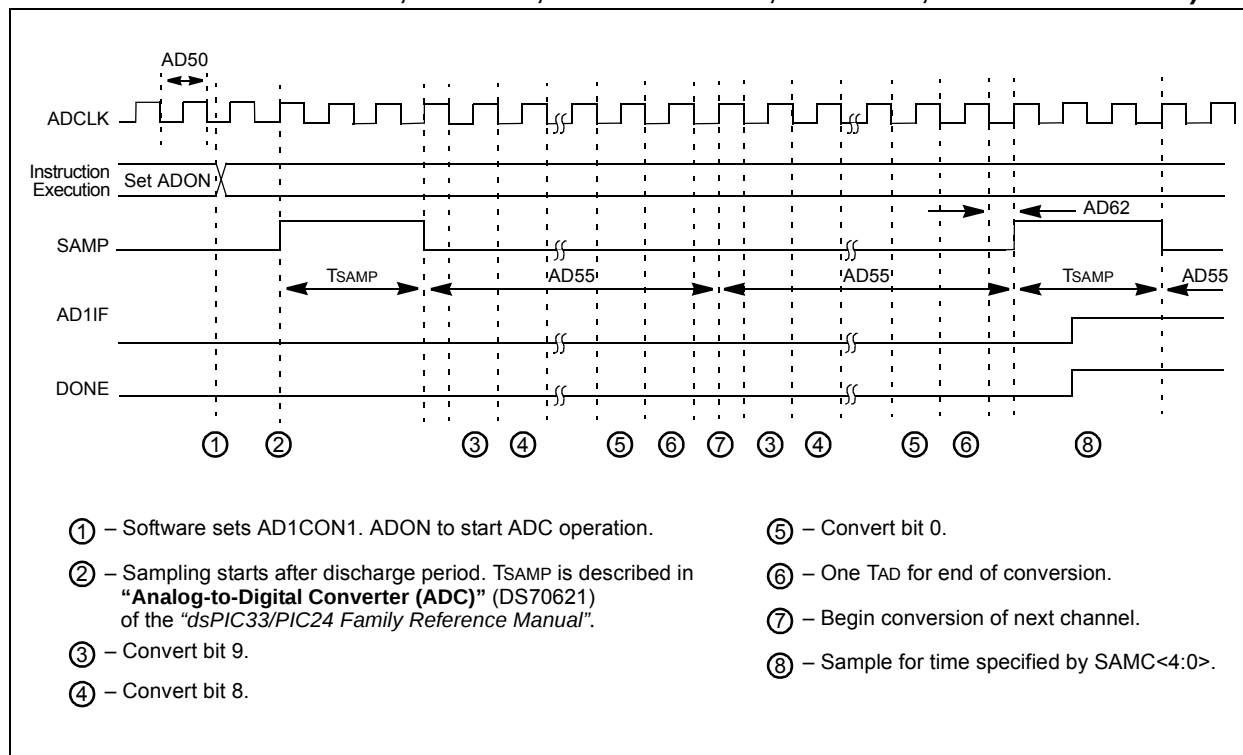


FIGURE 33-40: ADC1 CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010)



dsPIC33EPXXXGM3XX/6XX/7XX

PMCON (Parallel Master Port Control)	396	RPINR25 (Peripheral Pin Select Input 25).....	192
PMD1 (Peripheral Module Disable Control 1)	156	RPINR26 (Peripheral Pin Select Input 26).....	193
PMD2 (Peripheral Module Disable Control 2)	158	RPINR27 (Peripheral Pin Select Input 27).....	194
PMD3 (Peripheral Module Disable Control 3)	159	RPINR28 (Peripheral Pin Select Input 28).....	195
PMD4 (Peripheral Module Disable Control 4)	161	RPINR29 (Peripheral Pin Select Input 29).....	196
PMD6 (Peripheral Module Disable Control 6)	161	RPINR3 (Peripheral Pin Select Input 3).....	177
PMD7 (Peripheral Module Disable Control 7)	162	RPINR30 (Peripheral Pin Select Input 30).....	197
PMODE (Parallel Master Port Mode)	398	RPINR37 (Peripheral Pin Select Input 37).....	198
PMSTAT (Parallel Master Port Status)	402	RPINR38 (Peripheral Pin Select Input 38).....	199
POSxCNTH (Position Counter x High Word)	265	RPINR39 (Peripheral Pin Select Input 39).....	200
POSxCNTL (Position Counter x Low Word)	265	RPINR40 (Peripheral Pin Select Input 40).....	201
POSxHLD (Position Counter x Hold)	266	RPINR41 (Peripheral Pin Select Input 41).....	202
PTCON (PWMx Time Base Control)	233	RPINR7 (Peripheral Pin Select Input 7).....	178
PTCON2 (PWMx Primary Master Clock Divider Select 2)	235	RPINR8 (Peripheral Pin Select Input 8).....	179
PTGBTE (PTG Broadcast Trigger Enable)	354	RPINR9 (Peripheral Pin Select Input 9).....	180
PTGC0LIM (PTG Counter 0 Limit)	357	RPOR0 (Peripheral Pin Select Output 0).....	203
PTGC1LIM (PTG Counter 1 Limit)	358	RPOR1 (Peripheral Pin Select Output 1).....	203
PTGCON (PTG Control)	353	RPOR10 (Peripheral Pin Select Output 10).....	208
PTGCST (PTG Control/Status)	351	RPOR11 (Peripheral Pin Select Output 11).....	208
PTGHOLD (PTG Hold)	358	RPOR12 (Peripheral Pin Select Output 12).....	209
PTGSDLIM (PTG Step Delay Limit)	357	RPOR2 (Peripheral Pin Select Output 2).....	204
PTGT0LIM (PTG Timer0 Limit)	356	RPOR3 (Peripheral Pin Select Output 3).....	204
PTGT1LIM (PTG Timer1 Limit)	356	RPOR4 (Peripheral Pin Select Output 4).....	205
PTPER (PWMx Primary Master Time Base Period)	236	RPOR5 (Peripheral Pin Select Output 5).....	205
PWMCAPx (PWMx Primary Time Base Capture)	255	RPOR6 (Peripheral Pin Select Output 6).....	206
PWMCONx (PWMx Control)	242	RPOR7 (Peripheral Pin Select Output 7).....	206
QEIXCON (QEIX Control)	259	RPOR8 (Peripheral Pin Select Output 8).....	207
QEIXGECH (QEIX Greater Than or Equal Compare High Word)	270	RPOR9 (Peripheral Pin Select Output 9).....	207
QEIXGECL (QEIX Greater Than or Equal Compare Low Word)	270	RSCON (DCI Receive Slot Control)	348
QEIXICH (QEIX Initialization/Capture High Word)	268	RTCVAL (Minutes and Seconds Value, RTCPTR = 00)	390
QEIXICL (QEIX Initialization/Capture Low Word)	268	RTCVAL (Month and Day Value, RTCPTR = 10)	389
QEIXIOC (QEIX I/O Control)	261	RTCVAL (Weekday and Hours Value, RTCPTR = 01)	390
QEIXLECH (QEIX Less Than or Equal Compare High Word)	269	RTCVAL (Year Value, RTCPTR = 11)	389
QEIXLECL (QEIX Less Than or Equal Compare Low Word)	269	SDCx (PWMx Secondary Duty Cycle)	244
QEIXSTAT (QEIX Status)	263	SEVTCMP (PWMx Primary Special Event Compare)	236
RCFGCAL (RTCC Calibration and Configuration)	386	SPHASEx (PWMx Secondary Phase-Shift)	245
RCON (Reset Control)	112	SPIxCON1 (SPIx Control 1)	278
REFOCON (Reference Oscillator Control)	152	SPIxCON2 (SPIx Control 2)	280
RPINR0 (Peripheral Pin Select Input 0)	175	SPIxSTAT (SPIx Status and Control)	276
RPINR1 (Peripheral Pin Select Input 1)	176	SR (CPU STATUS)	31, 121
RPINR10 (Peripheral Pin Select Input 10)	181	SSEVTCMP (PWMx Secondary Special Event Compare)	240
RPINR11 (Peripheral Pin Select Input 11)	182	STCON (PWMx Secondary Time Base Control)	237
RPINR12 (Peripheral Pin Select Input 12)	183	STCON2 (PWMx Secondary Master Clock Divider Select 2)	239
RPINR14 (Peripheral Pin Select Input 14)	184	STPER (PWMx Secondary Master Time Base Period)	240
RPINR15 (Peripheral Pin Select Input 15)	185	T1CON (Timer1 Control)	212
RPINR16 (Peripheral Pin Select Input 16)	186	TRGCONx (PWMx Trigger Control)	247
RPINR17 (Peripheral Pin Select Input 17)	187	TRIGx (PWMx Primary Trigger Compare Value)	249
RPINR18 (Peripheral Pin Select Input 18)	188	TSCON (DCI Transmit Slot Control)	348
RPINR19 (Peripheral Pin Select Input 19)	188	TxCON (T2CON, T4CON, T6CON and T8CON Control)	216
RPINR22 (Peripheral Pin Select Input 22)	189	TyCON (T3CON, T5CON, T7CON and T9CON Control)	217
RPINR23 (Peripheral Pin Select Input 23)	190	UxMODE (UARTx Mode)	291
RPINR24 (Peripheral Pin Select Input 24)	191	UxSTA (UARTx Status and Control)	293
		VELxCNT (Velocity Counter x)	266