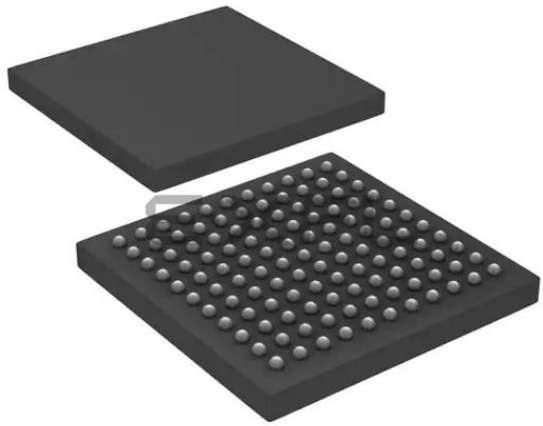
# Microchip Technology - DSPIC33EP128GM710-H/BG Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | - |
| Connectivity | CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | - |
| Data Converters | A/D 49x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 150°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 121-TFBGA |
| Supplier Device Package | 121-TFBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm710-h-bg |

**REGISTER 3-2: CORCON: CORE CONTROL REGISTER(3)**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VAR | — | US1 | US0 | EDT(1) | DL2 | DL1 | DL0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SATA | SATB | SATDW | ACCSAT | IPL3(2) | SFA | RND | IF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing latency is enabled
0 = Fixed exception processing latency is enabled

bit 14 **Unimplemented:** Read as '0'

bit 13-12 **US<1:0>:** DSP Multiply Unsigned/Signed Control bits
11 = Reserved
10 = DSP engine multiplies are mixed-sign
01 = DSP engine multiplies are unsigned
00 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit(1)
1 = Terminates executing DO loop at end of current loop iteration
0 = No effect

bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits
111 = 7 DO loops are active
•
•
•
001 = 1 DO loop is active
000 = 0 DO loops are active

bit 7 **SATA:** ACCA Saturation Enable bit
1 = Accumulator A saturation is enabled
0 = Accumulator A saturation is disabled

bit 6 **SATB:** ACCB Saturation Enable bit
1 = Accumulator B saturation is enabled
0 = Accumulator B saturation is disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit
1 = Data Space write saturation is enabled
0 = Data Space write saturation is disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

**Note 1:** This bit is always read as '0'.
**2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.
**3:** Refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"CPU"** (DS70359) for more detailed information.

**TABLE 4-46: PORTA REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 0E00 | TRISA<15:14> | | — | TRISA<12:7> | | | | | | — | — | TRISA4 | — | — | TRISA<1:0> | | DF9F |
| PORTA | 0E02 | RA<15:14> | | — | RA<12:7> | | | | | | — | — | RA4 | — | — | RA<1:0> | | 0000 |
| LATA | 0E04 | LATA<15:14> | | — | LATA<12:7> | | | | | | — | — | LATA4 | — | — | LATA<1:0> | | 0000 |
| ODCA | 0E06 | ODCA<15:14> | | — | ODCA<12:7> | | | | | | — | — | ODCA4 | — | — | ODCA<1:0> | | 0000 |
| CNENA | 0E08 | CNIEA<15:14> | | — | CNIEA<12:7> | | | | | | — | — | CNIEA4 | — | — | CNIEA<1:0> | | 0000 |
| CNPUA | 0E0A | CNPUA<15:14> | | — | CNPUA<12:7> | | | | | | — | — | CNPUA4 | — | — | CNPUA<1:0> | | 0000 |
| CNPDA | 0E0C | CNPDA<15:14> | | — | CNPDA<12:7> | | | | | | — | — | CNPDA4 | — | — | CNPDA<1:0> | | 0000 |
| ANSELA | 0E0E | ANSA<15:14> | | — | ANSA<12:11> | | — | ANSA9 | — | — | — | — | ANSA4 | — | — | ANSA<1:0> | | 1813 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-47: PORTA REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 0E00 | — | — | — | TRISA<12:7> | | | | | | — | — | TRISA4 | — | — | TRISA<1:0> | | DF9F |
| PORTA | 0E02 | — | — | — | RA<12:7> | | | | | | — | — | RA4 | — | — | RA<1:0> | | 0000 |
| LATA | 0E04 | — | — | — | LATA<12:7> | | | | | | — | — | LATA4 | — | — | LATA<1:0> | | 0000 |
| ODCA | 0E06 | — | — | — | ODCA<12:7> | | | | | | — | — | ODCA4 | — | — | ODCA<1:0> | | 0000 |
| CNENA | 0E08 | — | — | — | CNIEA<12:7> | | | | | | — | — | CNIEA4 | — | — | CNIEA<1:0> | | 0000 |
| CNPUA | 0E0A | — | — | — | CNPUA<12:7> | | | | | | — | — | CNPUA4 | — | — | CNPUA<1:0> | | 0000 |
| CNPDA | 0E0C | — | — | — | CNPDA<12:7> | | | | | | — | — | CNPDA4 | — | — | CNPDA<1:0> | | 0000 |
| ANSELA | 0E0E | — | — | — | ANSA<12:11> | | — | ANSA9 | — | — | — | — | ANSA4 | — | — | ANSA<1:0> | | 1813 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-48: PORTA REGISTER MAP FOR dsPIC33EPXXXGM304/604 DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 0E00 | — | — | — | — | — | TRISA<10:7> | | | | — | — | TRISA<4:0> | | | | | DF9F |
| PORTA | 0E02 | — | — | — | — | — | RA<10:7> | | | | — | — | RA<4:0> | | | | | 0000 |
| LATA | 0E04 | — | — | — | — | — | LATA<10:7> | | | | — | — | LATA<4:0> | | | | | 0000 |
| ODCA | 0E06 | — | — | — | — | — | ODCA<10:7> | | | | — | — | ODCA<4:0> | | | | | 0000 |
| CNENA | 0E08 | — | — | — | — | — | CNIEA<10:7> | | | | — | — | CNIEA<4:0> | | | | | 0000 |
| CNPUA | 0E0A | — | — | — | — | — | CNPUA<10:7> | | | | — | — | CNPUA<4:0> | | | | | 0000 |
| CNPDA | 0E0C | — | — | — | — | — | CNPDA<10:7> | | | | — | — | CNPDA<4:0> | | | | | 0000 |
| ANSELA | 0E0E | — | — | — | — | — | — | ANSA9 | — | — | — | — | ANSA4 | — | ANSA<2:0> | | | 1813 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 7-7: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | ILR3 | ILR2 | ILR1 | ILR0 |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VECNUM7 | VECNUM6 | VECNUM5 | VECNUM4 | VECNUM3 | VECNUM2 | VECNUM1 | VECNUM0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as ‘0’

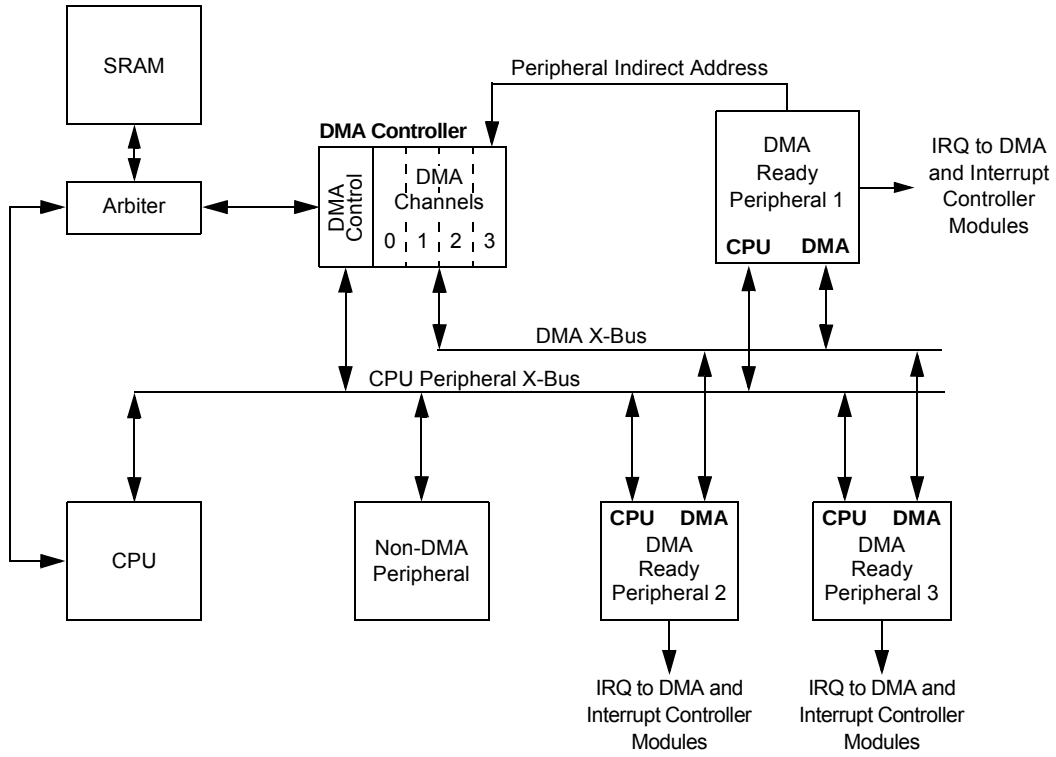
bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits
1111 = CPU Interrupt Priority Level is 15
•
•
•
0001 = CPU Interrupt Priority Level is 1
0000 = CPU Interrupt Priority Level is 0

bit 7-0 **VECNUM<7:0>:** Vector Number of Pending Interrupt bits
11111111 = 255, Reserved; do not use
•
•
•
00001001 = 9, IC1 – Input Capture 1
00001000 = 8, INT0 – External Interrupt 0
00000111 = 7, Reserved; do not use
00000110 = 6, Generic soft error trap
00000101 = 5, DMA Controller error trap
00000100 = 4, Math error trap
00000011 = 3, Stack error trap
00000010 = 2, Generic hard trap
00000001 = 1, Address error trap
00000000 = 0, Oscillator fail trap

**TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS (CONTINUED)**

| Peripheral to DMA Association | DMAxREQ Register IRQSEL<7:0> Bits | DMAxPAD Register (Values to Read from Peripheral) | DMAxPAD Register (Values to Write to Peripheral) |
|---|---|---|---|
| CAN1 – RX Data Ready | 00100010 | 0x0440 (C1RXD) | — |
| CAN1 – TX Data Request | 01000110 | — | 0x0442 (C1TXD) |
| CAN2 – RX Data Ready | 00110111 | 0X0540(C2RXD) | — |
| CAN2 – TX Data Request | 01000111 | — | 0X0542(C2TXD) |
| DCI – Codec Transfer Done | 00111100 | 0X0290(RXBUF0) | 0X0298(TXBUF0) |
| ADC1 – ADC1 Convert Done | 00001101 | 0x0300 (ADC1BUF0) | — |
| ADC2 – ADC2 Convert Done | 00010101 | 0X0340(ADC2BUF0) | — |
| PMP – PMP Data Move | 00101101 | 0X0608(PMPDAT1) | 0X0608(PMPDAT1) |

**FIGURE 8-2: DMA CONTROLLER BLOCK DIAGRAM**




**Note:** CPU and DMA address buses are not shown for clarity.

**REGISTER 16-9: CHOP: PWMx CHOP CLOCK GENERATOR REGISTER**

| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CHPCLKEN | — | — | — | — | — | CHOPCLK9 | CHOPCLK8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CHOPCLK7 | CHOPCLK6 | CHOPCLK5 | CHOPCLK4 | CHOPCLK3 | CHOPCLK2 | CHOPCLK1 | CHOPCLK0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **CHPCLKEN:** Enable Chop Clock Generator bit
1 = Chop clock generator is enabled
0 = Chop clock generator is disabled

bit 14-10 **Unimplemented:** Read as ‘0’

bit 9-0 **CHOPCLK<9:0>:** Chop Clock Divider bits
The frequency of the chop clock signal is given by the following expression:
Chop Frequency = (FP/PCLKDIV<2:0>)/(CHOP<9:0> + 1)

**REGISTER 16-10: MDC: PWMx MASTER DUTY CYCLE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MDC<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MDC<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **MDC<15:0>:** PWMx Master Duty Cycle Value bits

**REGISTER 16-25: PWMCAPx: PWMx PRIMARY TIME BASE CAPTURE REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PWMCAPx<15:8>(1,2) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PWMCAPx<7:0>(1,2) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PWMCAPx<15:0>:** PWMx Captured Time Base Value bits(1,2)
The value in this register represents the captured PWMx time base value when a leading edge is detected on the current-limit input.

**Note 1:** The capture feature is only available on a primary output (PWMxH).
**2:** This feature is active only after LEB processing on the current-limit input signal is complete.

**REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)**

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as $I^2C$ slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as $I^2C$ master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as $I^2C$ master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; hardware clears at the end of the master Acknowledge sequence
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as $I^2C$ master)
1 = Enables Receive mode for $I^2C$; hardware clears at the end of the eighth bit of a master receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as $I^2C$ master)
1 = Initiates Stop condition on SDAx and SCLx pins; hardware clears at the end of a master Stop sequence
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as $I^2C$ master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware clears at the end of a master Repeated Start sequence
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as $I^2C$ master)
1 = Initiates Start condition on SDAx and SCLx pins; hardware clears at the end of a master Start sequence
0 = Start condition is not in progress

**Note 1:** When performing master operations, ensure that the IPMIEN bit is set to '0'.

**REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receive buffer and the UxRSR to the empty state

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

**Note 1:** Refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) for information on enabling the UART module for transmit operation.

**REGISTER 21-11: CxFEN1: CANx ACCEPTANCE FILTER ENABLE REGISTER 1**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| FLTEN<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| FLTEN<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **FLTEN<15:0>:** Enable Filter n to Accept Messages bits
1 = Enables Filter n
0 = Disables Filter n

**REGISTER 21-12: CxBUFPNT1: CANx FILTERS 0-3 BUFFER POINTER REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F3BP3 | F3BP2 | F3BP1 | F3BP0 | F2BP3 | F2BP2 | F2BP1 | F2BP0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F1BP3 | F1BP2 | F1BP1 | F1BP0 | F0BP3 | F0BP2 | F0BP1 | F0BP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **F3BP<3:0>:** RX Buffer Mask for Filter 3 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP<3:0>:** RX Buffer Mask for Filter 2 bits (same values as bits 15-12)

bit 7-4 **F1BP<3:0>:** RX Buffer Mask for Filter 1 bits (same values as bits 15-12)

bit 3-0 **F0BP<3:0>:** RX Buffer Mask for Filter 0 bits (same values as bits 15-12)

**REGISTER 24-5: RSCON: DCI RECEIVE SLOT CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| RSE<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| RSE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **RSE<15:0>:** DCI Receive Slot Enable bits
1 = CSDI data is received during Individual Time Slot n
0 = CSDI data is ignored during Individual Time Slot n

**REGISTER 24-6: TSCON: DCI TRANSMIT SLOT CONTROL REGISTER**

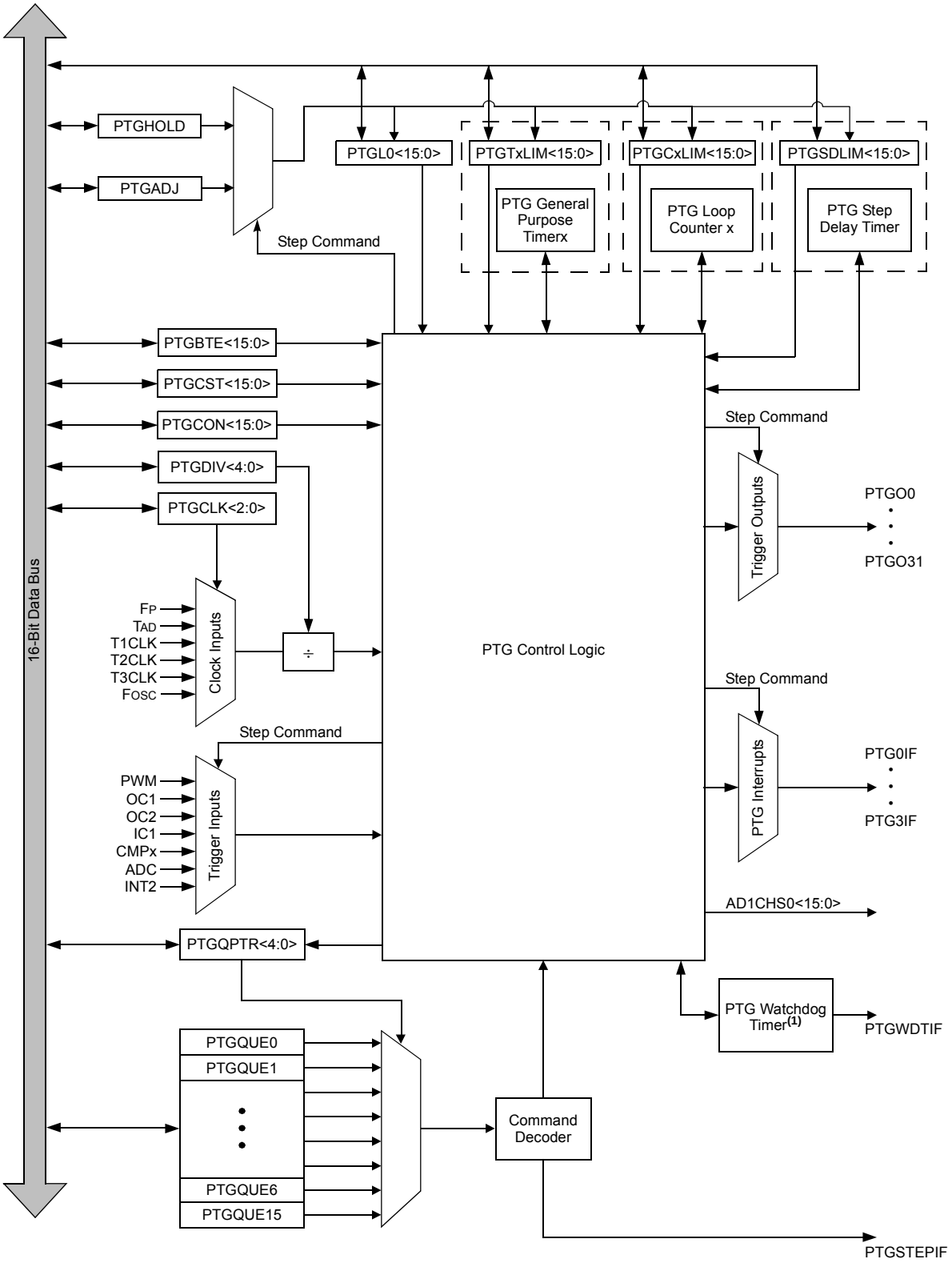
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TSE<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TSE<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **TSE<15:0>:** DCI Transmit Slot Enable Control bits
1 = Transmit buffer contents are sent during Individual Time Slot n
0 = CSDO pin is tri-stated or driven to logic ‘0’ during the individual time slot, depending on the state of the CSDOM bit

**FIGURE 25-1: PTG BLOCK DIAGRAM**




**Note 1:** This is a dedicated Watchdog Timer for the PTG module and is independent of the device Watchdog Timer.

**REGISTER 25-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | PTGQPTR<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits
This register points to the currently active Step command in the step queue.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**REGISTER 25-13: PTGQUEx: PTG STEP QUEUE REGISTER x (x = 0-15)(1,3)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STEP(2x + 1)<7:0>(2) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STEP(2x)<7:0>(2) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **STEP(2x + 1)<7:0>:** PTG Step Queue Pointer Register bits(2)
A queue location for storage of the STEP(2x +1) command byte.

bit 7-0 **STEP(2x)<7:0>:** PTG Step Queue Pointer Register bits(2)
A queue location for storage of the STEP(2x) command byte.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**2:** Refer to Table 25-1 for the Step command encoding.

**3:** The Step registers maintain their values on any type of Reset.

**REGISTER 26-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | RW-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | SELSRCC3 | SELSRCC2 | SELSRCC1 | SELSRCC0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-8 **SELSRCC<3:0>:** Mask C Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 7-4 **SELSRCB<3:0>:** Mask B Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

**REGISTER 27-3: ALCFGRPT: ALARM CONFIGURATION REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ALRMEN | CHIME | AMASK3 | AMASK2 | AMASK1 | AMASK0 | ALRMPTR1 | ALRMPTR0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ARPT7 | ARPT6 | ARPT5 | ARPT4 | ARPT3 | ARPT2 | ARPT1 | ARPT0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ALRMEN:** Alarm Enable bit

1 = Alarm is enabled (cleared automatically after an alarm event whenever ARPT<7:0> = 0x00 and CHIME = 0)
0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit

1 = Chime is enabled; ARPT<7:0> bits are allowed to roll over from 0x00 to 0xFF
0 = Chime is disabled; ARPT<7:0> bits stop once they reach 0x00

bit 13-10 **AMASK<3:0>:** Alarm Mask Configuration bits

0000 = Every half second
0001 = Every second
0010 = Every 10 seconds
0011 = Every minute
0100 = Every 10 minutes
0101 = Every hour
0110 = Once a day
0111 = Once a week
1000 = Once a month
1001 = Once a year (except when configured for February 29th, once every 4 years)
101x = Reserved – do not use
11xx = Reserved – do not use

bit 9-8 **ALRMPTR<1:0>:** Alarm Value Register Window Pointer bits

Points to the corresponding Alarm Value registers when reading the ALRMVAL register. The ALRMPTR<1:0> value decrements on every read or write of ALRMVAL until it reaches '00'.

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits

11111111 = Alarm will repeat 255 more times
•
•
•
00000000 = Alarm will not repeat

The counter decrements on any alarm event. The counter is prevented from rolling over from 0x00 to 0xFF unless CHIME = 1.

**FIGURE 33-12: TIMERQ (QEIx MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS**

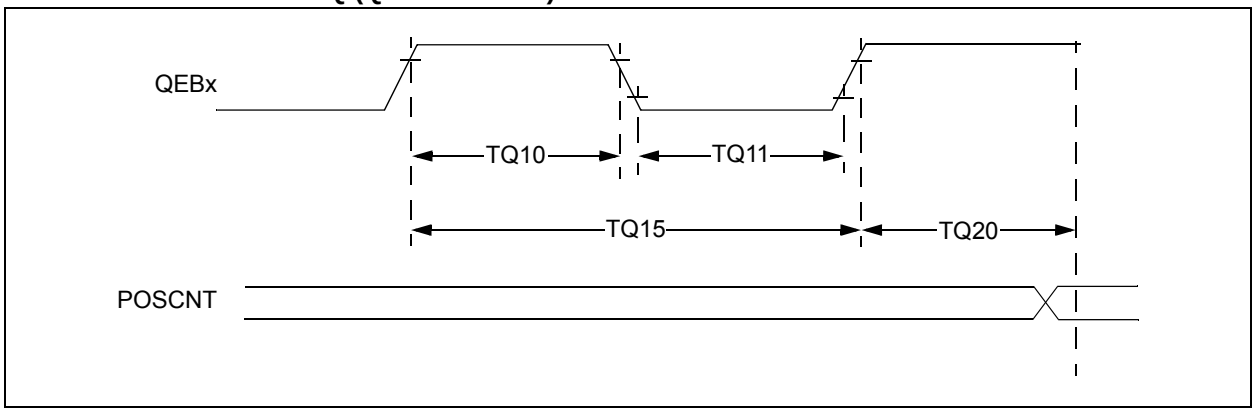



**TABLE 33-29: QEIx MODULE EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TQ10 | TtQH | TQCK High Time | Synchronous, with Prescaler | Greater of: 12.5 + 25 or (0.5 TCY/N) + 25 | — | — | ns | Must also meet Parameter TQ15 |
| TQ11 | TtQL | TQCK Low Time | Synchronous, with Prescaler | Greater of: 12.5 + 25 or (0.5 TCY/N) + 25 | — | — | ns | Must also meet Parameter TQ15 |
| TQ15 | TtQP | TQCP Input Period | Synchronous, with Prescaler | Greater of: 25 + 50 or (1 TCY/N) + 50 | — | — | ns | |
| TQ20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | — | 1 | TCY | — | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**TABLE 33-60: ADCx CONVERSION (10-BIT MODE) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(4)** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| AD50 | TAD | ADCx Clock Period | 75 | — | — | ns | |
| AD51 | tRC | ADCx Internal RC Oscillator Period | — | 250 | — | ns | |
| **Conversion Rate** | | | | | | | |
| AD55 | tCONV | Conversion Time | — | 12 TAD | — | — | |
| AD56 | FCNV | Throughput Rate | — | — | 1.1 | Msps | Using simultaneous sampling |
| AD57a | TSAMP | Sample Time When Sampling Any ANx Input | 2 TAD | — | — | — | |
| AD57b | TSAMP | Sample Time When Sampling the Op Amp Outputs | 4 TAD | — | — | — | |
| **Timing Parameters** | | | | | | | |
| AD60 | tPCS | Conversion Start from Sample Trigger(2) | 2 TAD | — | 3 TAD | — | Auto-convert trigger not selected |
| AD61 | tPSS | Sample Start from Setting Sample (SAMP) bit(2) | 2 TAD | — | 3 TAD | — | |
| AD62 | tCSS | Conversion Completion to Sample Start (ASAM = 1)(2) | — | 0.5 TAD | — | — | |
| AD63 | tDPU | Time to Stabilize Analog Stage from ADC Off to ADC On(2) | — | — | 20 | μs | **(Note 3)** |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

**2:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

**3:** The parameter, tDPU, is the time required for the ADCx module to stabilize at the appropriate level when the module is turned on (AD1CON1<ADON> = 1). During this time, the ADCx result is indeterminate.

**4:** These parameters are characterized, but not tested in manufacturing.

**TABLE 33-61: DMA MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| DM1 | DMA Byte/Word Transfer Latency | 1 TCY(2) | — | — | ns | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.

**TABLE 34-14: ADCx MODULE SPECIFICATIONS (12-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions |
| **ADC Accuracy (12-Bit Mode)(1)** | | | | | | | |
| HAD20a | Nr | Resolution(3) | 12 Data Bits | | | bits | |
| HAD21a | INL | Integral Nonlinearity | -6 | — | 6 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD22a | DNL | Differential Nonlinearity | -1 | — | 1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD23a | GERR | Gain Error | -10 | — | 10 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD24a | EOFF | Offset Error | -5 | — | 5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| **Dynamic Performance (12-Bit Mode)(2)** | | | | | | | |
| HAD33a | FNYQ | Input Signal Bandwidth | — | — | 200 | kHz | |

**Note 1:** These parameters are characterized, but are tested at 20 ksps only.

**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

**3:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**TABLE 34-15: ADCx MODULE SPECIFICATIONS (10-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions |
| **ADC Accuracy (10-Bit Mode)(1)** | | | | | | | |
| HAD20b | Nr | Resolution(3) | 10 Data Bits | | | bits | |
| HAD21b | INL | Integral Nonlinearity | -1.5 | — | 1.5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD22b | DNL | Differential Nonlinearity | -0.25 | — | 0.25 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD23b | GERR | Gain Error | -2.5 | — | 2.5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD24b | EOFF | Offset Error | -1.25 | — | 1.25 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| **Dynamic Performance (10-Bit Mode)(2)** | | | | | | | |
| HAD33b | FNYQ | Input Signal Bandwidth | — | — | 400 | kHz | |

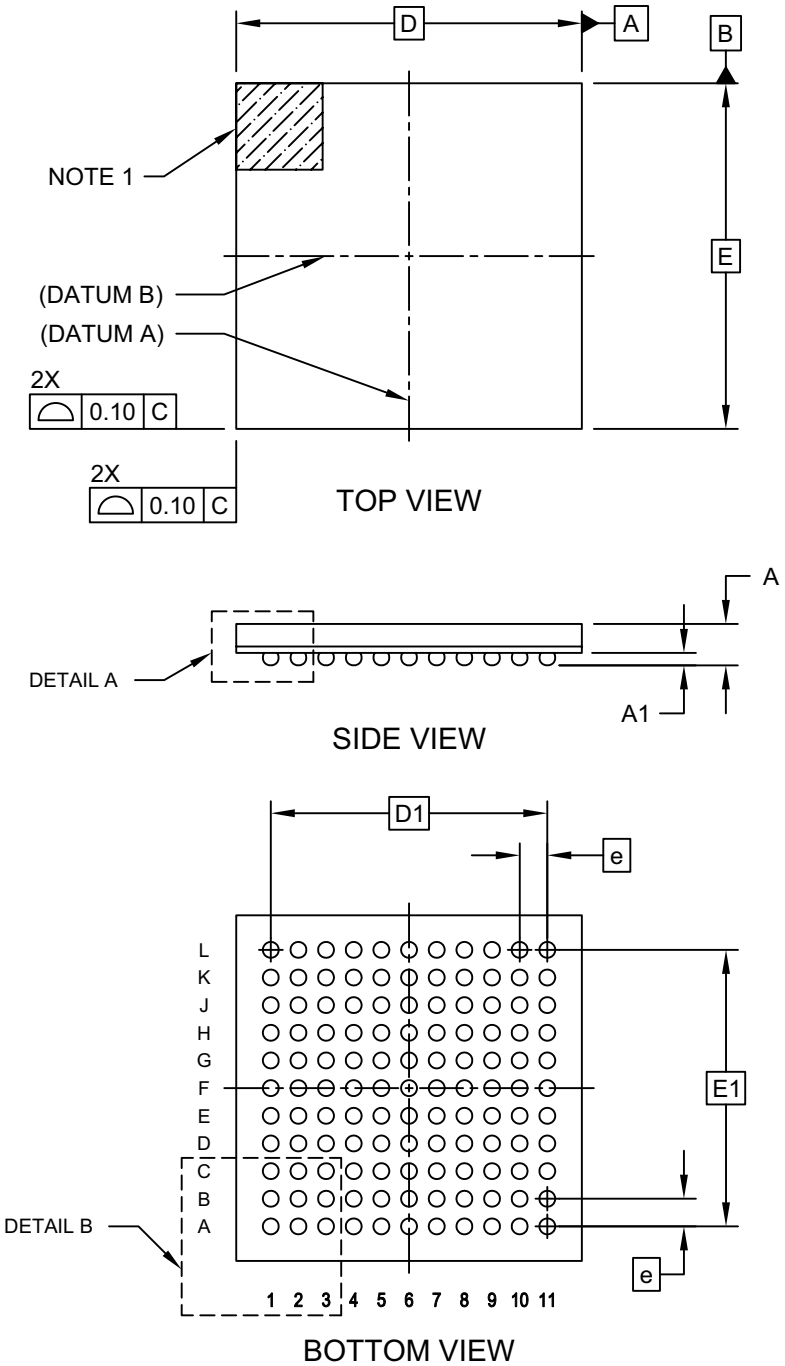
**Note 1:** These parameters are characterized, but are tested at 20 ksps only.

**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

**3:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**121-Ball Plastic Thin Profile Fine Pitch Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA]**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-148 Rev F Sheet 1 of 2

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