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### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm710t-i-pf

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TABLE 4-6:	OUTPUT COMPARE REGISTER MAP (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC7CON1	093C	_	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	_	ENFLTB	ENFLTA	_	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC7CON2	093E	FLTMD	FLTOUT	FLTTRIEN	OCINV		—		OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC7RS	0940							Ou	tput Comp	are 7 Seco	ondary Regis	ter						xxxx
OC7R	0942								Output	Compare 7	' Register							xxxx
OC7TMR	0944							Out	put Compa	are 7 Time	r Value Regis	ster						xxxx
OC8CON1	0946		—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0		ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC8CON2	0948	FLTMD	FLTOUT	FLTTRIEN	OCINV		_		OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC8RS	094A							Ou	tput Comp	are 8 Seco	ondary Regis	ter						xxxx
OC8R	094C		Output Compare 8 Register xxxx										xxxx					
OC8TMR	094E		Output Compare 8 Timer Value Register xxxx															

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

### TABLE 4-46: PORTA REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES

								1			1		1		1		(	1
SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	TRISA	<15:14>	—			TRISA<	12:7>			—	—	TRISA4	-	—	TRISA	<1:0>	DF9F
PORTA	0E02	RA<1	5:14>	_			RA<12	2:7>			_	_	RA4	_	_	RA<	1:0>	0000
LATA	0E04	LATA<	15:14>	_			LATA<1	2:7>			_	_	LATA4	_	_	LATA	<1:0>	0000
ODCA	0E06	ODCA<	<15:14>	_			ODCA<	12:7>			_	_	ODCA4	_	_	ODCA	<1:0>	0000
CNENA	0E08	CNIEA	<15:14>	_			CNIEA<	12:7>			_	_	CNIEA4	_	_	CNIEA	<1:0>	0000
CNPUA	0E0A	CNPUA	<15:14>	_		CNPUA<12:7>					_	_	CNPUA4	_	_	CNPU	4<1:0>	0000
CNPDA	0E0C	CNPDA	<15:14>			CNPDA<12:7>				_	_	CNPDA4	_	_	CNPD	4<1:0>	0000	
ANSELA	0E0E	ANSA<	<15:14>	_	ANSA<	12:11>		ANSA9	_	_	_	_	ANSA4		_	ANSA	<1:0>	1813

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## TABLE 4-47: PORTA REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00		—	_			TRISA<	12:7>				—	TRISA4	_	—	TRISA	<1:0>	DF9F
PORTA	0E02	—	—	_			RA<12	:7>			_	_	RA4	-	—	RA<	1:0>	0000
LATA	0E04	—	_				LATA<1	2:7>			_	_	LATA4		_	LATA	<1:0>	0000
ODCA	0E06	—	—	_			ODCA<	12:7>			_	—	ODCA4	-	—	ODCA	<1:0>	0000
CNENA	0E08	—	—				CNIEA<	12:7>			—	_	CNIEA4		_	CNIEA	<1:0>	0000
CNPUA	0E0A	—	_				CNPUA<	12:7>			_	_	CNPUA4		_	CNPU	4<1:0>	0000
CNPDA	0E0C	—	—			CNPDA<12:7					_	—	CNPDA4		—	CNPD	۹<1:0>	0000
ANSELA	0E0E	_	_		ANSA<	12:11>	_	ANSA9	_		_	_	ANSA4		_	ANSA	<1:0>	1813

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## TABLE 4-48: PORTA REGISTER MAP FOR dsPIC33EPXXXGM304/604 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	_	_	_	_	_		TRISA	<10:7>		_	_		-	TRISA<4:0	>		DF9F
PORTA	0E02	_	_	_	-	—		RA<1	0:7>		—	_			RA<4:0>			0000
LATA	0E04	_	_	_	_	—		LATA<	10:7>		—	_			LATA<4:0>			0000
ODCA	0E06	_	_	_	_	—		ODCA.	<10:7>		—	_		(	ODCA<4:0	>		0000
CNENA	0E08	—	_	—	—	—		CNIEA	<10:7>		_	—		(	CNIEA<4:0	>		0000
CNPUA	0E0A	_	_	_	_	—		CNPUA	<10:7>		—	_	CNPUA<4:0>			0000		
CNPDA	0E0C	_	_	_	_	_	CNPDA<10:7>		_	_	CNPDA<4:0>			0000				
ANSELA	0E0E	_	_	_	_	_	_	ANSA9	_	_	_	_	ANSA4	_		ANSA<2:0>	>	1813

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## REGISTER 8-5: DMAXSTBH: DMA CHANNEL X START ADDRESS REGISTER B (HIGH)

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	_	—	—	—	—
bit 15	-						bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STB<	23:16>			
bit 7							bit 0
l egend:							

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 STB<23:16>: DMA Secondary Start Address bits (source or destination)

#### REGISTER 8-6: DMAXSTBL: DMA CHANNEL X START ADDRESS REGISTER B (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STB	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STE	3<7:0>			
bit 7							bit 0
Legend:							
R = Readable b	oit	W = Writable b	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 **STB<15:0>:** DMA Secondary Start Address bits (source or destination)

# 11.0 I/O PORTS

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33/PIC24 Family Reference Manual", "I/O Ports" (DS70000598) which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the Parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

# 11.1 Parallel I/O (PIO) Ports

Generally, a Parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the Data Direction register bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device are disabled. This means the corresponding LATx and TRISx registers, and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.



## FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE

## 11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-29). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

#### FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



## 11.4.4.1 Virtual Connections

dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 26-1 in Section 26.0 "Op Amp/Comparator Module") and the PTG module (see Section 25.0 "Peripheral Trigger Generator (PTG) Module").

In addition, dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual connections to the filtered QEIx module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in Section 17.0 "Quadrature Encoder Interface (QEI) Module").

Virtual connections provide a simple way of interperipheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of `b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEIx module allows peripherals to be connected to the QEIx digital filter input. To utilize this filter, the QEIx module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEIx digital filter.

## EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43

RPINR15 = 0x2500; RPINR7 = 0x009;	/* /*	Connect Connect	the the	QEI IC1	1 HOME: input	l input to the	to RP37 digital	(pin 43 filter	) */ on th	e FHOME1	input	*/
QEI1IOC = 0x4000; QEI1CON = 0x8000;	/* /*	Enable t Enable t	the Q the Q	2EI 2EI	digita: module	l filte: */	r */					

Input Name <sup>(1)</sup>	Function Name	Register	Configuration Bits
input Italito		Regional	eeningalaalen Elle
PWM Sync Input 1	SYNCI1	RPINR37	SYNCI1R<6:0>
PWM Dead-Time Compensation 1	DTCMP1	RPINR38	DTCMP1R<6:0>
PWM Dead-Time Compensation 2	DTCMP2	RPINR39	DTCMP2R<6:0>
PWM Dead-Time Compensation 3	DTCMP3	RPINR39	DTCMP3R<6:0>
PWM Dead-Time Compensation 4	DTCMP4	RPINR40	DTCMP4R<6:0>
PWM Dead-Time Compensation 5	DTCMP5	RPINR40	DTCMP5R<6:0>
PWM Dead-Time Compensation 6	DTCMP6	RPINR41	DTCMP6R<6:0>

## TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION) (CONTINUED)

**Note 1:** Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input is available on dsPIC33EPXXXGM6XX/7XX devices only.

NOTES:

# REGISTER 13-2: TyCON (T3CON, T5CON, T7CON AND T9CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON <sup>(1)</sup>	—	TSIDL <sup>(2)</sup>	—	—	—	—	_
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE <sup>(1)</sup>	TCKPS1 <sup>(1)</sup>	TCKPS0 <sup>(1)</sup>	-	—	TCS <sup>(1,3)</sup>	—
bit 7							bit 0
Legend:							

-				
R = Readable bit		W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value at POR		'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 15	TON: Tir	nery On bit <sup>(1)</sup>		
	1 = Start	s 16-bit Timery		
	0 = Stops	s 16-bit Timery		
bit 14	Unimple	mented: Read as '0'		
bit 13	TSIDL: 1	Timery Stop in Idle Mode bit	2)	
	1 = Disco	ontinues module operation v	when device enters Idle mode	
	0 = Cont	inues module operation in lo	dle mode	
bit 12-7	Unimple	mented: Read as '0'		
bit 6	TGATE:	Timery Gated Time Accumu	llation Enable bit <sup>(1)</sup>	
	When TO	<u> CS = 1:</u>		
	This bit is	s ignored.		
	When TO	<u>CS = 0:</u>	1.1	
	1 = Gate	d time accumulation is enact		
bit 5 1			concele Select hite(1)	
DIL 3-4	11 - 1.2	Se	escale Select bits.	
	11 = 1.23 10 = 1.64	4		
	01 = 1:8			
	00 = 1:1			
bit 3-2	Unimple	mented: Read as '0'		
bit 1	TCS: Tin	nery Clock Source Select bit	<sub>(</sub> (1,3)	
	1 = Exte	rnal clock from pin, TyCK (or	n the rising edge)	
	0 = Inter	nal clock (FP)		
bit 0	Unimple	mented: Read as '0'		
Note 1:	When 32-bit of functions are	peration is enabled (T2CON set through TxCON.	I<3> = 1), these bits have no ef	ffect on Timery operation; all timer

2: When 32-bit timer operation is enabled (T32 = 1) in the Timerx Control register (TxCON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

3: The TyCK pin is not available on all timers. See the "Pin Diagrams" section for the available pins.

### REGISTER 16-5: STCON: PWMx SECONDARY TIME BASE CONTROL REGISTER (CONTINUED)

- **Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.
  - 2: See Section 25.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

NOTES:

#### FIGURE 17-1: QEIX BLOCK DIAGRAM



JSPIC33EPXXXGM3XX/6XX/7XX

-							
U-0	U-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
_	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
bit 15							bit 8
HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
PCIIRQ <sup>(1)</sup>	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
bit 7	-		•			-	bit C
Legend:		HS = Hardware	e Settable bit	C = Clearable	e bit		
R = Readable	e bit	W = Writable b	bit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15-14	Unimpleme	nted: Read as '	כ'				
bit 13	PCHEQIRQ	: Position Count	er Greater Tha	n or Equal Cor	npare Status bi	t	
	1 = POSxCN	NT ≥ QEIxGEC					
	0 = POSxCN	NT < QEIXGEC					
bit 12	PCHEQIEN:	Position Counter	er Greater Tha	n or Equal Con	npare Interrupt	Enable bit	
	1 = Interrupt	is enabled					
<b>b</b> :+ 44			ar Loop Them a		are Otetus hit		
DICTI			er Less Than o	r Equal Compa	are Status bit		
	1 = POSXCN 0 = POSXCN	T = QEIXLEC					
bit 10	PCLEQIEN:	Position Counte	er Less Than o	r Equal Compa	are Interrupt En	able bit	
	1 = Interrupt	is enabled					
	0 = Interrupt	is disabled					
bit 9	POSOVIRQ	: Position Count	er Overflow Sta	atus bit			
	1 = Overflow	has occurred					
		now has occurre					
DIT 8	POSOVIEN:	Position Counter	er Overflow Int	errupt Enable t	DIT		
	$\perp = Interrupt$ 0 = Interrupt	is disabled					
bit 7	PCIIRQ: Pos	sition Counter (F	lomina) Initializ	vation Process	Complete Stati	us hit(1)	
SICT	1 = POSxCN	NT was reinitializ	ed		Complete clat		
	0 = POSxCN	NT was not reinit	ialized				
bit 6	PCIIEN: Pos	sition Counter (H	loming) Initializ	ation Process	Complete inter	rupt Enable bit	
	1 = Interrupt	is enabled					
	0 = Interrupt	is disabled					
bit 5	VELOVIRQ: Velocity Counter Overflow Status bit						
	1 = Overflow	v has occurred	d				
bit 4			u r Ovorflow Inte	rrunt Enghla b	:+		
DIL 4	1 = Interrunt is enabled						
	0 = Interrupt	is disabled					
bit 3	HOMIRQ: S	tatus Flag for Ho	ome Event Stat	us bit			
	1 = Home ev	vent has occurre	d				
	0 = No home	e event has occu	urred				

#### REGISTER 17-3: QEIxSTAT: QEIx STATUS REGISTER

**Note 1:** This status bit is only applicable to PIMOD<2:0> = 011 and 100 modes.

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE <sup>(1)</sup>
bit 15							bit 8
R/W-0	) R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN	<sup>2)</sup> CKP	MSTEN	SPRE2 <sup>(3)</sup>	SPRE1 <sup>(3)</sup>	SPRE0 <sup>(3)</sup>	PPRE1 <sup>(3)</sup>	PPRE0 <sup>(3)</sup>
bit 7							bit 0
Legend:			1.11				
R = Read	able bit	W = Writable	bit		nented bit, read		
-n = Value	e at POR	'1' = Bit is set		$0^{\circ}$ = Bit is cle	ared	x = Bit is unkr	lown
hit 15 12	Unimplomon	tod. Dood oo '	0'				
bit 12		abla SCKy Din	∪ bit (SPI Maste	or modes only)			
DIL 12	1 = Internal S	PI clock is dis	abled nin func	tions as I/O			
	0 = Internal S	PI clock is ena	bled				
bit 11	DISSDO: Dis	able SDOx Pin	bit				
	1 = SDOx pin	is not used by	the module; p	oin functions as	s I/O		
	0 = SDOx pin	is controlled b	y the module				
bit 10	MODE16: Wo	ord/Byte Comm	unication Sele	ect bit			
	1 = Communi 0 = Communi	ication is word-	wide (16 bits) wide (8 bits)				
bit 9	SMP: SPIX D	ata Input Sam	ble Phase bit				
	Master mode	:					
	1 = Input data	is sampled at	the end of dat	ta output time			
	0 = Input data	a is sampled at	the middle of	data output tin	ne		
	Slave mode: SMP must be	cleared when	SPIx is used i	n Slave mode.			
bit 8	CKE: SPIx C	lock Edge Sele	ect bit <sup>(1)</sup>				
	1 = Serial out	put data chang	es on transitio	on from active	clock state to Id	le clock state (	refer to bit 6)
	0 = Serial out	put data chang	es on transitio	on from Idle clo	ock state to activ	ve clock state (	refer to bit 6)
bit 7	SSEN: Slave	Select Enable	bit (Slave mo	de) <sup>(2)</sup>			
	$1 = \overline{SSx}$ pin is used for Slave mode						
hit 6	0 = SSX piri is	olarity Soloct I	ne module, pli sit		by port function		
1 =  d e  state for clock is a high level: active state is a low level							
0 = Idle state for clock is a low level; active state is a high level							
bit 5	MSTEN: Mas	ter Mode Enat	ole bit				
1 = Master mode							
	0 = Slave mo	de					
Note 1:	The CKE bit is not	used in Frame	d SPI modes. I	Program this bi	it to '0' for Frame	ed SPI modes (	FRMEN = 1).
2:	This bit must be cl	eared when FF	RMEN = 1.	-		·	,

### REGISTER 18-2: SPIXCON1: SPIX CONTROL REGISTER 1

**3:** Do not set both primary and secondary prescalers to the value of 1:1.

# 25.0 PERIPHERAL TRIGGER GENERATOR (PTG) MODULE

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33/PIC24 Family Reference Manual", "Peripheral Trigger Generator (PTG)" (DS70669), which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

# 25.1 Module Introduction

The Peripheral Trigger Generator (PTG) provides a means to schedule complex, high-speed peripheral operations that would be difficult to achieve using software. The PTG module uses 8-bit commands, called "steps", that the user writes to the PTG Queue register (PTGQUE0-PTQUE15), which performs operations, such as wait for input signal, generate output trigger and wait for timer.

The PTG module has the following major features:

- Multiple Clock Sources
- Two 16-Bit General Purpose Timers
- Two 16-Bit General Limit Counters
- Configurable for Rising or Falling Edge Triggering
- Generates Processor Interrupts to Include:
  - Four configurable processor interrupts
  - Interrupt on a step event in Single-Step modeInterrupt on a PTG Watchdog Timer time-out
- Able to Receive Trigger Signals from these Peripherals:
  - ADC
  - PWM
  - Output Compare
  - Input Capture
  - Op Amp/Comparator
  - INT2
- Able to Trigger or Synchronize to these Peripherals:
- Watchdog Timer
- Output Compare
- Input Capture
- ADC
- PWM
- Op Amp/Comparator

### **REGISTER 25-6: PTGSDLIM: PTG STEP DELAY LIMIT REGISTER**<sup>(1,2)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
1011 0	1411 0	1011 0		IM <15:05	1011 0	1011 0	
			PIGSDL	10:82			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGSDI	_IM<7:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGSDLIM<15:0>:** PTG Step Delay Limit Register bits Holds a PTG step delay value, representing the number of additional PTG clocks, between the start of a Step command and the completion of a Step command.

- **Note 1:** A base step delay of one PTG clock is added to any value written to the PTGSDLIM register (Step Delay = (PTGSDLIM) + 1).
  - 2: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

## REGISTER 25-7: PTGC0LIM: PTG COUNTER 0 LIMIT REGISTER<sup>(1)</sup>

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC0	_IM<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PTGC0	LIM<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit	t	W = Writable bit		U = Unimpler	nented bit, read	l as '0'	

bit 15-0 **PTGC0LIM<15:0>:** PTG Counter 0 Limit Register bits

'1' = Bit is set

May be used to specify the loop count for the PTGJMPC0 Step command or as a limit register for the General Purpose Counter 0.

'0' = Bit is cleared

-n = Value at POR

x = Bit is unknown

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

# 28.0 PARALLEL MASTER PORT (PMP)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33/PIC24 Family Reference Manual", "Parallel Master Port (PMP)" (DS70576), which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Parallel Master Port (PMP) module is a parallel 8-bit I/O module, specifically designed to communicate with a wide variety of parallel devices, such as communication peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP is highly configurable.

Key features of the PMP module include:

- Eight Data Lines
- Up to 16 Programmable Address Lines
- · Up to 2 Chip Select Lines
- Programmable Strobe Options:
  - Individual read and write strobes, or
  - Read/Write strobe with enable strobe
- Address Auto-Increment/Auto-Decrement
- Programmable Address/Data Multiplexing
- Programmable Polarity on Control Signals
- · Legacy Parallel Slave Port (PSP) Support
- Enhanced Parallel Slave Support:
  - Address support
  - 4-byte deep auto-incrementing buffer
- Programmable Wait States

### FIGURE 28-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	С
26	DEC	DEC	f	f = f - 1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f - 2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws – 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None
29	DIV	DIV.S	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
30	DIVF	DIVF	Wm,Wn	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
31	DO	DO	#lit15,Expr	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO	Wn,Expr	Do code to PC + Expr, (Wn) + 1 times	2	2	None
32	ED	ED	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
33	EDAC	EDAC	Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
34	EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
35	FBCL	FBCL	Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	С
36	FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	С
37	FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	С
38	GOTO	GOTO	Expr	Go to address	2	4	None
		GOTO	Wn	Go to indirect	1	4	None
		GOTO.L	Wn	Go to indirect (long address)	1	4	None
39	INC	INC	f	f = f + 1	1	1	C,DC,N,OV,Z
		INC	f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC	Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
40	INC2	INC2	f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2	f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2	Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
41	IOR	IOR	f	f = f .IOR. WREG	1	1	N,Z
		IOR	f,WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
42	LAC	LAC	Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
43	LNK	LNK	#lit14	Link Frame Pointer	1	1	SFA
44	LSR	LSR	f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
45	MAC	MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm*Wm, Acc, Wx, Wxd, Wy, Wyd	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB

## TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

## TABLE 33-61: DMA MODULE TIMING REQUIREMENTS

AC CH	ARACTERISTICS	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param No.	Characteristic	Min.	Тур. <sup>(1)</sup>	Max.	Units	Conditions	
DM1	DMA Byte/Word Transfer Latency	1 Tcy <b>(2)</b>			ns		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.

## 100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

Mold Draft Angle Bottom

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

β

11°

12°

- 4. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B

13°

# **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Microchip Trade Architecture — Core Family — Program Memo Product Group Pin Count — Tape and Reel F Temperature Ra Package — Pattern —	dsPIC 33 EP 512 GM7 10 T - I / PT XXX emark	Example: dsPIC33EP512GM710-I/PT: dsPIC33, Enhanced Performance, 512-Kbyte program memory, 100-pin, Industrial temperature, TQFP package.
Architecture:	33 = 16-Bit Digital Signal Controller	
Family:	EP = Enhanced Performance	
Product Group:	GM7 = General Purpose plus Motor Control Family	
Pin Count:	04 = 44-pin 06 = 64-pin 10 = 100/124-pin	
Temperature Range:	$ \begin{array}{rcl} & = & -40^{\circ}\text{C to } +85^{\circ}\text{C (Industrial)} \\ \text{E} & = & -40^{\circ}\text{C to } +125^{\circ}\text{C (Extended)} \end{array} $	
Package:	BG= Plastic Thin Profile Ball Grid Array - (121-pin) 10x10 mm body (TFBGA)ML= Plastic Quad, No Lead Package - (44-pin) 8x8 mm body (QFN)MR= Plastic Quad, No Lead Package - (64-pin) 9x9 mm body (QFN)PT= Plastic Thin Quad Flatpack - (44-pin) 10x10 mm body (TQFP)PT= Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP)PT= Thin Quad Flatpack - (100-pin) 12x12x1 mm body (TQFP)PF= Thin Quad Flatpack - (100-pin) 14x14x1 mm body (TQFP)	