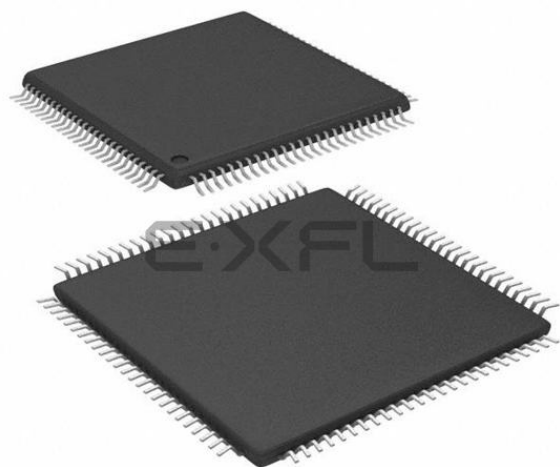




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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gm710t-i-pt

dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 2: PIN NAMES: dsPIC33EP128/256/512GM310/710 DEVICES^(1,2,3) (CONTINUED)

Pin #	Full Pin Name	Pin #	Full Pin Name
E1	PWM6H/T8CK/RD4	J8	No Connect
E2	PWM6L/T9CK/RD3	J9	No Connect
E3	AN19/RP118/PMA5/RG6	J10	AN41/RP81/RE1
E4	PWM5H/RD2	J11	AN30/SDA1/RPI52/RC4
E5	No Connect	K1	PGED3/OA2IN-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
E6	RP113/RG1	K2	PGEC3/CVREF+/OA1OUT/AN3/C1IN4-/C4IN2-/RPI33/CTED1/RB1
E7	No Connect	K3	VREF+/AN34/PMA7/RF10
K4	OA3OUT/AN6/C3IN4-/C4IN4-/C4IN1+/RP48/OCFB/RC0	L3	AVss
K5	No Connect	L4	OA3IN-/AN7/C3IN1-/C4IN1-/RP49/RC1
K6	AN37/RF12	L5	OA3IN+/AN8/C3IN3-/C3IN1+/RPI50/U1RTS/BCLK1/FLT3/PMA13/RC2
K7	AN14/RPI94/FLT7/PMA1/RE14	L6	AN36/RF13
K8	VDD	L7	AN13/C3IN2-/U2CTS/FLT6/PMA10/RE13
K9	AN39/RD15	L8	AN15/RPI95/FLT8/PMA0/RE15
K10	OA5IN+/AN24/C5IN3-/C5IN1+/SDO1/RP20/T1CK/RA4	L9	AN38/RD14
K11	AN40/RPI80/RE0	L10	SDA2/RPI24/PMA9/RA8
L1	PGEC1/OA1IN+/AN4/C1IN3-/C1IN1+/C2IN3-/RPI34/RB2	L11	FLT32/SCL2/RP36/PMA8/RB4
L2	VREF-/AN33/PMA6/RF9		

Note 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.

2: Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.

3: The availability of I²C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5.4>). See **Section 30.0 “Special Features”** for more information.

TABLE 4-6: OUTPUT COMPARE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0900	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC1RS	0904	Output Compare 1 Secondary Register																xxxx
OC1R	0906	Output Compare 1 Register																xxxx
OC1TMR	0908	Output Compare 1 Timer Value Register																xxxx
OC2CON1	090A	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC2RS	090E	Output Compare 2 Secondary Register																xxxx
OC2R	0910	Output Compare 2 Register																xxxx
OC2TMR	0912	Output Compare 2 Timer Value Register																xxxx
OC3CON1	0914	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC3RS	0918	Output Compare 3 Secondary Register																xxxx
OC3R	091A	Output Compare 3 Register																xxxx
OC3TMR	091C	Output Compare 3 Timer Value Register																xxxx
OC4CON1	091E	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC4RS	0922	Output Compare 4 Secondary Register																xxxx
OC4R	0924	Output Compare 4 Register																xxxx
OC4TMR	0926	Output Compare 4 Timer Value Register																xxxx
OC5CON1	0928	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC5CON2	092A	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC5RS	092C	Output Compare 5 Secondary Register																xxxx
OC5R	092E	Output Compare 5 Register																xxxx
OC5TMR	0930	Output Compare 5 Timer Value Register																xxxx
OC6CON1	0932	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	ENFLTB	ENFLTA	—	OCFLTB	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC6CON2	0934	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC6RS	0936	Output Compare 6 Secondary Register																xxxx
OC6R	0938	Output Compare 6 Register																xxxx
OC6TMR	093A	Output Compare 6 Timer Value Register																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-25: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES⁽¹⁾

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400-041E	See definition when WIN = x																
C1BUFPNT1	0420	F3BP3	F3BP2	F3BP1	F3BP0	F2BP3	F2BP2	F2BP1	F2BP0	F1BP3	F1BP2	F1BP1	F1BP0	F0BP3	F0BP2	F0BP1	F0BP0	0000
C1BUFPNT2	0422	F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0	F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0	0000
C1BUFPNT3	0424	F11BP3	F11BP2	F11BP1	F11BP0	F10BP3	F10BP2	F10BP1	F10BP0	F9BP3	F9BP2	F9BP1	F9BP0	F8BP3	F8BP2	F8BP1	F8BP0	0000
C1BUFPNT4	0426	F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0	F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0	0000
C1RXM0SID	0430	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C1RXM0EID	0432	EID<15:0>																xxxx
C1RXM1SID	0434	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C1RXM1EID	0436	EID<15:0>																xxxx
C1RXM2SID	0438	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C1RXM2EID	043A	EID<15:0>																xxxx
C1RXF0SID	0440	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF0EID	0442	EID<15:0>																xxxx
C1RXF1SID	0444	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF1EID	0446	EID<15:0>																xxxx
C1RXF2SID	0448	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF2EID	044A	EID<15:0>																xxxx
C1RXF3SID	044C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF3EID	044E	EID<15:0>																xxxx
C1RXF4SID	0450	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF4EID	0452	EID<15:0>																xxxx
C1RXF5SID	0454	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF5EID	0456	EID<15:0>																xxxx
C1RXF6SID	0458	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF6EID	045A	EID<15:0>																xxxx
C1RXF7SID	045C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF7EID	045E	EID<15:0>																xxxx
C1RXF8SID	0460	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF8EID	0462	EID<15:0>																xxxx
C1RXF9SID	0464	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF9EID	0466	EID<15:0>																xxxx
C1RXF10SID	0468	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF10EID	046A	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

TABLE 4-46: PORTA REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	TRISA<15:14>		—	TRISA<12:7>						—	—	TRISA4	—	—	TRISA<1:0>		DF9F
PORTA	0E02	RA<15:14>		—	RA<12:7>						—	—	RA4	—	—	RA<1:0>		0000
LATA	0E04	LATA<15:14>		—	LATA<12:7>						—	—	LATA4	—	—	LATA<1:0>		0000
ODCA	0E06	ODCA<15:14>		—	ODCA<12:7>						—	—	ODCA4	—	—	ODCA<1:0>		0000
CNENA	0E08	CNIEA<15:14>		—	CNIEA<12:7>						—	—	CNIEA4	—	—	CNIEA<1:0>		0000
CNPUA	0E0A	CNPUA<15:14>		—	CNPUA<12:7>						—	—	CNPUA4	—	—	CNPUA<1:0>		0000
CNPDA	0E0C	CNPDA<15:14>		—	CNPDA<12:7>						—	—	CNPDA4	—	—	CNPDA<1:0>		0000
ANSELA	0E0E	ANSA<15:14>		—	ANSA<12:11>		—	ANSA9	—	—	—	—	ANSA4	—	—	ANSA<1:0>		1813

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-47: PORTA REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	TRISA<12:7>						—	—	TRISA4	—	—	TRISA<1:0>		DF9F
PORTA	0E02	—	—	—	RA<12:7>						—	—	RA4	—	—	RA<1:0>		0000
LATA	0E04	—	—	—	LATA<12:7>						—	—	LATA4	—	—	LATA<1:0>		0000
ODCA	0E06	—	—	—	ODCA<12:7>						—	—	ODCA4	—	—	ODCA<1:0>		0000
CNENA	0E08	—	—	—	CNIEA<12:7>						—	—	CNIEA4	—	—	CNIEA<1:0>		0000
CNPUA	0E0A	—	—	—	CNPUA<12:7>						—	—	CNPUA4	—	—	CNPUA<1:0>		0000
CNPDA	0E0C	—	—	—	CNPDA<12:7>						—	—	CNPDA4	—	—	CNPDA<1:0>		0000
ANSELA	0E0E	—	—	—	ANSA<12:11>		—	ANSA9	—	—	—	—	ANSA4	—	—	ANSA<1:0>		1813

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-48: PORTA REGISTER MAP FOR dsPIC33EPXXXGM304/604 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	TRISA<10:7>				—	—	TRISA<4:0>					DF9F
PORTA	0E02	—	—	—	—	—	RA<10:7>				—	—	RA<4:0>					0000
LATA	0E04	—	—	—	—	—	LATA<10:7>				—	—	LATA<4:0>					0000
ODCA	0E06	—	—	—	—	—	ODCA<10:7>				—	—	ODCA<4:0>					0000
CNENA	0E08	—	—	—	—	—	CNIEA<10:7>				—	—	CNIEA<4:0>					0000
CNPUA	0E0A	—	—	—	—	—	CNPUA<10:7>				—	—	CNPUA<4:0>					0000
CNPDA	0E0C	—	—	—	—	—	CNPDA<10:7>				—	—	CNPDA<4:0>					0000
ANSELA	0E0E	—	—	—	—	—	—	ANSA9	—	—	—	—	ANSA4	—	ANSA<2:0>			1813

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 8-3: DMAxSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<23:16>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **STA<23:16>:** DMA Primary Start Address bits (source or destination)

REGISTER 8-4: DMAxSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **STA<15:0>:** DMA Primary Start Address bits (source or destination)

10.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Watchdog Timer and Power-Saving Modes” (DS70615), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

The dsPIC33EPXXXGM3XX/6XX/7XX devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV #SLEEP_MODE    ; Put the device into Sleep mode
PWRSAV #IDLE_MODE     ; Put the device into Idle mode
```

10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGM3XX/6XX/7XX devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 “Oscillator Configuration”**.

10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGM3XX/6XX/7XX devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the Assembler Include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to “wake-up”.

TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name ⁽¹⁾	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<6:0>
External Interrupt 2	INT2	RPINR1	INT2R<6:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<6:0>
Input Capture 1	IC1	RPINR7	IC1R<6:0>
Input Capture 2	IC2	RPINR7	IC2R<6:0>
Input Capture 3	IC3	RPINR8	IC3R<6:0>
Input Capture 4	IC4	RPINR8	IC4R<6:0>
Input Capture 5	IC5	RPINR9	IC5R<6:0>
Input Capture 6	IC6	RPINR9	IC6R<6:0>
Input Capture 7	IC7	RPINR10	IC7R<6:0>
Input Capture 8	IC8	RPINR10	IC8R<6:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<6:0>
PWM Fault 1	FLT1	RPINR12	FLT1R<6:0>
PWM Fault 2	FLT2	RPINR12	FLT2R<6:0>
QE1 Phase A	QEA1	RPINR14	QEA1R<6:0>
QE1 Phase B	QEB1	RPINR14	QEB1R<6:0>
QE1 Index	INDX1	RPINR 15	INDX1R<6:0>
QE1 Home	HOME1	RPINR15	HOM1R<6:0>
QE2 Phase A	QEA2	RPINR16	QEA2R<6:0>
QE2 Phase B	QEB2	RPINR16	QEB2R<6:0>
QE2 Index	INDX2	RPINR17	INDX2R<6:0>
QE2 Home	HOME2	RPINR17	HOM2R<6:0>
UART1 Receive	U1RX	RPINR18	U1RXR<6:0>
UART2 Receive	U2RX	RPINR19	U2RXR<6:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<6:0>
SPI2 Clock Input	SCK2	RPINR22	SCK2R<6:0>
SPI2 Slave Select	$\overline{SS2}$	RPINR23	SS2R<6:0>
DCI Data Input	CSDI	RPINR24	CSDIR<6:0>
DCI Clock Input	CCLK	RPINR24	CCLKR<6:0>
DCI Frame Synchronization Input	COFS	RPINR25	COFSR<6:0>
CAN1 Receive ⁽²⁾	C1RX	RPINR26	C1RXR<6:0>
CAN2 Receive ⁽²⁾	C2RX	RPINR26	C2RXR<6:0>
UART3 Receive	U3RX	RPINR27	U3RXR<6:0>
UART3 Clear-to-Send	$\overline{U3CTS}$	RPINR27	U3CTSR<6:0>
UART4 Receive	U4RX	RPINR28	U4RXR<6:0>
UART4 Clear-to-Send	$\overline{U4CTS}$	RPINR28	U4CTSR<6:0>
SPI3 Data Input	SDI3	RPINR29	SDI3R<6:0>
SPI3 Clock Input	SCK3	RPINR29	SCK3R<6:0>
SPI3 Slave Select	$\overline{SS3}$	RPINR 30	SS3R<6:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input is available on dsPIC33EPXXXGM6XX/7XX devices only.

REGISTER 11-16: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SCK2R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SDI2R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **SCK2R<6:0>:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•

•

•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **SDI2R<6:0>:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

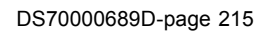
•

•

•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss



REGISTER 17-1: QEIXCON: QEIX CONTROL REGISTER (CONTINUED)

- bit 6-4 **INTDIV<2:0>**: Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select)⁽³⁾
- 111 = 1:128 prescale value
 - 110 = 1:64 prescale value
 - 101 = 1:32 prescale value
 - 100 = 1:16 prescale value
 - 011 = 1:8 prescale value
 - 010 = 1:4 prescale value
 - 001 = 1:2 prescale value
 - 000 = 1:1 prescale value
- bit 3 **CNTPOL**: Position and Index Counter/Timer Direction Select bit
- 1 = Counter direction is negative unless modified by external up/down signal
 - 0 = Counter direction is positive unless modified by external up/down signal
- bit 2 **GATEN**: External Count Gate Enable bit
- 1 = External gate signal controls position counter operation
 - 0 = External gate signal does not affect position counter/timer operation
- bit 1-0 **CCM<1:0>**: Counter Control Mode Selection bits
- 11 = Internal Timer mode with optional external count is selected
 - 10 = External clock count with optional external count is selected
 - 01 = External clock count with external up/down direction is selected
 - 00 = Quadrature Encoder Interface (x4 mode) Count mode is selected

- Note 1:** When CCM<1:0> = 10 or CCM<1:0> = 11, all of the QEI counters operate as timers and the PIMOD<2:0> bits are ignored.
- 2:** When CCM<1:0> = 00, and QEAX and QEBx values match the Index Match Value (IMV), the POSCNTNTH and POSCNTL registers are reset.
- 3:** The selected clock rate should be at least twice the expected maximum quadrature count rate.
- 4:** The match value applies to the A and B inputs after the swap and polarity bits have been applied.

18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
 - a) If FRMPOL (SPIxCON2<13>) = 1, use a pull-down resistor on $\overline{SSx}$.
 - b) If FRMPOL = 0, use a pull-up resistor on $\overline{SSx}$.

Note: This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode (i.e., not using $\overline{SSx}$ from a master):
 - a) If CKP (SPIxCON1<6>) = 1, always place a pull-up resistor on $\overline{SSx}$.
 - b) If CKP = 0, always place a pull-down resistor on $\overline{SSx}$.

Note: This will insure that during power-up and initialization, the master/slave will not lose sync due to an errant SCK transition that would cause the slave to accumulate data shift errors, for both transmit and receive, appearing as corrupted data.

3. FRMEN (SPIxCON2<15>) = 1 and SSEN (SPIxCON1<7>) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the $\overline{SSx}$ pin, which indicates the start of a data frame.

Note: Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in **Section 33.0 “Electrical Characteristics”** for details.

4. In Master mode only, set the SMP bit (SPIxCON1<9>) to a '1' for the fastest SPI data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1<5>) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

REGISTER 21-13: CxBUFNT2: CANx FILTERS 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-12 **F7BP<3:0>**: RX Buffer Mask for Filter 7 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
.
.
.
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0
- bit 11-8 **F6BP<3:0>**: RX Buffer Mask for Filter 6 bits (same values as bits 15-12)
- bit 7-4 **F5BP<3:0>**: RX Buffer Mask for Filter 5 bits (same values as bits 15-12)
- bit 3-0 **F4BP<3:0>**: RX Buffer Mask for Filter 4 bits (same values as bits 15-12)

REGISTER 21-14: CxBUFNT3: CANx FILTERS 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP3	F11BP2	F11BP1	F11BP0	F10BP3	F10BP2	F10BP1	F10BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP3	F9BP2	F9BP1	F9BP0	F8BP3	F8BP2	F8BP1	F8BP0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-12 **F11BP<3:0>**: RX Buffer Mask for Filter 11 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
.
.
.
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0
- bit 11-8 **F10BP<3:0>**: RX Buffer Mask for Filter 10 bits (same values as bits 15-12)
- bit 7-4 **F9BP<3:0>**: RX Buffer Mask for Filter 9 bits (same values as bits 15-12)
- bit 3-0 **F8BP<3:0>**: RX Buffer Mask for Filter 8 bits (same values as bits 15-12)

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 21-18: CxFMSKSEL1: CANx FILTERS 7-0 MASK SELECTION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSK1	F7MSK0	F6MSK1	F6MSK0	F5MSK1	F5MSK0	F4MSK1	F4MSK0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3MSK1	F3MSK0	F2MSK1	F2MSK0	F1MSK1	F1MSK0	F0MSK1	F0MSK0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **F7MSK<1:0>**: Mask Source for Filter 7 bit

11 = Reserved

10 = Acceptance Mask 2 registers contain mask

01 = Acceptance Mask 1 registers contain mask

00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F6MSK<1:0>**: Mask Source for Filter 6 bit (same values as bits 15-14)

bit 11-10 **F5MSK<1:0>**: Mask Source for Filter 5 bit (same values as bits 15-14)

bit 9-8 **F4MSK<1:0>**: Mask Source for Filter 4 bit (same values as bits 15-14)

bit 7-6 **F3MSK<1:0>**: Mask Source for Filter 3 bit (same values as bits 15-14)

bit 5-4 **F2MSK<1:0>**: Mask Source for Filter 2 bit (same values as bits 15-14)

bit 3-2 **F1MSK<1:0>**: Mask Source for Filter 1 bit (same values as bits 15-14)

bit 1-0 **F0MSK<1:0>**: Mask Source for Filter 0 bit (same values as bits 15-14)

TABLE 25-2: PTG OUTPUT DESCRIPTIONS

PTG Output Number	PTG Output Description
PTGO0	Trigger/Synchronization Source for OC1
PTGO1	Trigger/Synchronization Source for OC2
PTGO2	Trigger/Synchronization Source for OC3
PTGO3	Trigger/Synchronization Source for OC4
PTGO4	Clock Source for OC1
PTGO5	Clock Source for OC2
PTGO6	Clock Source for OC3
PTGO7	Clock Source for OC4
PTGO8	Trigger/Synchronization Source for IC1
PTGO9	Trigger/Synchronization Source for IC2
PTGO10	Trigger/Synchronization Source for IC3
PTGO11	Trigger/Synchronization Source for IC4
PTGO12	Sample Trigger for ADC
PTGO13	Sample Trigger for ADC
PTGO14	Sample Trigger for ADC
PTGO15	Sample Trigger for ADC
PTGO16	PWM Time Base Synchronous Source for PWM
PTGO17	PWM Time Base Synchronous Source for PWM
PTGO18	Mask Input Select for Op Amp/Comparator
PTGO19	Mask Input Select for Op Amp/Comparator
PTGO20	Reserved
PTGO21	Reserved
PTGO22	Reserved
PTGO23	Reserved
PTGO24	Reserved
PTGO25	Reserved
PTGO26	Reserved
PTGO27	Reserved
PTGO28	Reserved
PTGO29	Reserved
PTGO30	PTG Output to PPS Input Selection
PTGO31	PTG Output to PPS Input Selection

FIGURE 33-7: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS

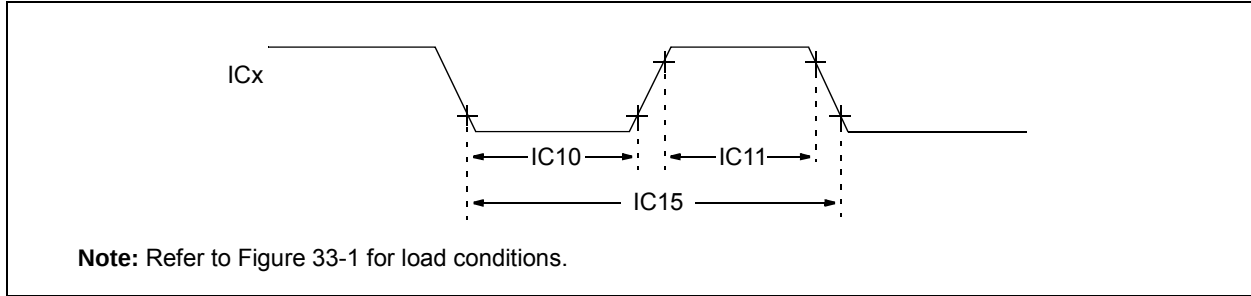


TABLE 33-25: INPUT CAPTURE x (ICx) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Max.	Units	Conditions	
IC10	TccL	ICx Input Low Time	Greater of: 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15	N = Prescale value (1, 4, 16)
IC11	TccH	ICx Input High Time	Greater of: 12.5 + 25 or (0.5 Tcy/N) + 25	—	ns	Must also meet Parameter IC15	
IC15	TccP	ICx Input Period	Greater of: 25 + 50 or (1 Tcy/N) + 50	—	ns		

Note 1: These parameters are characterized, but not tested in manufacturing.

dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 33-8: OUTPUT COMPARE x (OCx) TIMING CHARACTERISTICS

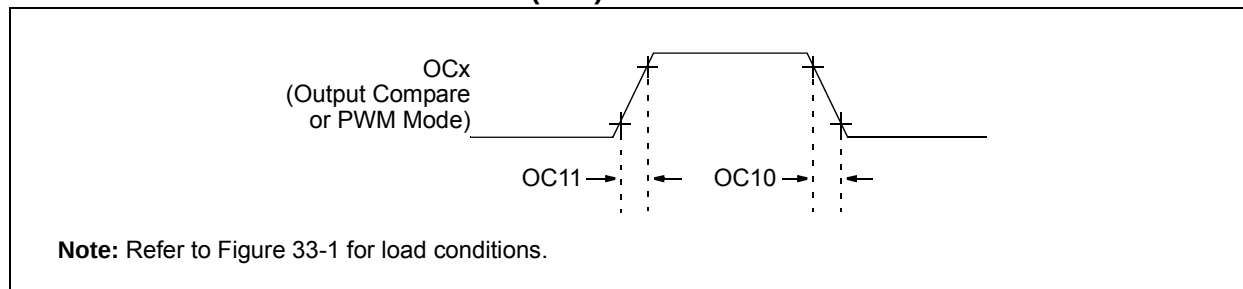


TABLE 33-26: OUTPUT COMPARE x (OCx) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 33-9: OCx/PWMx MODULE TIMING CHARACTERISTICS

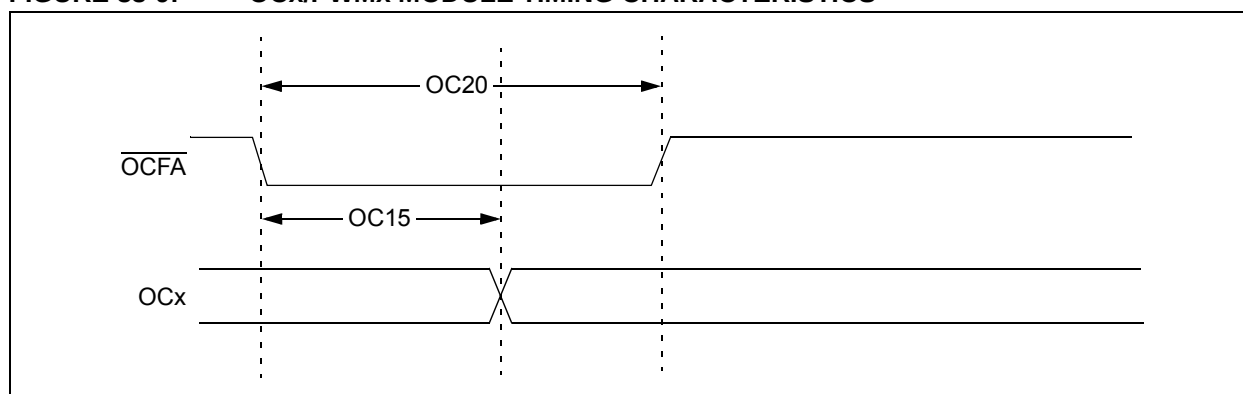


TABLE 33-27: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC15	TfD	Fault Input to PWMx I/O Change	—	—	Tcy + 20	ns	
OC20	TfLT	Fault Input Pulse Width	Tcy + 20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 33-24: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS

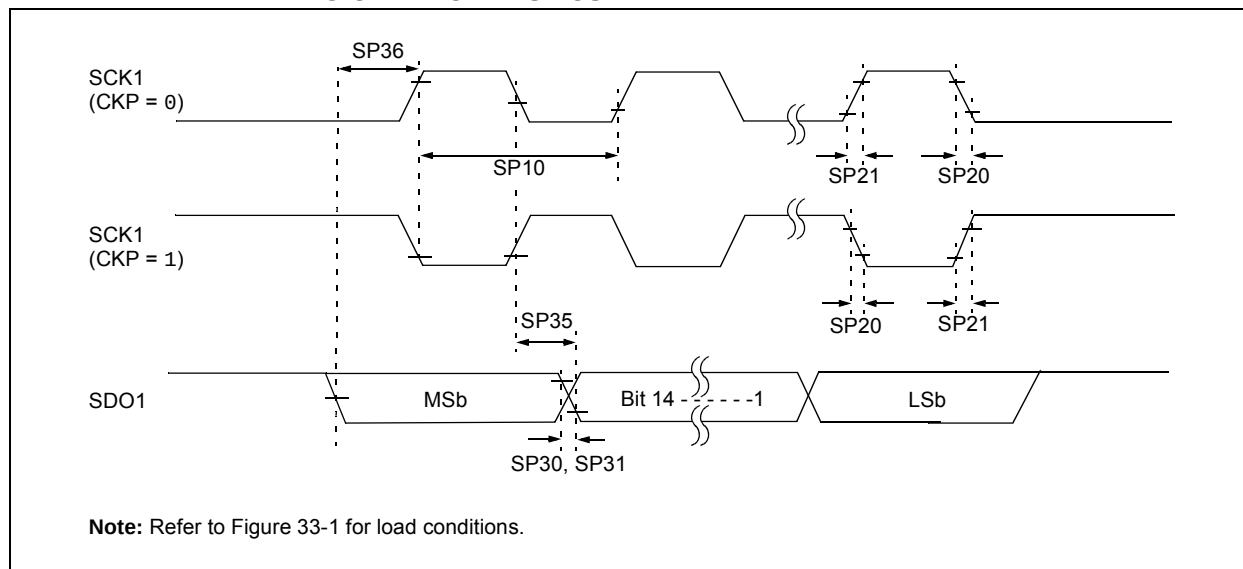
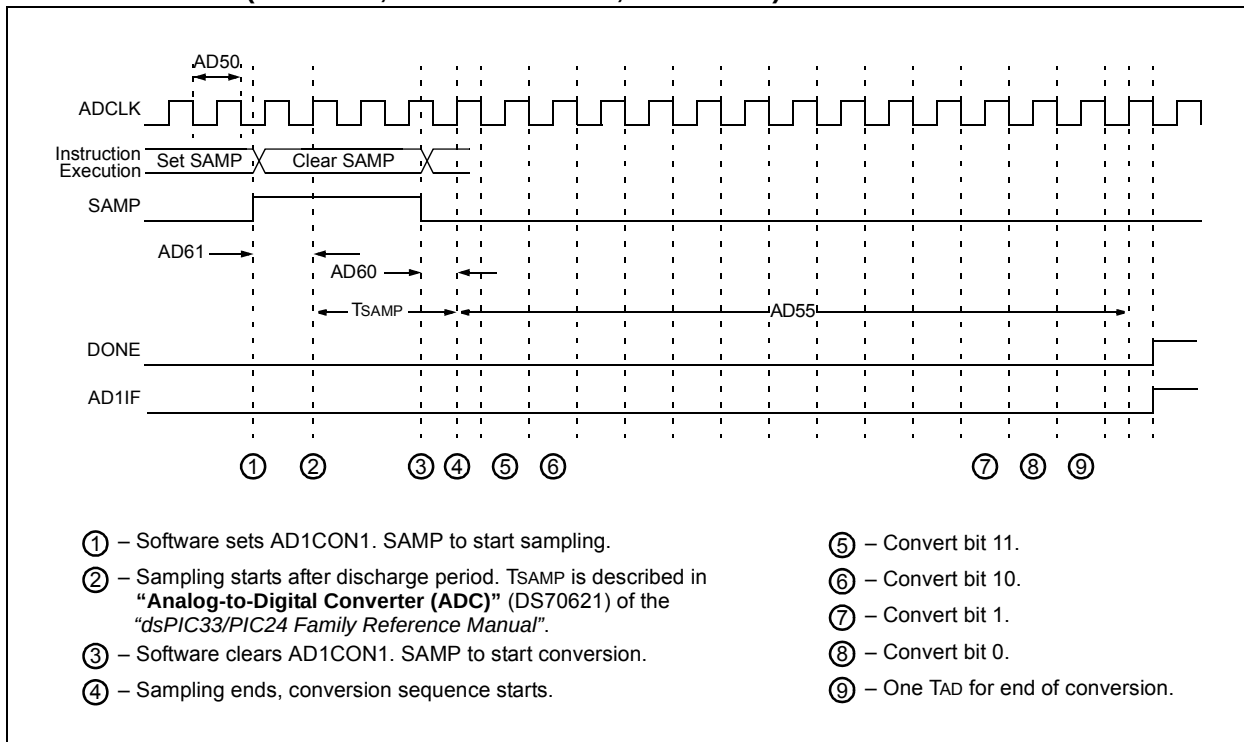


TABLE 33-41: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	(Note 3)
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	

- Note 1:** These parameters are characterized, but are not tested in manufacturing.
- Note 2:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
- Note 3:** The minimum clock period for SCK1 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.
- Note 4:** Assumes 50 pF load on all SPI1 pins.

FIGURE 33-38: ADC1 CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS
(ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)



F

Flash Program Memory	103
Control Registers	104
Operations	104
RTSP Operation.....	104
Table Instructions.....	103
Flexible Configuration	411

G

Getting Started with 16-Bit DSCs	21
Connection Requirements	21
CPU Logic Filter Capacitor Connection (VCAP)	22
Decoupling Capacitors	21
External Oscillator Pins	23
ICSP Pins.....	23
Master Clear (MCLR) Pin.....	22
Oscillator Value Conditions on Device Start-up	24
Unused I/Os	24

H

High-Speed PWM	229
Control Registers	233
Faults	229
High-Temperature Electrical Characteristics.....	499
Absolute Maximum Ratings	499
High-Voltage Detect (HVD).....	173

I

I/O Ports	163
Configuring Analog/Digital Port Pins.....	164
Helpful Tips.....	173
Open-Drain Configuration	164
Parallel I/O (PIO).....	163
Write/Read Timing	164
In-Circuit Debugger.....	418
In-Circuit Emulation.....	411
In-Circuit Serial Programming (ICSP)	411, 418
Input Capture	219
Control Registers	220
Input Change Notification (ICN)	164
Instruction Addressing Modes.....	96
File Register Instructions	96
Fundamental Modes Supported.....	97
MAC Instructions.....	97
MCU Instructions	96
Move and Accumulator Instructions	97
Other Instructions.....	97
Instruction Set	
Overview	422
Summary.....	419
Interfacing Program and Data Memory Spaces	101
Inter-Integrated Circuit (I ² C).....	281
Control Registers	283
Internal LPRC Oscillator	
Use with WDT	417
Internet Address.....	536
Interrupt Controller	
Control and Status Registers	120
IECx	120
IFSx	120
INTCON1	120
INTCON2	120
INTCON3	120
INTCON4	120
INTTREG	120
IPCx	120

Reset Sequence	115
Interrupt Vector	
Details (table)	117
Interrupt Vector Table (IVT)	115
Interrupt Vector Table (table).....	116

J

JTAG Boundary Scan Interface	411
JTAG Interface	418

M

Memory Maps	
EDS	94
Memory Organization	37
Microchip Internet Web Site.....	536
Modulo Addressing	98
Applicability.....	99
Operation Example	98
Start and End Address	98
W Address Register Selection.....	98
MPLAB Assembler, Linker, Librarian.....	430
MPLAB ICD 3 In-Circuit Debugger	431
MPLAB PM3 Device Programmer	431
MPLAB REAL ICE In-Circuit Emulator System	431
MPLAB X Integrated Development	
Environment Software	429
MPLAB X SIM Software Simulator	431
MPLIB Object Librarian.....	430
MPLINK Object Linker	430

O

Op Amp	
Application Considerations	368
Configuration A.....	368
Configuration B.....	369
Op Amp/Comparator.....	365
Control Registers.....	370
Resources	369
Oscillator Configuration	143
CPU Clocking System	144
Output Compare	223
Control Registers.....	224

P

Packaging	507
Details.....	517, 518
Marking.....	507, 508
Parallel Master Port (PMP).....	395
Peripheral Module Disable (PMD)	155
Peripheral Pin Select (PPS).....	165
Input Sources, Maps Input to Function	167
Output Selection for Remappable Pins	172
Peripheral Trigger Generator (PTG) Module	349
PICkit 3 In-Circuit Debugger/Programmer	431
Pinout I/O Descriptions (table).....	16
PMP	
Control Registers.....	396
Power-Saving Features	153
Clock Frequency and Switching	153
Instruction-Based Modes	153
Idle.....	154
Sleep	154
Interrupts Coincident with Power Save	
Instructions	154
PPS	
Control Registers.....	175

AUXCONx (PWMx Auxiliary Control).....	254	DEVREV (Device Revision).....	415
CHOP (PWMx Chop Clock Generator).....	241	DMALCA (DMA Last Channel Active Status).....	140
CLKDIV (Clock Divisor).....	148	DMA PPS (DMA Ping-Pong Status).....	141
CM4CON (Op Amp/Comparator 4 Control).....	373	DMA PWC (DMA Peripheral Write Collision Status).....	138
CMSTAT (Op Amp/Comparator Status).....	370	DMA RQC (DMA Request Collision Status).....	139
CMxCON (Op Amp/Comparator x Control, x = 1, 2, 3 or 5).....	371	DMAxCNT (DMA Channel x Transfer Count).....	136
CMxFLTR (Comparator x Filter Control).....	379	DMAxCON (DMA Channel x Control).....	132
CMxMSKCON (Comparator x Mask Gating Control).....	377	DMAxPAD (DMA Channel x Peripheral Address).....	136
CMxMSKSR (Comparator x Mask Source Select Control).....	375	DMAxREQ (DMA Channel x IRQ Select).....	133
CORCON (Core Control).....	33, 122	DMAxSTAH (DMA Channel x Start Address A, High).....	134
CRCCON1 (CRC Control 1).....	407	DMAxSTAL (DMA Channel x Start Address A, Low).....	134
CRCCON2 (CRC Control 2).....	408	DMAxSTBH (DMA Channel x Start Address B, High).....	135
CRCXORH (CRC XOR Polynomial High).....	409	DMAxSTBL (DMA Channel x Start Address B, Low).....	135
CRCXORL (CRC XOR Polynomial Low).....	409	DSADRH (DMA Most Recent RAM High Address).....	137
CTMUCON1 (CTMU Control Register 1).....	323	DSADRL (DMA Most Recent RAM Low Address).....	137
CTMUCON2 (CTMU Control Register 2).....	324	DTRx (PWMx Dead-Time).....	246
CTMUICON (CTMU Current Control).....	326	FCLCONx (PWMx Fault Current-Limit Control).....	250
CVR1CON (Comparator Voltage Reference Control 1).....	380	I2CxCON (I2Cx Control).....	283
CVR2CON (Comparator Voltage Reference Control 2).....	381	I2CxMSK (I2Cx Slave Mode Address Mask).....	287
CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1).....	306	I2CxSTAT (I2Cx Status).....	285
CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2).....	307	ICxCON1 (Input Capture x Control 1).....	220
CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3).....	307	ICxCON2 (Input Capture x Control 2).....	221
CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4).....	308	INDxCNTH (Index Counter x High Word).....	267
CxCFG1 (CANx Baud Rate Configuration 1).....	304	INDxCNTL (Index Counter x Low Word).....	267
CxCFG2 (CANx Baud Rate Configuration 2).....	305	INDxHLD (Index Counter x Hold).....	268
CxCTRL1 (CANx Control 1).....	297	INTCON1 (Interrupt Control 1).....	123
CxCTRL2 (CANx Control 2).....	298	INTCON2 (Interrupt Control 2).....	125
CxEC (CANx Transmit/Receive Error Count).....	304	INTCON3 (Interrupt Control 3).....	126
CxFCTRL (CANx FIFO Control).....	300	INTCON4 (Interrupt Control 4).....	126
CxFEN1 (CANx Acceptance Filter Enable 1).....	306	INTTREG (Interrupt Control and Status).....	127
CxFIFO (CANx FIFO Status).....	301	INTxHLDH (Interval Timerx Hold High Word).....	272
CxFMSKSEL1 (CANx Filters 7-0 Mask Selection 1).....	310	INTxHLDL (Interval Timerx Hold Low Word).....	272
CxFMSKSEL2 (CANx Filters 15-8 Mask Selection 2).....	311	INTxTMRH (Interval Timerx High Word).....	271
CxINTE (CANx Interrupt Enable).....	303	INTxTMRL (Interval Timerx Low Word).....	271
CxINTF (CANx Interrupt Flag).....	302	IOCONx (PWMx I/O Control).....	248
CxRXFnEID (CANx Acceptance Filter n Extended Identifier).....	309	LEBCONx (Leading-Edge Blanking Control x).....	252
CxRXFnSID (CANx Acceptance Filter n Standard Identifier).....	309	LEBDLYx (Leading-Edge Blanking Delay x).....	253
CxRXFUL1 (CANx Receive Buffer Full 1).....	313	MDC (PWMx Master Duty Cycle).....	241
CxRXFUL2 (CANx Receive Buffer Full 2).....	313	NVMADR (Nonvolatile Memory Lower Address).....	107
CxRXMnEID (CANx Acceptance Filter Mask n Extended Identifier).....	312	NVMADRU (Nonvolatile Memory Upper Address).....	107
CxRXMnSID (CANx Acceptance Filter Mask n Standard Identifier).....	312	NVMCON (Nonvolatile Memory (NVM) Control).....	105
CxRXOVF1 (CANx Receive Buffer Overflow 1).....	314	NVMKEY (Nonvolatile Memory Key).....	108
CxRXOVF2 (CANx Receive Buffer Overflow 2).....	314	NVMSRCADRH (Nonvolatile Data Memory Upper Address).....	108
CxTRMnCON (CANx TX/RX Buffer mn Control).....	315	NVMSRCADRL (Nonvolatile Data Memory Lower Address).....	109
CxVEC (CANx Interrupt Code).....	299	OCxCON1 (Output Compare x Control 1).....	224
DCICON1 (DCI Control 1).....	344	OCxCON2 (Output Compare x Control 2).....	226
DCICON2 (DCI Control 2).....	345	OSCCON (Oscillator Control).....	146
DCICON3 (DCI Control 3).....	346	OSCTUN (FRC Oscillator Tuning).....	151
DCISTAT (DCI Status).....	347	PADCFG1 (Pad Configuration Control).....	387, 403
DEVID (Device ID).....	415	PDCx (PWMx Generator Duty Cycle).....	244
		PHASEx (PWMx Primary Phase-Shift).....	245
		PLLFB (PLL Feedback Divisor).....	150
		PMADDR (Parallel Master Port Address).....	400
		PMAEN (Parallel Master Port Address Enable).....	401