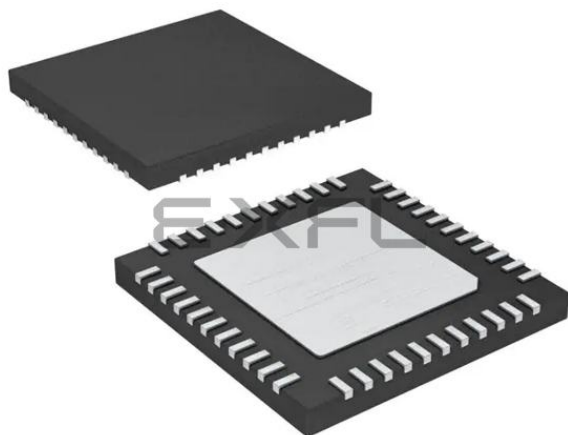




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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gm304t-i-ml

3.5 Programmer's Model

The programmer's model for the dsPIC33EPXXXGM3XX/6XX/7XX devices is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGM3XX/6XX/7XX devices contain control registers for Modulo

Addressing and Bit-Reversed Addressing, and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Table 4-1.

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15	Working Register Array
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine Status register
SPLIM	Stack Pointer Limit Value register
TBLPAG	Table Memory Page Address register
DSRPAG	Extended Data Space (EDS) Read Page register
DSWPAG	Extended Data Space (EDS) Write Page register
RCOUNT	REPEAT Loop Count register
DCOUNT	D0 Loop Count register
DOSTARTH ⁽¹⁾ , DOSTARTL ⁽¹⁾	D0 Loop Start Address register (High and Low)
DOENDH, DOENDL	D0 Loop End Address register (High and Low)
CORCON	Contains DSP Engine, D0 Loop Control and Trap Status bits

Note 1: The DOSTARTH and DOSTARTL registers are read-only.

dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 4-7: DATA MEMORY MAP FOR 512-KBYTE DEVICES

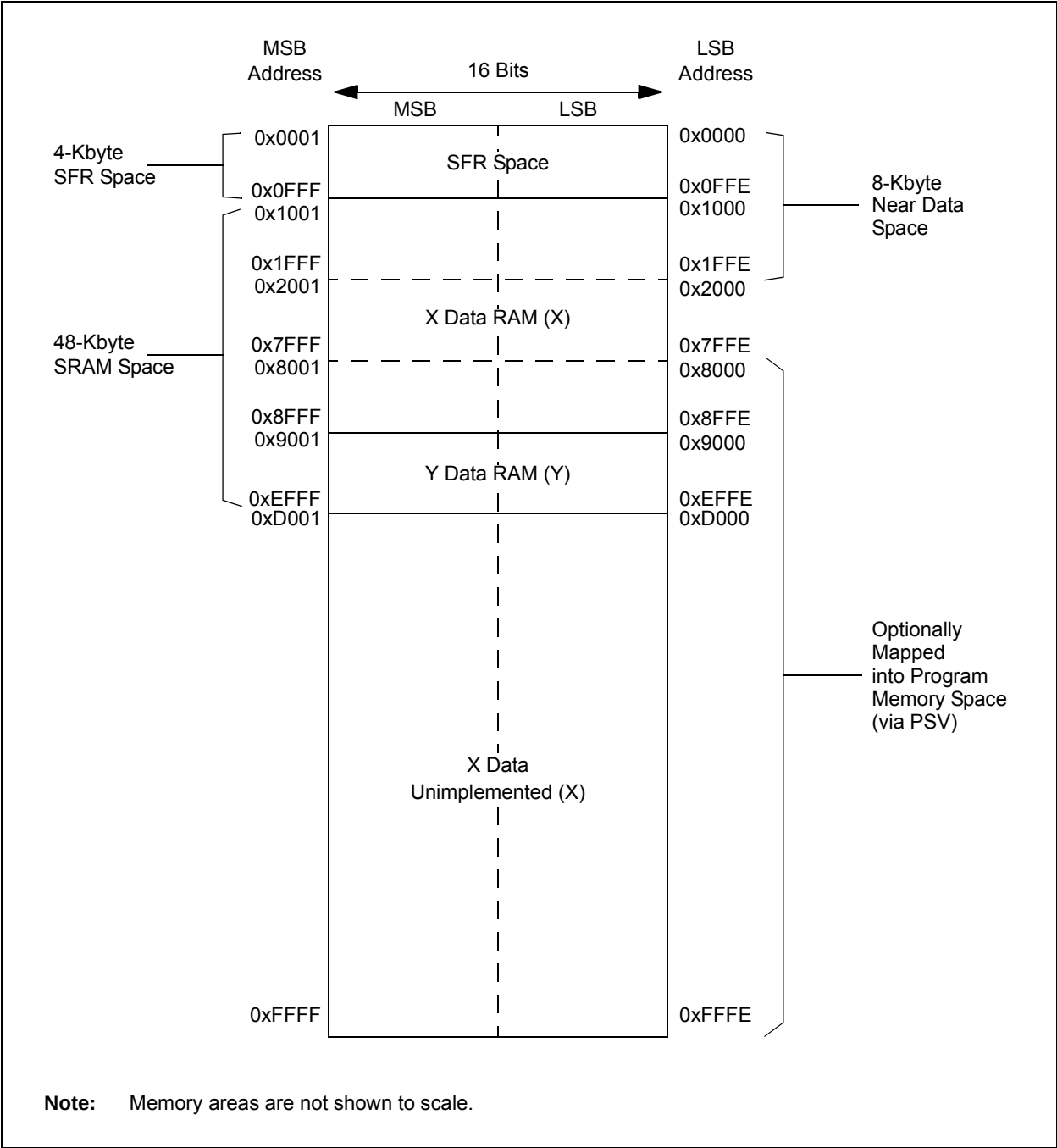


TABLE 4-28: CAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES⁽¹⁾

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0500-051E	See definition when WIN = x																
C2BUFNT1	0520	F3BP3	F3BP2	F3BP1	F3BP0	F2BP3	F2BP2	F2BP1	F2BP0	F1BP3	F1BP2	F1BP1	F1BP0	F0BP3	F0BP2	F0BP1	F0BP0	0000
C2BUFNT2	0522	F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0	F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0	0000
C2BUFNT3	0524	F11BP3	F11BP2	F11BP1	F11BP0	F10BP3	F10BP2	F10BP1	F10BP0	F9BP3	F9BP2	F9BP1	F9BP0	F8BP3	F8BP2	F8BP1	F8BP0	0000
C2BUFNT4	0526	F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0	F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0	0000
C2RXM0SID	0530	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXM0EID	0532	EID<15:0>																xxxx
C2RXM1SID	0534	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXM1EID	0536	EID<15:0>																xxxx
C2RXM2SID	0538	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXM2EID	053A	EID<15:0>																xxxx
C2RXF0SID	0540	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF0EID	0542	EID<15:0>																xxxx
C2RXF1SID	0544	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF1EID	0546	EID<15:0>																xxxx
C2RXF2SID	0548	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF2EID	054A	EID<15:0>																xxxx
C2RXF3SID	054C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF3EID	054E	EID<15:0>																xxxx
C2RXF4SID	0550	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF4EID	0552	EID<15:0>																xxxx
C2RXF5SID	0554	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF5EID	0556	EID<15:0>																xxxx
C2RXF6SID	0558	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF6EID	055A	EID<15:0>																xxxx
C2RXF7SID	055C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF7EID	055E	EID<15:0>																xxxx
C2RXF8SID	0560	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF8EID	0562	EID<15:0>																xxxx
C2RXF9SID	0564	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF9EID	0566	EID<15:0>																xxxx
C2RXF10SID	0568	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF10EID	056A	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

TABLE 4-34: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGM3XX DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets		
RPINR0	06A0	—	INT1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>								0000	
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>								0000	
RPINR7	06AE	—	IC2R<6:0>								—	IC1R<6:0>								0000
RPINR8	06B0	—	IC4R<6:0>								—	IC3R<6:0>								0000
RPINR9	06B2	—	IC6R<6:0>								—	IC5R<6:0>								0000
RPINR10	06B4	—	IC8R<6:0>								—	IC7R<6:0>								0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>								0000	
RPINR12	06B8	—	FLT2R<6:0>								—	FLT1R<6:0>								0000
RPINR14	06BC	—	QEB1R<6:0>								—	QEA1R<6:0>								0000
RPINR15	06BE	—	HOME1R<6:0>								—	INDX1R<6:0>								0000
RPINR16	06C0	—	QEB2R<6:0>								—	QEA2R<6:0>								0000
RPINR17	06C2	—	HOME2R<6:0>								—	INDX2R<6:0>								0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>								0000	
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>								0000	
RPINR22	06CC	—	SCK2R<6:0>								—	SDI2R<6:0>								0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>								0000	
RPINR24	06D0	—	CSCKR<6:0>								—	CSDIR<6:0>								0000
RPINR25	06D2	—	—	—	—	—	—	—	—	—	COFSR<6:0>								0000	
RPINR27	06D6	—	U3CTSR<6:0>								—	U3RXR<6:0>								0000
RPINR28	06D8	—	U4CTSR<6:0>								—	U4RXR<6:0>								0000
RPINR29	06DA	—	SCK3R<6:0>								—	SDI3R<6:0>								0000
RPINR30	06DC	—	—	—	—	—	—	—	—	—	SS3R<6:0>								0000	
RPINR37	06EA	—	SYNCI1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR38	06EC	—	DTCMP1R<6:0>								—	—	—	—	—	—	—	—	0000	
RPINR39	06EE	—	DTCMP3R<6:0>								—	DTCMP2R<6:0>								0000
RPINR40	06F0	—	DTCMP5R<6:0>								—	DTCMP4R<6:0>								0000
RPINR41	06F2	—	—	—	—	—	—	—	—	—	DTCMP6R<6:0>								0000	

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-58: PORTE REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	0E40	TRISE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	F000
PORTE	0E42	RE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	xxxx
LATE	0E44	LATE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	xxxx
ODCE	0E46	ODCE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENE	0E48	CNIEE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPUE	0E4A	CNPUE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPDE	0E4C	CNPDE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	0000
ANSELE	0E4E	ANSE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-59: PORTF REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	TRISF<13:12>		—	TRISF<10:9>		—	TRISF<7:4>				—	—	TRISF<1:0>		F303
PORTF	0E52	—	—	RF<13:12>		—	RF<10:9>		—	RF<7:4>				—	—	RF<1:0>		xxxx
LATF	0E54	—	—	LATF<13:12>		—	LATF<10:9>		—	LATF<7:4>				—	—	LATF<1:0>		xxxx
ODCF	0E56	—	—	ODCF<13:12>		—	ODCF<10:9>		—	ODCF<7:4>				—	—	ODCF<1:0>		0000
CNENF	0E58	—	—	CNIEF<13:12>		—	CNIEF<10:9>		—	CNIEF<7:4>				—	—	CNIEF<1:0>		0000
CNPUF	0E5A	—	—	CNPUF<13:12>		—	CNPUF<10:9>		—	CNPUF<7:4>				—	—	CNPUF<1:0>		0000
CNPDF	0E5C	—	—	CNPDF<13:12>		—	CNPDF<10:9>		—	CNPDF<7:4>				—	—	CNPDF<1:0>		0000
ANSELF	0E4E	—	—	ANSF<13:12>		—	ANSF<10:9>		—	—	—	ANSF<5:4>		—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-60: PORTF REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF<1:0>		0003
PORTF	0E52	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF<1:0>		xxxx
LATF	0E54	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF<1:0>		xxxx
ODCF	0E56	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF<1:0>		0000
CNENF	0E58	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF<1:0>		0000
CNPUF	0E5A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF<1:0>		0000
CNPDF	0E5C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN ⁽²⁾	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred
- bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or Uninitialized W Register Reset has not occurred
- bit 13-12 **Unimplemented:** Read as '0'
- bit 11 **VREGSF:** Flash Voltage Regulator Standby During Sleep bit
1 = Flash Voltage regulator is active during Sleep
0 = Flash Voltage regulator goes into Standby mode during Sleep
- bit 10 **Unimplemented:** Read as '0'
- bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred.
0 = A Configuration Mismatch Reset has NOT occurred
- bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep
- bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred
- bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed
- bit 5 **SWDTEN:** Software Enable/Disable of WDT bit⁽²⁾
1 = WDT is enabled
0 = WDT is disabled
- bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **IC8MD:IC1MD:** Input Capture x (x = 1-8) Module Disable bits

1 = Input Capture x module is disabled

0 = Input Capture x module is enabled

bit 7-0 **OC8MD:OC1MD:** Output Compare x (x = 1-8) Module Disable bits

1 = Output Compare x module is disabled

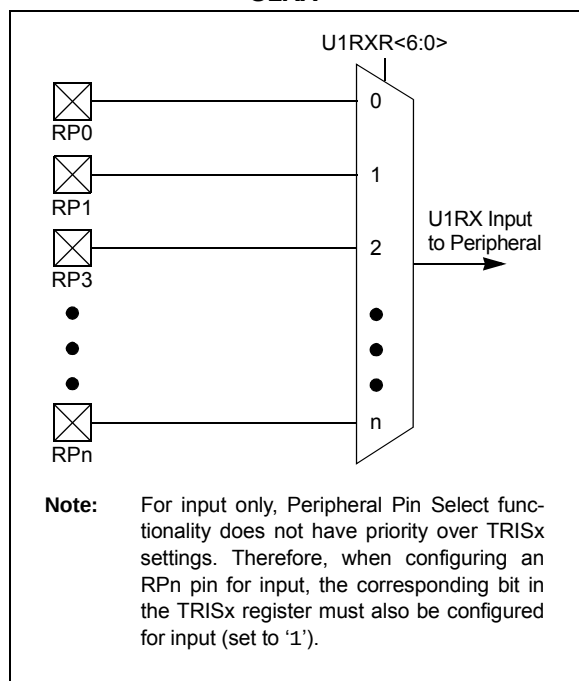
0 = Output Compare x module is enabled

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINR_x registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-29). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RP_n pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



11.4.4.1 Virtual Connections

dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 26-1 in **Section 26.0 “Op Amp/Comparator Module”**) and the PTG module (see **Section 25.0 “Peripheral Trigger Generator (PTG) Module”**).

In addition, dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual connections to the filtered QE_Ix module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 “Quadrature Encoder Interface (QE_I) Module”**).

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of 'b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QE_Ix module allows peripherals to be connected to the QE_Ix digital filter input. To utilize this filter, the QE_Ix module must be enabled and its inputs must be connected to a physical RP_n pin. Example 11-2 illustrates how the input capture module can be connected to the QE_Ix digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QE1 DIGITAL FILTER INPUT ON PIN 43

```
RPINR15 = 0x2500;    /* Connect the QE1 HOME1 input to RP37 (pin 43) */
RPINR7  = 0x009;     /* Connect the IC1 input to the digital filter on the FHOME1 input */

QE1I1OC = 0x4000;    /* Enable the QE1 digital filter */
QE1ICON = 0x8000;    /* Enable the QE1 module */
```

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 11-17: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SS2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-7
- Unimplemented:** Read as '0'
- bit 6-0
- SS2R<6:0>:** Assign SPI2 Slave Select ($\overline{SS2}$) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-18: RPINR24: PERIPHERAL PIN SELECT INPUT REGISTER 24

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CSCK2R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CSDIR<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **CSCK2R<6:0>:** Assign DCI Clock Input (CSCK) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•

•

•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **CSDIR<6:0>:** Assign DCI Data Input (CSDI) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•

•

•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>**: Input Source Select for Synchronization and Trigger Operation bits⁽⁴⁾

11111 = Capture timer is unsynchronized
11110 = Capture timer is unsynchronized
11101 = Capture timer is unsynchronized
11100 = CTMU trigger is the source for the capture timer synchronization
11011 = ADC1 interrupt is the source for the capture timer synchronization⁽⁵⁾
11010 = Analog Comparator 3 is the source for the capture timer synchronization⁽⁵⁾
11001 = Analog Comparator 2 is the source for the capture timer synchronization⁽⁵⁾
11000 = Analog Comparator 1 is the source for the capture timer synchronization⁽⁵⁾
10111 = Input Capture 8 interrupt is the source for the capture timer synchronization
10110 = Input Capture 7 interrupt is the source for the capture timer synchronization
10101 = Input Capture 6 interrupt is the source for the capture timer synchronization
10100 = Input Capture 5 interrupt is the source for the capture timer synchronization
10011 = Input Capture 4 interrupt is the source for the capture timer synchronization
10010 = Input Capture 3 interrupt is the source for the capture timer synchronization
10001 = Input Capture 2 interrupt is the source for the capture timer synchronization
10000 = Input Capture 1 interrupt is the source for the capture timer synchronization
01111 = GP Timer5 is the source for the capture timer synchronization
01110 = GP Timer4 is the source for the capture timer synchronization
01101 = GP Timer3 is the source for the capture timer synchronization
01100 = GP Timer2 is the source for the capture timer synchronization
01011 = GP Timer1 is the source for the capture timer synchronization
01010 = PTGx trigger is the source for the capture timer synchronization⁽⁶⁾
01001 = Capture timer is unsynchronized
01000 = Output Compare 8 is the source for the capture timer synchronization
00111 = Output Compare 7 is the source for the capture timer synchronization
00110 = Output Compare 6 is the source for the capture timer synchronization
00101 = Output Compare 5 is the source for the capture timer synchronization
00100 = Output Compare 4 is the source for the capture timer synchronization
00011 = Output Compare 3 is the source for the capture timer synchronization
00010 = Output Compare 2 is the source for the capture timer synchronization
00001 = Output Compare 1 is the source for the capture timer synchronization
00000 = Capture timer is unsynchronized

- Note 1:** The IC32 bit in both the Odd and Even ICx must be set to enable Cascade mode.
2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
3: This bit is set by the selected input source (selected by SYNCSEL<4:0> bits); it can be read, set and cleared in software.
4: Do not use the ICx module as its own Sync or Trigger source.
5: This option should only be selected as a trigger source and not as a synchronization source.
6: Each Input Capture x module (ICx) has one PTG input source. See **Section 25.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
PTGO8 = IC1, IC5
PTGO9 = IC2, IC6
PTGO10 = IC3, IC7
PTGO11 = IC4, IC8

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 16-7: STPER: PWMx SECONDARY MASTER TIME BASE PERIOD REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
STPER<15:8>							
bit 15				bit 8			

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
STPER<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **STPER<15:0>**: PWMx Secondary Master Time Base (PMTMR) Period Value bits

REGISTER 16-8: SSEVTCMP: PWMx SECONDARY SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEVTCMP<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEVTCMP<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **SSEVTCMP<15:0>**: PWMx Secondary Special Event Compare Count Value bits

TABLE 25-1: PTG STEP COMMAND FORMAT (CONTINUED)

bit 3-0	Step Command	OPTION<3:0>	Option Description
	PTGWHI ⁽¹⁾ or PTGWLO ⁽¹⁾	0000	PWM Special Event Trigger
		0001	PWM master time base synchronization output
		0010	PWM1 interrupt
		0011	PWM2 interrupt
		0100	PWM3 interrupt
		0101	PWM4 interrupt
		0110	PWM5 interrupt
		0111	OC1 Trigger Event
		1000	OC2 Trigger Event
		1001	IC1 Trigger Event
		1010	CMP1 Trigger Event
		1011	CMP2 Trigger Event
		1100	CMP3 Trigger Event
		1101	CMP4 Trigger Event
		1110	ADC conversion done interrupt
		1111	INT2 external interrupt
	PTGIRQ ⁽¹⁾	0000	Generate PTG Interrupt 0
		0001	Generate PTG Interrupt 1
		0010	Generate PTG Interrupt 2
		0011	Generate PTG Interrupt 3
		0100	Reserved
		• • •	• • •
		1111	Reserved
	PTGTRIG ⁽²⁾	00000	PTGO0
		00001	PTGO1
		• • •	• • •
		11110	PTGO30
		11111	PTGO31

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 25-2 for the trigger output descriptions.

26.0 OP AMP/COMPARATOR MODULE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Op Amp/Comparator” (DS70000357), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX devices contain up to five comparators that can be configured in various ways. Comparators, CMP1, CMP2, CMP3 and CMP5, also have the option to be configured as op amps, with the output being brought to an external pin for gain/filtering connections. As shown in Figure 26-1, individual comparator options are specified by the comparator module’s Special Function Register (SFR) control bits.

These options allow users to:

- Select the edge for trigger and interrupt generation
- Configure the comparator voltage reference
- Configure output blanking and masking
- Configure as a comparator or op amp (CMP1, CMP2, CMP3 and CMP5 only)

Note: Not all op amp/comparator input/output connections are available on all devices. See the “Pin Diagrams” section for available connections.

FIGURE 26-1: OP AMP/COMPARATOR x MODULE BLOCK DIAGRAM

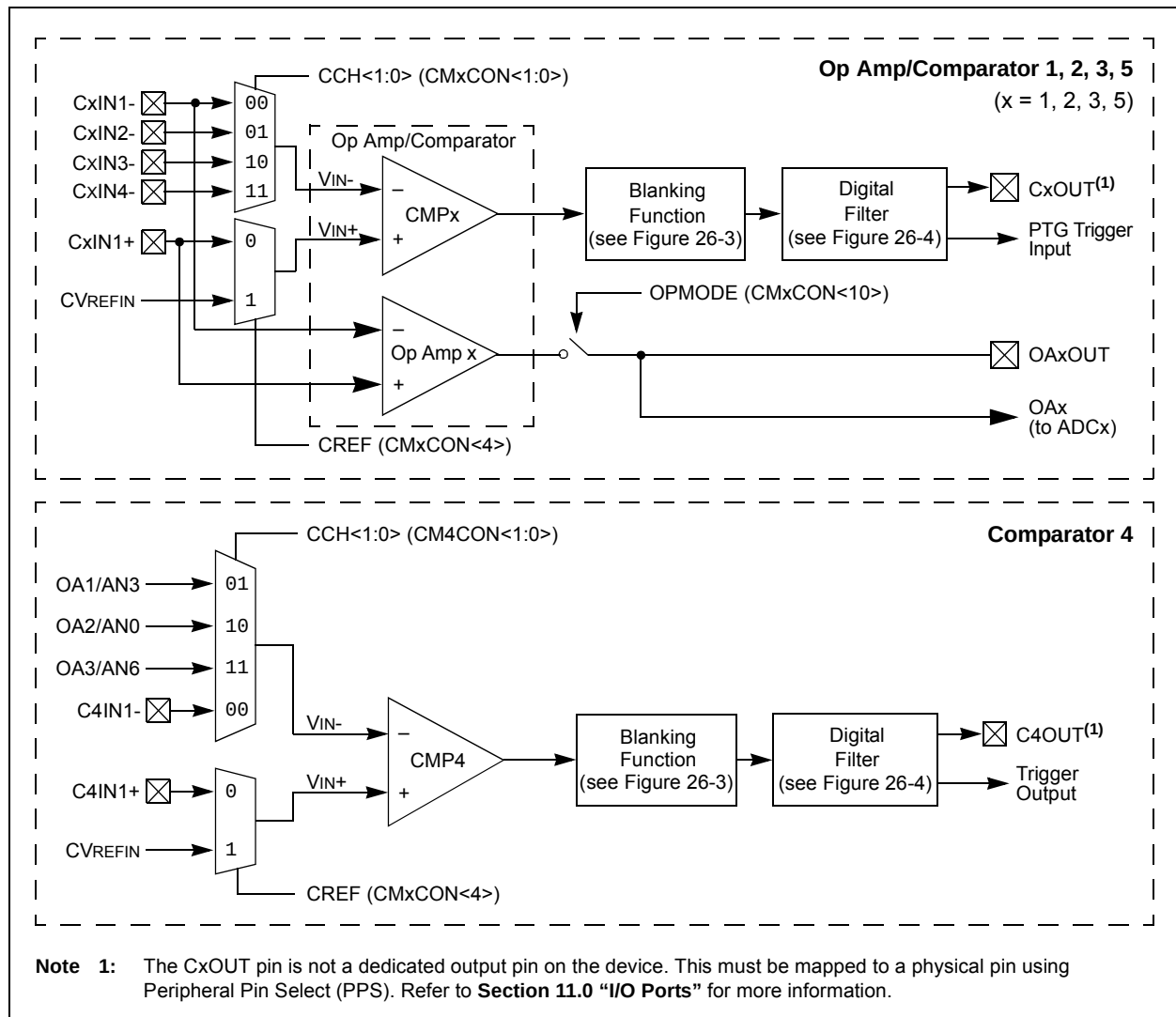
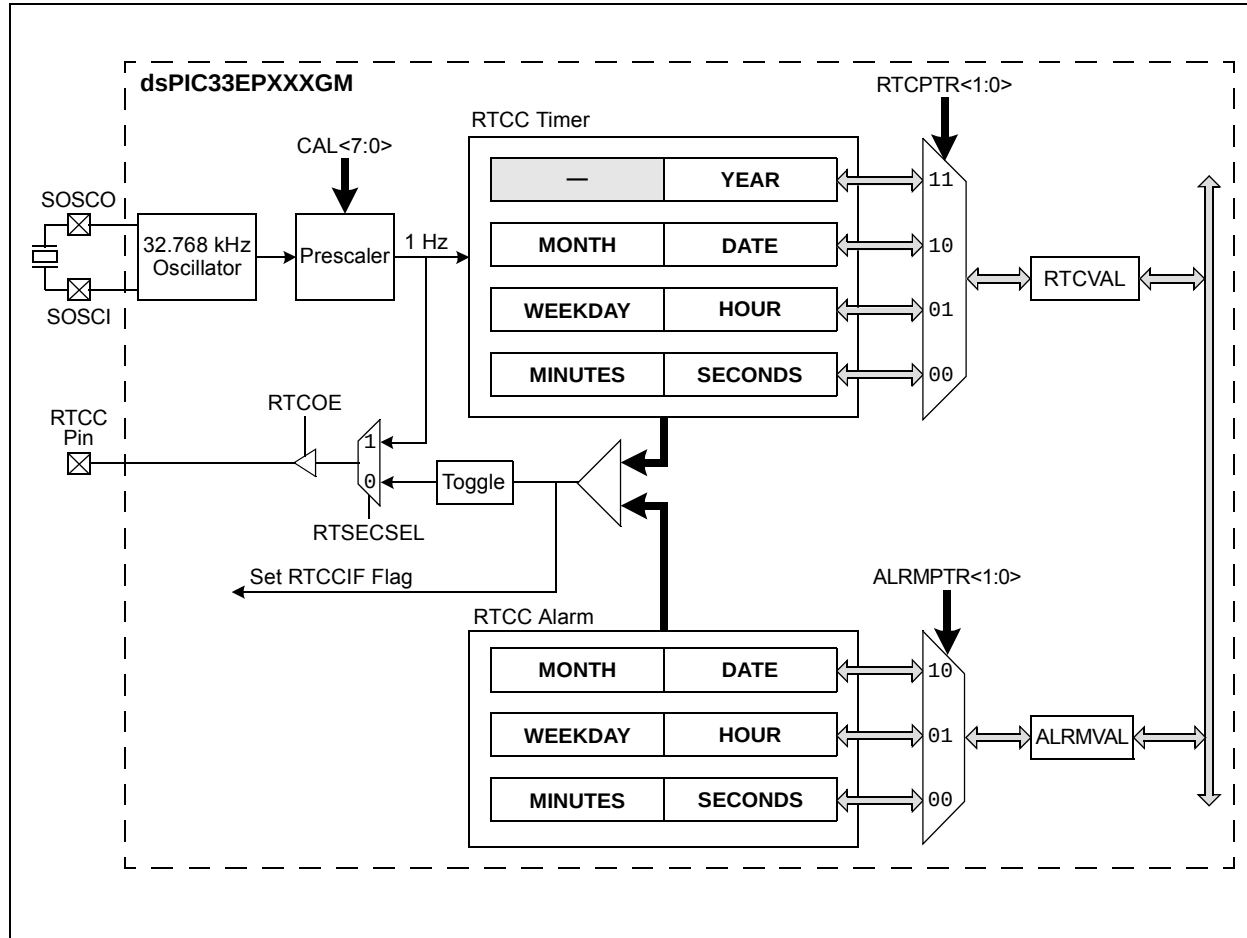


FIGURE 27-1: RTCC BLOCK DIAGRAM



Note: The RTCC is only operational on devices which include the SOSC; therefore, the RTCC module is not available on 44-pin devices.

FIGURE 33-31: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

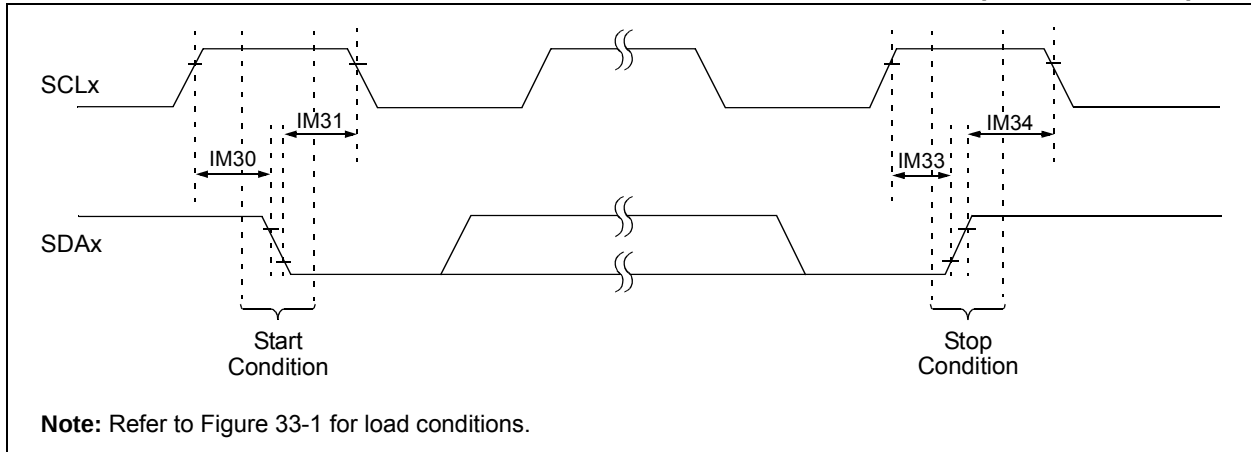


FIGURE 33-32: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

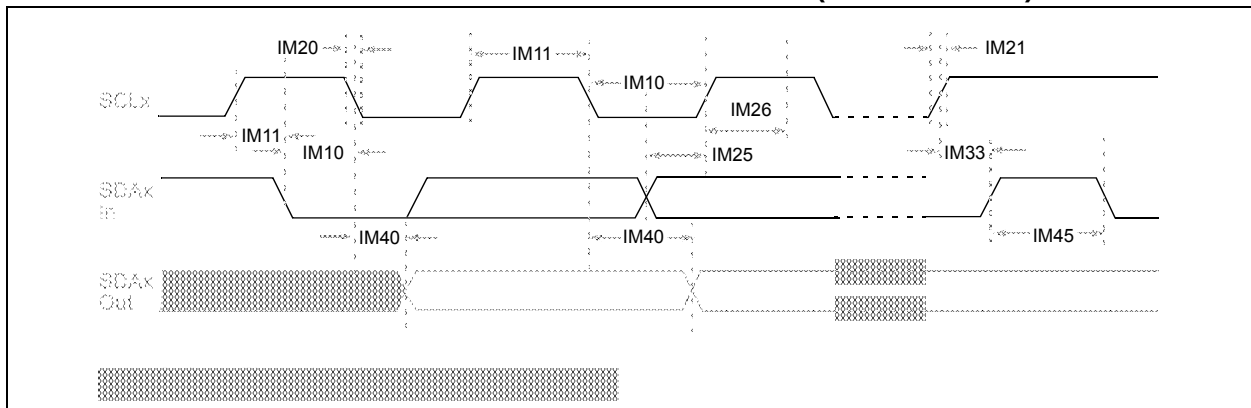


TABLE 34-5: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$			
Parameter No.	Typical	Max	Units	Conditions		
HDC40e	3.6	8	mA	+150°C	3.3V	10 MIPS
HDC42e	5	15	mA	+150°C	3.3V	20 MIPS
HDC44e	10	20	mA	+150°C	3.3V	40 MIPS

TABLE 34-6: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$			
Parameter No.	Typical	Max	Units	Conditions		
HDC20	11	25	mA	+150°C	3.3V	10 MIPS
HDC22	15	30	mA	+150°C	3.3V	20 MIPS
HDC23	21	50	mA	+150°C	3.3V	40 MIPS

TABLE 34-7: DC CHARACTERISTICS: DOZE CURRENT (I_{DOZE})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$			
Parameter No.	Typical	Max	Doze Ratio	Units	Conditions	
HDC72a	25	45	1:2	mA	+150°C	3.3V
HDC72g ⁽¹⁾	14	33	1:128	mA		

Note 1: Parameters with Doze ratios of 1:64 and 1:128 are characterized, but are not tested in manufacturing.

NOTES:

dsPIC33EPXXXGM3XX/6XX/7XX

Program Address Space	37	Peripheral Pin Select Input (dsPIC33EPGM60X/7XX Devices)	76
Memory Map for dsPIC33EP128GM3XX/6XX/7XX Devices	37	Peripheral Pin Select Input (dsPIC33EPXXXGM3XX Devices)	77
Memory Map for dsPIC33EP256GM3XX/6XX/7XX Devices	38	Peripheral Pin Select Output (dsPIC33EPXXXGM304/604 Devices)	74
Memory Map for dsPIC33EP512GM3XX/6XX/7XX Devices	39	Peripheral Pin Select Output (dsPIC33EPXXXGM306/706 Devices)	74
Program Memory		Peripheral Pin Select Output (dsPIC33EPXXXGM310/710 Devices)	75
Organization	40	PMD (dsPIC33EPXXXGM3XX Devices)	80
Reset Vector	40	PMD (dsPIC33EPXXXGM6XX/7XX Devices)	79
Program Space		PORTA (dsPIC33EPXXXGM304/604 Devices)	84
Address Construction	101	PORTA (dsPIC33EPXXXGM306/706 Devices)	84
Data Access from Program Memory Using Table Instructions	102	PORTA (dsPIC33EPXXXGM310/710 Devices)	84
Table Read Instructions		PORTB (dsPIC33EPXXXGM304/604 Devices)	85
TBLRDH	102	PORTB (dsPIC33EPXXXGM306/706 Devices)	85
TBLRDL	102	PORTB (dsPIC33EPXXXGM310/710 Devices)	85
Programmable CRC		PORTC (dsPIC33EPXXXGM304/604 Devices)	86
Control Registers	407	PORTC (dsPIC33EPXXXGM306/706 Devices)	86
Overview	406	PORTC (dsPIC33EPXXXGM310/710 Devices)	86
Setup Examples	406	PORTD (dsPIC33EPXXXGM306/706 Devices)	87
Programmable Cyclic Redundancy Check (CRC) Generator	405	PORTD (dsPIC33EPXXXGM310/710 Devices)	87
PTG		PORTE (dsPIC33EPXXXGM306/706 Devices)	88
Control Registers	351	PORTE (dsPIC33EPXXXGM310/710 Devices)	87
Introduction	349	PORTF (dsPIC33EPXXXGM306/706 Devices)	88
Output Descriptions	364	PORTF (dsPIC33EPXXXGM310/710 Devices)	88
Step Commands and Format	361	PORTG (dsPIC33EPXXXGM306/706 Devices)	89
Q		PORTG (dsPIC33EPXXXGM310/710 Devices)	89
Quadrature Encoder Interface (QEI)	257	Programmable CRC	73
Control Registers	259	PTG	56
R		PWM	57
Real-Time Clock and Calendar (RTCC)	383	PWM Generator 1	57
Referenced Sources	13	PWM Generator 2	58
Register		PWM Generator 3	58
PTGADJ (PTG Adjust)	359	PWM Generator 4	59
PTGL0 (PTG Literal 0)	359	PWM Generator 5	59
PTGQPTR (PTG Step Queue Pointer)	360	PWM Generator 6	60
PTGQUEX (PTG Step Queue x)	360	QE1	61
Register Maps		QE2	62
ADC1 and ADC2	66	Real-Time Clock and Calendar	82
CAN1 (When WIN (C1CTRL) = 0 or 1)	68	Reference Clock	78
CAN1 (When WIN (C1CTRL) = 0)	68	SPI1, SPI2 and SPI3	64
CAN1 (When WIN (C1CTRL) = 1)	69	System Control	78
CAN2 (When WIN (C1CTRL) = 0 or 1)	70	Timers	52
CAN2 (When WIN (C1CTRL) = 0)	71	UART1 and UART2	63
CAN2 (When WIN (C1CTRL) = 1)	72	UART3 and UART4	64
Configuration Byte	412	Registers	
CPU Core	46	ADxCHS0 (ADCx Input Channel 0 Select)	338
CTMU	82	ADxCHS123 (ADCx Input Channel 1, 2, 3 Select)	337
DCI	65	ADxCON1 (ADCx Control 1)	331
DMA Controller	83	ADxCON2 (ADCx Control 2)	333
I2C1 and I2C2	63	ADxCON3 (ADCx Control 3)	335
Input Capture 1-8	53	ADxCON4 (ADCx Control 4)	336
Interrupt Controller (dsPIC33EPXXXGM3XX Devices)	50	ADxCSSH (ADCx Input Scan Select High)	340
Interrupt Controller (dsPIC33EPXXXGM6XX/7XX Devices)	48	ADxCSSL (ADCx Input Scan Select Low)	342
JTAG Interface	82	ALCFGRPT (Alarm Configuration)	388
NVM	78	ALRMVAL (Alarm Minutes and Seconds Value, ALRMPTR = 00)	393
Op Amp/Comparator	81	ALRMVAL (Alarm Month and Day Value, ALRMPTR = 10)	391
Output Compare	54	ALRMVAL (Alarm Weekday and Hours Value, ALRMPTR = 01)	392
Pad Configuration	89	ALTDTRx (PWMx Alternate Dead-Time)	246
Parallel Master/Slave Port	79		

dsPIC33EPXXXGM3XX/6XX/7XX

PMCON (Parallel Master Port Control)	396	RPINR25 (Peripheral Pin Select Input 25).....	192
PMD1 (Peripheral Module Disable Control 1)	156	RPINR26 (Peripheral Pin Select Input 26).....	193
PMD2 (Peripheral Module Disable Control 2)	158	RPINR27 (Peripheral Pin Select Input 27).....	194
PMD3 (Peripheral Module Disable Control 3)	159	RPINR28 (Peripheral Pin Select Input 28).....	195
PMD4 (Peripheral Module Disable Control 4)	161	RPINR29 (Peripheral Pin Select Input 29).....	196
PMD6 (Peripheral Module Disable Control 6)	161	RPINR3 (Peripheral Pin Select Input 3).....	177
PMD7 (Peripheral Module Disable Control 7)	162	RPINR30 (Peripheral Pin Select Input 30).....	197
PMODE (Parallel Master Port Mode)	398	RPINR37 (Peripheral Pin Select Input 37).....	198
PMSTAT (Parallel Master Port Status)	402	RPINR38 (Peripheral Pin Select Input 38).....	199
POSxCNTH (Position Counter x High Word)	265	RPINR39 (Peripheral Pin Select Input 39).....	200
POSxCNTL (Position Counter x Low Word)	265	RPINR40 (Peripheral Pin Select Input 40).....	201
POSxHLD (Position Counter x Hold)	266	RPINR41 (Peripheral Pin Select Input 41).....	202
PTCON (PWMx Time Base Control)	233	RPINR7 (Peripheral Pin Select Input 7).....	178
PTCON2 (PWMx Primary Master Clock Divider Select 2)	235	RPINR8 (Peripheral Pin Select Input 8).....	179
PTGBTE (PTG Broadcast Trigger Enable)	354	RPINR9 (Peripheral Pin Select Input 9).....	180
PTGC0LIM (PTG Counter 0 Limit)	357	RPOR0 (Peripheral Pin Select Output 0).....	203
PTGC1LIM (PTG Counter 1 Limit)	358	RPOR1 (Peripheral Pin Select Output 1).....	203
PTGCON (PTG Control)	353	RPOR10 (Peripheral Pin Select Output 10).....	208
PTGCST (PTG Control/Status)	351	RPOR11 (Peripheral Pin Select Output 11).....	208
PTGHOLD (PTG Hold)	358	RPOR12 (Peripheral Pin Select Output 12).....	209
PTGSDLIM (PTG Step Delay Limit)	357	RPOR2 (Peripheral Pin Select Output 2).....	204
PTGT0LIM (PTG Timer0 Limit)	356	RPOR3 (Peripheral Pin Select Output 3).....	204
PTGT1LIM (PTG Timer1 Limit)	356	RPOR4 (Peripheral Pin Select Output 4).....	205
PTPER (PWMx Primary Master Time Base Period)	236	RPOR5 (Peripheral Pin Select Output 5).....	205
PWMCAPx (PWMx Primary Time Base Capture)	255	RPOR6 (Peripheral Pin Select Output 6).....	206
PWMCONx (PWMx Control)	242	RPOR7 (Peripheral Pin Select Output 7).....	206
QEIXCON (QEIX Control)	259	RPOR8 (Peripheral Pin Select Output 8).....	207
QEIXGECH (QEIX Greater Than or Equal Compare High Word)	270	RPOR9 (Peripheral Pin Select Output 9).....	207
QEIXGECL (QEIX Greater Than or Equal Compare Low Word)	270	RSCON (DCI Receive Slot Control)	348
QEIXICH (QEIX Initialization/Capture High Word)	268	RTCVAL (Minutes and Seconds Value, RTCPTR = 00)	390
QEIXICL (QEIX Initialization/Capture Low Word)	268	RTCVAL (Month and Day Value, RTCPTR = 10)	389
QEIXIOC (QEIX I/O Control)	261	RTCVAL (Weekday and Hours Value, RTCPTR = 01)	390
QEIXLECH (QEIX Less Than or Equal Compare High Word)	269	RTCVAL (Year Value, RTCPTR = 11)	389
QEIXLECL (QEIX Less Than or Equal Compare Low Word)	269	SDCx (PWMx Secondary Duty Cycle)	244
QEIXSTAT (QEIX Status)	263	SEVTCMP (PWMx Primary Special Event Compare)	236
RCFGCAL (RTCC Calibration and Configuration)	386	SPHASEx (PWMx Secondary Phase-Shift)	245
RCON (Reset Control)	112	SPIxCON1 (SPIx Control 1)	278
REFOCON (Reference Oscillator Control)	152	SPIxCON2 (SPIx Control 2)	280
RPINR0 (Peripheral Pin Select Input 0)	175	SPIxSTAT (SPIx Status and Control)	276
RPINR1 (Peripheral Pin Select Input 1)	176	SR (CPU STATUS)	31, 121
RPINR10 (Peripheral Pin Select Input 10)	181	SSEVTCMP (PWMx Secondary Special Event Compare)	240
RPINR11 (Peripheral Pin Select Input 11)	182	STCON (PWMx Secondary Time Base Control)	237
RPINR12 (Peripheral Pin Select Input 12)	183	STCON2 (PWMx Secondary Master Clock Divider Select 2)	239
RPINR14 (Peripheral Pin Select Input 14)	184	STPER (PWMx Secondary Master Time Base Period)	240
RPINR15 (Peripheral Pin Select Input 15)	185	T1CON (Timer1 Control)	212
RPINR16 (Peripheral Pin Select Input 16)	186	TRGCONx (PWMx Trigger Control)	247
RPINR17 (Peripheral Pin Select Input 17)	187	TRIGx (PWMx Primary Trigger Compare Value)	249
RPINR18 (Peripheral Pin Select Input 18)	188	TSCON (DCI Transmit Slot Control)	348
RPINR19 (Peripheral Pin Select Input 19)	188	TxCON (T2CON, T4CON, T6CON and T8CON Control)	216
RPINR22 (Peripheral Pin Select Input 22)	189	TyCON (T3CON, T5CON, T7CON and T9CON Control)	217
RPINR23 (Peripheral Pin Select Input 23)	190	UxMODE (UARTx Mode)	291
RPINR24 (Peripheral Pin Select Input 24)	191	UxSTA (UARTx Status and Control)	293
		VELxCNT (Velocity Counter x)	266