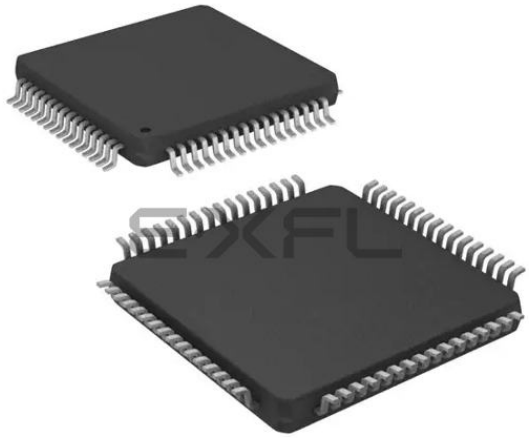
Microchip Technology - DSPIC33EP256GM306-I/PT Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 30x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gm306-i-pt

NOTES:

TABLE 4-14: PWM GENERATOR 6 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON6	0CC0	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	DTCP	—	MTBS	CAM	XPRES	IUE	0000
IOCON6	0CC2	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON6	0CC4	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	00F8
PDC6	0CC6	PDC6<15:0>																0000
PHASE6	0CC8	PHASE6<15:0>																0000
DTR6	0CCA	—	—	DTR6<13:0>														0000
ALTDTR6	0CCC	—	—	ALTDTR6<13:0>														0000
SDC6	0CCE	SDC6<15:0>																0000
SPHASE6	0CD0	SPHASE6<15:0>																0000
TRIG6	0CD2	TRGCMP<15:0>																0000
TRGCON6	0CD4	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	—	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
PWMCAP6	0CD8	PWMCAP6<15:0>																0000
LEBCON6	0CDA	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY6	0CDC	—	—	—	—	LEB<11:0>												0000
AUXCON6	0CDE	—	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-33: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGM60X/7XX DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—	INT1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>							0000
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>							0000
RPINR7	06AE	—	IC2R<6:0>							—	IC1R<6:0>							0000
RPINR8	06B0	—	IC4R<6:0>							—	IC3R<6:0>							0000
RPINR9	06B2	—	IC6R<6:0>							—	IC5R<6:0>							0000
RPINR10	06B4	—	IC8R<6:0>							—	IC7R<6:0>							0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>							0000
RPINR12	06B8	—	FLT2R<6:0>							—	FLT1R<6:0>							0000
RPINR14	06BC	—	QEB1R<6:0>							—	QEA1R<6:0>							0000
RPINR15	06BE	—	HOME1R<6:0>							—	INDX1R<6:0>							0000
RPINR16	06C0	—	QEB2R<6:0>							—	QEA2R<6:0>							0000
RPINR17	06C2	—	HOME2R<6:0>							—	INDX2R<6:0>							0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>							0000
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>							0000
RPINR22	06CC	—	SCK2R<6:0>							—	SDI2R<6:0>							0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>							0000
RPINR24	06D0	—	CSCKR<6:0>							—	CSDIR<6:0>							0000
RPINR25	06D2	—	—	—	—	—	—	—	—	—	COFSR<6:0>							0000
RPINR26	06D4	—	C2RXR<6:0>							—	C1RXR<6:0>							0000
RPINR27	06D6	—	U3CTSR<6:0>							—	U3RXR<6:0>							0000
RPINR28	06D8	—	U4CTSR<6:0>							—	U4RXR<6:0>							0000
RPINR29	06DA	—	SCK3R<6:0>							—	SDI3R<6:0>							0000
RPINR30	06DC	—	—	—	—	—	—	—	—	—	SS3R<6:0>							0000
RPINR37	06EA	—	SYNCI1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR38	06EC	—	DTCMP1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR39	06EE	—	DTCMP3R<6:0>							—	DTCMP2R<6:0>							0000
RPINR40	06F0	—	DTCMP5R<6:0>							—	DTCMP4R<6:0>							0000
RPINR41	06F2	—	—	—	—	—	—	—	—	—	DTCMP6R<6:0>							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 7-1: SR: CPU STATUS REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0(3)	R/W-0(3)	R/W-0(3)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(2)	**IPL1(2)**	**IPL0(2)**	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(2,3)

111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see Register 3-1.

2: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

3: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	PWCOL3	PWCOL2	PWCOL1	PWCOL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **PWCOL3:** Channel 3 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = No write collision is detected

bit 2 **PWCOL2:** Channel 2 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = No write collision is detected

bit 1 **PWCOL1:** Channel 1 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = No write collision is detected

bit 0 **PWCOL0:** Channel 0 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = No write collision is detected

10.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To _complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Watchdog Timer and Power-Saving Modes"** (DS70615), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

The dsPIC33EPXXXGM3XX/6XX/7XX devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGM3XX/6XX/7XX devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGM3XX/6XX/7XX devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

Note: SLEEP_MODE and IDLE_MODE are constants defined in the Assembler Include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

```
PWRSAV  #SLEEP_MODE    ; Put the device into Sleep mode
PWRSAV  #IDLE_MODE     ; Put the device into Idle mode
```

10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled
- The LPRC clock continues to run in Sleep mode if the WDT is enabled
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled

The device wakes up from Sleep mode on any of the these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby mode when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

10.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions
- The WDT is automatically cleared
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 “Peripheral Module Disable”**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the TSIDL bit in the Timer1 Control register (T1CON<13>).

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

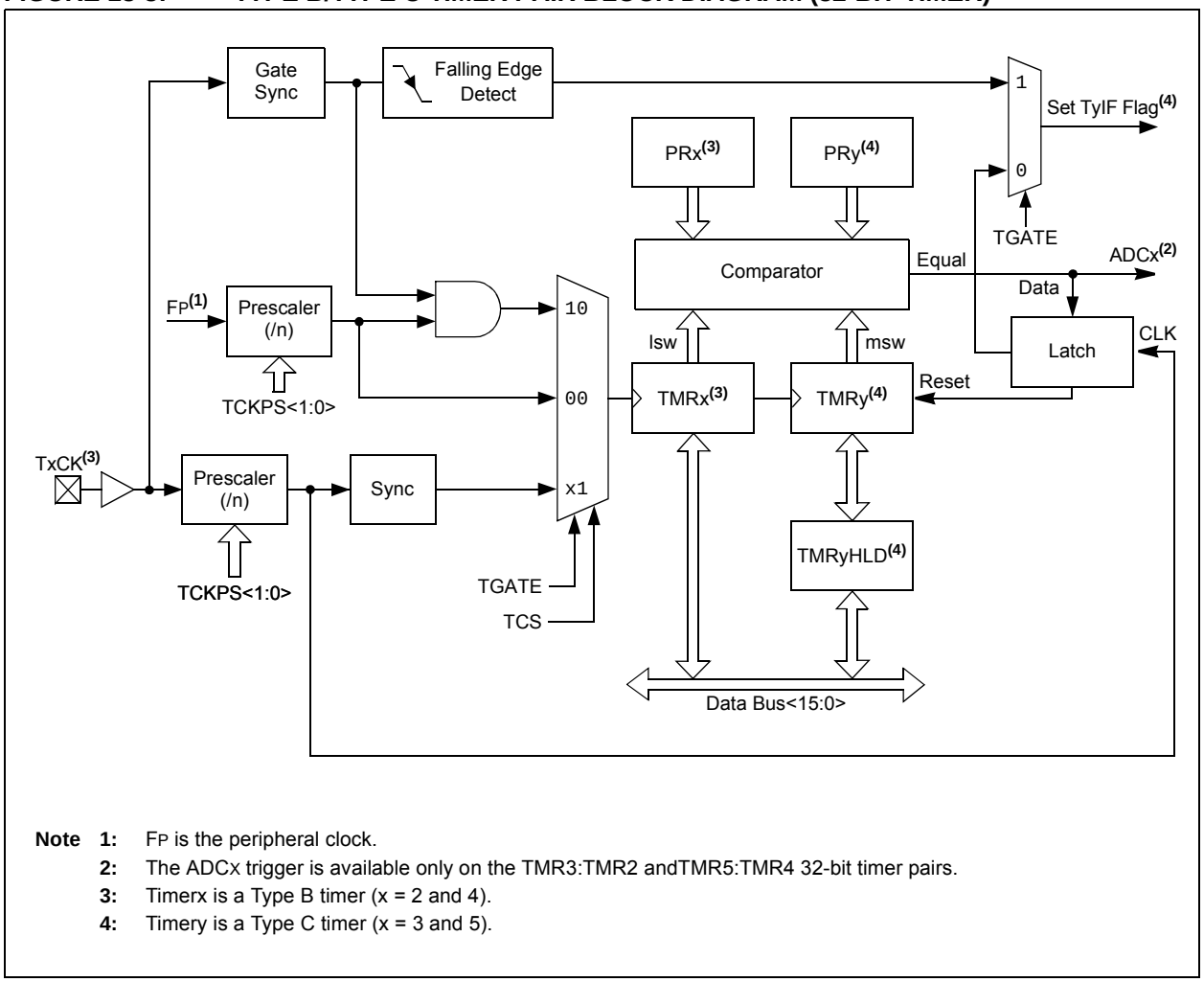
Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss	010 1100	I	RPI44
000 0001	I	CMP1(1)	010 1101	I	RPI45
000 0010	I	CMP2(1)	010 1110	I	RPI46
000 0011	I	CMP3(1)	010 1111	I	RPI47
000 0100	I	CMP4(1)	011 0000	I/O	RP48
000 0101	—	—	011 0001	I/O	RP49
000 0110	I	PTGO30(1)	011 0010	I	RPI50
000 0111	I	PTGO31(1)	011 0011	I	RPI51
000 1000	I	INDX1(1)	011 0100	I	RPI52
000 1001	I	HOME1(1)	011 0101	I	RPI53
000 1010	I	INDX2(1)	011 0110	I/O	RP54
000 1011	I	HOME2(1)	011 0111	I/O	RP55
000 1100	I	CMP5(1)	011 1000	I/O	RP56
000 1101	—	—	011 1001	I/O	RP57
000 1110	—	—	011 1010	I	RPI58
000 1111	—	—	011 1011	—	—
001 0000	I	RPI16	011 1100	I	RPI60
001 0001	I	RPI17	011 1101	I	RPI61
001 0010	I	RPI18	011 1110	—	—
001 0011	I	RPI19	011 1111	I	RPI 63
001 0100	I/O	RP20	100 0000	—	—
001 0101	—	—	100 0001	—	—
001 0110	—	—	100 0010	—	—
001 0111	—	—	100 0011	—	—
001 1000	I	RPI24	100 0100	—	—
001 1001	I	RPI25	100 0101	I/O	RP69
001 1010	—	—	100 0110	I/O	RP70
001 1011	I	RPI27	100 0111	—	—
001 1100	I	RPI28	100 1000	I	RPI72
001 1101	—	—	100 1001	—	—
001 1110	—	—	100 1010	—	—
001 1111	—	—	100 1011	—	—
010 0000	I	RPI32	100 1100	I	RPI76
010 0001	I	RPI33	100 1101	I	RPI77
010 0010	I	RPI34	100 1110	—	—
010 0011	I/O	RP35	100 1111	—	—
010 0100	I/O	RP36	101 0000	I	RPI80
010 0101	I/O	RP37	101 0001	I/O	RP81
010 0110	I/O	RP38	101 0010	—	—
010 0111	I/O	RP39	101 0011	—	—
010 1000	I/O	RP40	101 0100	—	—

Legend: Shaded rows indicate PPS Input register values that are unimplemented.

Note 1: See **Section 11.4.4.1 “Virtual Connections”** for more information on selecting this pin assignment.

6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
   a) Only one “output” function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
   b) It is possible to assign a “remappable output” function to multiple pins and externally short or tie them together for increased current drive.
   c) If any “dedicated output” function is enabled on a pin, it will take precedence over any remappable “output” function.
   d) If any “dedicated digital” (input or output) function is enabled on a pin, any number of “input” remappable functions can be mapped to the same pin.
   e) If any “dedicated analog” function(s) are enabled on a given pin, “digital input(s)” of any kind will all be disabled, although a single “digital output”, at the user’s cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADCx to convert the digital output logic level or to toggle a digital output on a comparator or ADCx input provided there is no external analog input, such as for a built-in self-test.
   f) Any number of “input” remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable “output”.
   g) The TRIS registers control *only* the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRIS setting. The TRIS register *does not* control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRIS settings, which means that the TRIS bit must be set to input for pins with only remappable input function(s) assigned.
   h) All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin is disabled. Only the Analog Pin Select registers control the digital input buffer, *not* the TRIS register. The user must disable the analog function on a pin using the Analog Pin Select registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)



Note 1: FP is the peripheral clock.
2: The ADCx trigger is available only on the TMR3:TMR2 andTMR5:TMR4 32-bit timer pairs.
3: Timerx is a Type B timer (x = 2 and 4).
4: Timery is a Type C timer (x = 3 and 5).

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Trigger/Synchronization Source Selection bits

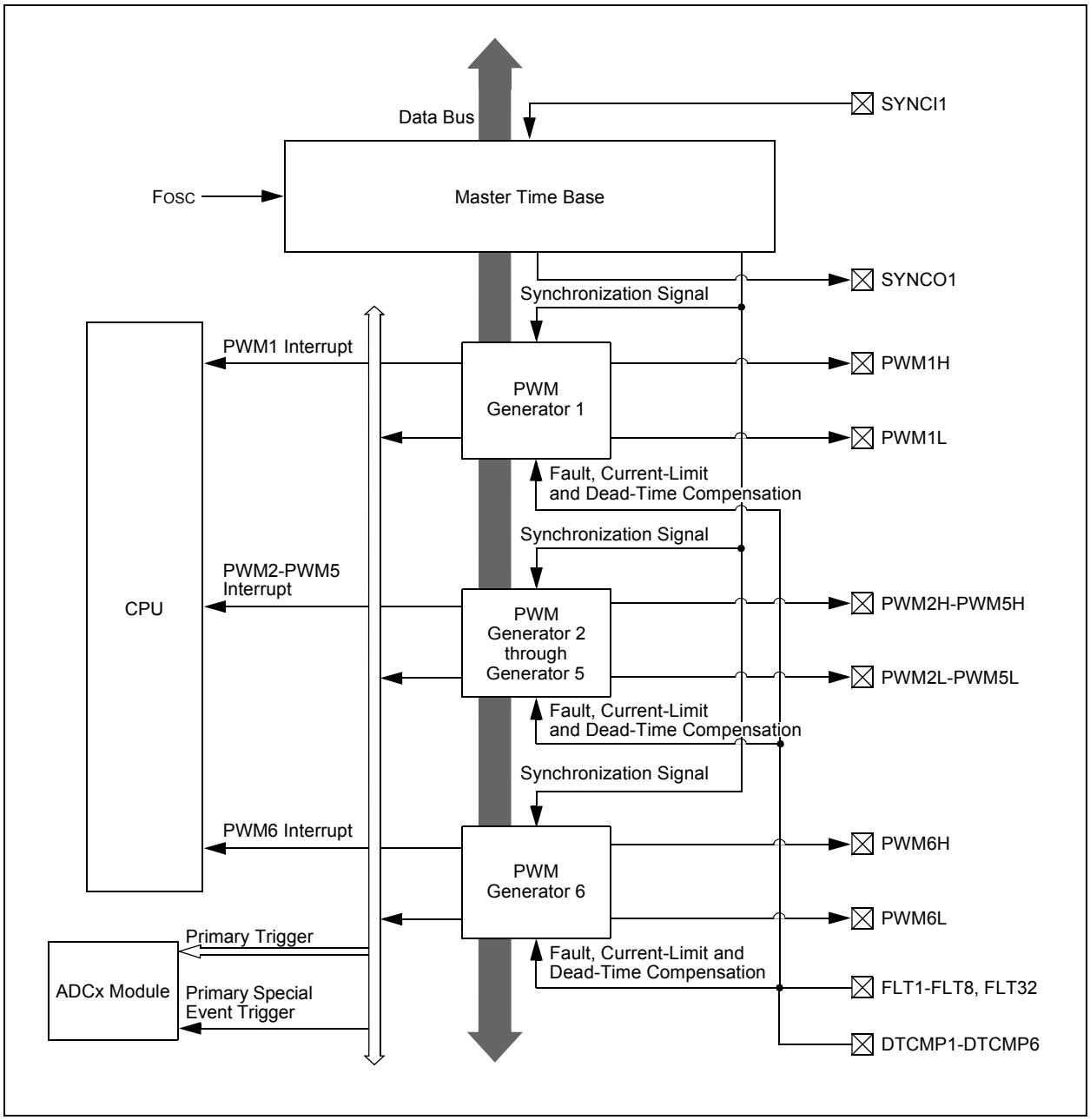
11111 = OCxRS compare event is used for synchronization
11110 = INT2 is the source for compare timer synchronization
11101 = INT1 is the source for compare timer synchronization
11100 = CTMU trigger is the source for compare timer synchronization
11011 = ADC1 interrupt is the source for compare timer synchronization
11010 = Analog Comparator 3 is the source for compare timer synchronization
11001 = Analog Comparator 2 is the source for compare timer synchronization
11000 = Analog Comparator 1 is the source for compare timer synchronization
10111 = Input Capture 8 interrupt is the source for compare timer synchronization
10110 = Input Capture 7 interrupt is the source for compare timer synchronization
10101 = Input Capture 6 interrupt is the source for compare timer synchronization
10100 = Input Capture 5 interrupt is the source for compare timer synchronization
10011 = Input Capture 4 interrupt is the source for compare timer synchronization
10010 = Input Capture 3 interrupt is the source for compare timer synchronization
10001 = Input Capture 2 interrupt is the source for compare timer synchronization
10000 = Input Capture 1 interrupt is the source for compare timer synchronization
01111 = GP Timer5 is the source for compare timer synchronization
01110 = GP Timer4 is the source for compare timer synchronization
01101 = GP Timer3 is the source for compare timer synchronization
01100 = GP Timer2 is the source for compare timer synchronization
01011 = GP Timer1 is the source for compare timer synchronization
01010 = PTGx trigger is the source for compare timer synchronization(3)
01001 = Compare timer is unsynchronized
01000 = Output Compare 8 is the source for compare timer synchronization(1,2)
00111 = Output Compare 7 is the source for compare timer synchronization(1,2)
00110 = Output Compare 6 is the source for compare timer synchronization(1,2)
00101 = Output Compare 5 is the source for compare timer synchronization(1,2)
00100 = Output Compare 4 is the source for compare timer synchronization(1,2)
00011 = Output Compare 3 is the source for compare timer synchronization(1,2)
00010 = Output Compare 2 is the source for compare timer synchronization(1,2)
00001 = Output Compare 1 is the source for compare timer synchronization(1,2)
00000 = Compare timer is unsynchronized

Note 1: Do not use the OCx module as its own synchronization or trigger source.

2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

3: Each Output Compare x module (OCx) has one PTG Trigger/Sync source. See **Section 25.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO4 = OC1, OC5
PTGO5 = OC2, OC6
PTGO6 = OC3, OC7
PTGO7 = OC4, OC8

FIGURE 16-1: HIGH-SPEED PWMx MODULE ARCHITECTURAL OVERVIEW



REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^2C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I^2C master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; hardware clears at the end of the master Acknowledge sequence
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^2C master)
1 = Enables Receive mode for I^2C; hardware clears at the end of the eighth bit of a master receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^2C master)
1 = Initiates Stop condition on SDAx and SCLx pins; hardware clears at the end of a master Stop sequence
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware clears at the end of a master Repeated Start sequence
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Start condition on SDAx and SCLx pins; hardware clears at the end of a master Start sequence
0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

24.2 DCI Control Registers

REGISTER 24-1: DCICON1: DCI CONTROL REGISTER 1

R/W-0	r-0	R/W-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0
DCIEN	r	DCISIDL	r	DLOOP	CSCKD	CSCKE	COFSD
bit 15							bit 8

R/W-0	R/W-0	R/W-0	r-0	r-0	r-0	R/W-0	R/W-0
UNFM	CSDOM	DJST	r	r	r	COFSM1	COFSM0
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DCIEN:** DCI Module Enable bit
1 = DCI module is enabled
0 = DCI module is disabled

bit 14 **Reserved:** Read as '0'

bit 13 **DCISIDL:** DCI Stop in Idle Control bit
1 = Module will halt in CPU Idle mode
0 = Module will continue to operate in CPU Idle mode

bit 12 **Reserved:** Read as '0'

bit 11 **DLOOP:** Digital Loopback Mode Control bit
1 = Digital Loopback mode is enabled; CSDI and CSDO pins are internally connected
0 = Digital Loopback mode is disabled

bit 10 **CSCKD:** Sample Clock Direction Control bit
1 = CSCK pin is an input when DCI module is enabled
0 = CSCK pin is an output when DCI module is enabled

bit 9 **CSCKE:** Sample Clock Edge Control bit
1 = Data changes on serial clock falling edge, sampled on serial clock rising edge
0 = Data changes on serial clock rising edge, sampled on serial clock falling edge

bit 8 **COFSD:** Frame Synchronization Direction Control bit
1 = COFS pin is an input when DCI module is enabled
0 = COFS pin is an output when DCI module is enabled

bit 7 **UNFM:** Underflow Mode bit
1 = Transmits last value written to the Transmit registers on a transmit underflow
0 = Transmits '0's on a transmit underflow

bit 6 **CSDOM:** Serial Data Output Mode bit
1 = CSDO pin will be tri-stated during disabled transmit time slots
0 = CSDO pin drives '0's during disabled transmit time slots

bit 5 **DJST:** DCI Data Justification Control bit
1 = Data transmission/reception is begun during the same serial clock cycle as the frame synchronization pulse
0 = Data transmission/reception is begun one serial clock cycle after the frame synchronization pulse

bit 4-2 **Reserved:** Read as '0'

bit 1-0 **COFSM<1:0>:** Frame Sync Mode bits
11 = 20-Bit AC-Link mode
10 = 16-Bit AC-Link mode
01 = I^2S Frame Sync mode
00 = Multi-Channel Frame Sync mode

REGISTER 25-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)

bit 1-0 **PTGITM<1:0>:** PTG Input Trigger Command Operating Mode bits(1)

11 = Single level detect with step delay is not executed on exit of command (regardless of PTGCTRL command)
10 = Single level detect with step delay is executed on exit of command
01 = Continuous edge detect with step delay is not executed on exit of command (regardless of PTGCTRL command)
00 = Continuous edge detect with step delay is executed on exit of command

Note 1: These bits apply to the PTGWHI and PTGWLO commands only.

2: This bit is only used with the PTGCTRL Step command software trigger option.

TABLE 30-1: CONFIGURATION BYTE REGISTER MAP

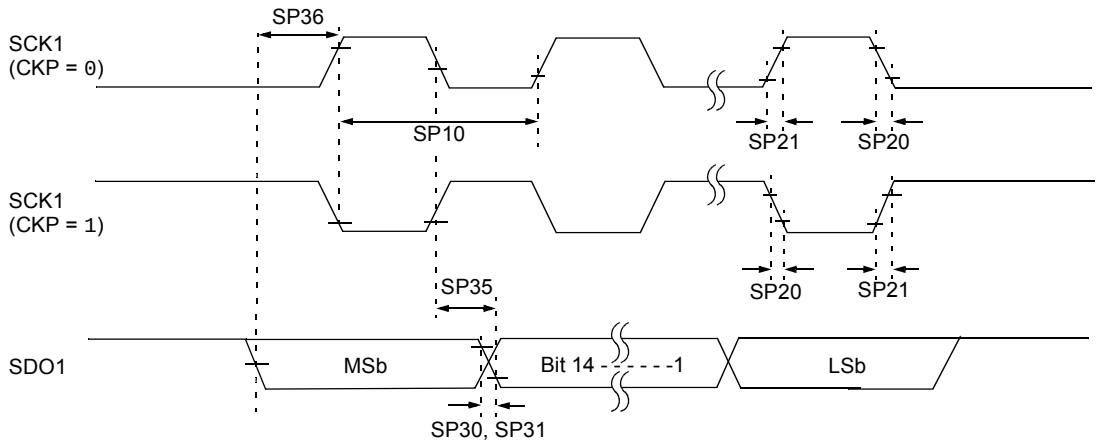
File Name	Address	Device Memory Size (Kbytes)	Bits 23-8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0157EC	128	—	—	—	—	—	—	—	—	—
	02AFEC	256									
	0557EC	512									
Reserved	0157EE	128	—	—	—	—	—	—	—	—	—
	02AFEE	256									
	0557EE	512									
FICD	0157F0	128	—	Reserved(2)	—	JTAGEN	Reserved(1)	Reserved(2)	—	ICS<1:0>	
	02AFF0	256									
	0557F0	512									
FPOR	0157F2	128	—	WDTWIN<1:0>		ALTI2C2	ALTI2C1	BOREN	—	—	—
	02AFF2	256									
	0557F2	512									
FWDT	0157F4	128	—	FWDTEN	WINDIS	PLLKEN	WDTPRE	WDTPOST<3:0>			
	02AFF4	256									
	0557F4	512									
FOSC	0157F6	128	—	FCKSM<1:0>		IOL1WAY	—	—	OSCIOFNC	POSCMD<1:0>	
	02AFF6	256									
	0557F6	512									
FOSCSEL	0157F8	128	—	IESO	PWMLOCK	—	—	—	FNOSC<2:0>		
	02AFF8	256									
	0557F8	512									
FGS	0157FA	128	—	—	—	—	—	—	—	GCP	GWRP
	02AFFA	256									
	0557FA	512									
Reserved	0157FC	128	—	—	—	—	—	—	—	—	—
	02AFFC	256									
	0557FC	512									
Reserved	0157FE	128	—	—	—	—	—	—	—	—	—
	02AFFE	256									
	0557FE	512									

Legend: — = unimplemented, read as '1'.

Note 1: This bit is reserved and must be programmed as '0'.

2: This bit is reserved and must be programmed as '1'.

FIGURE 33-24: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 33-1 for load conditions.

TABLE 33-41: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	**(Note 3)**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 33-49: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	**Symbol**	**Characteristic(3)**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			1 MHz mode(1)	0.5	—	µs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(1)	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(1)	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.6	—	µs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25		µs	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode(1)	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	400	pF	
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	**(Note 2)**

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: The Typical value for this parameter is 130 ns.

3: These parameters are characterized, but not tested in manufacturing.

34.1 High-Temperature DC Characteristics

TABLE 34-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Max MIPS
			dsPIC33EPXXXGM3XX/6XX/7XX
HDC5	3.0 to 3.6V(1)	-40°C to +150°C	40

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules, such as the ADC, may have degraded performance. Device functionality is tested but not characterized.

TABLE 34-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
High-Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+155	°C
Operating Ambient Temperature Range	TA	-40	—	+150	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 34-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Parameter No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
Operating Voltage							
HDC10	**Supply Voltage**						
	VDD	—	3.0	3.3	3.6	V	-40°C to +150°C

TABLE 34-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C			
Parameter No.	Typical	Max	Units	Conditions		
Power-Down Current (IPD)						
HDC60e	4.1	6	mA	+150°C	3.3V	Base Power-Down Current **(Notes 1, 3)**
HDC61c	15	30	µA	+150°C	3.3V	Watchdog Timer Current: ΔIWDT **(Notes 2, 4)**

Note 1: Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to VSS. WDT, etc., are all switched off and VREGS (RCON<8>) = 1.

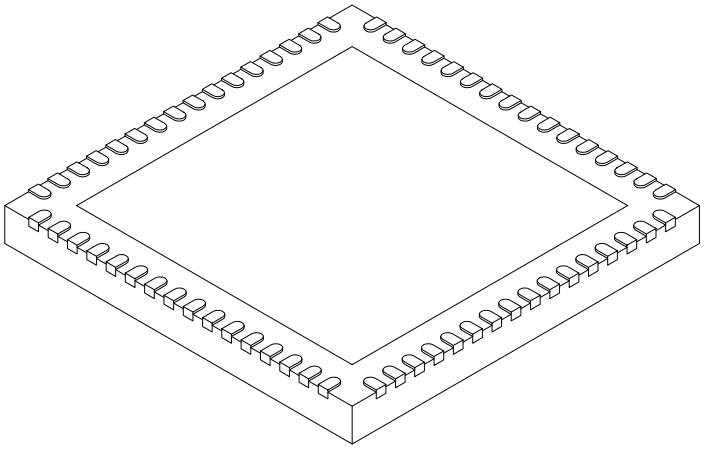
2: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

3: These currents are measured on the device containing the most memory in this family.

4: These parameters are characterized, but are not tested in manufacturing.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.15 x 7.15 Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.05	7.15	7.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.05	7.15	7.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149C Sheet 2 of 2