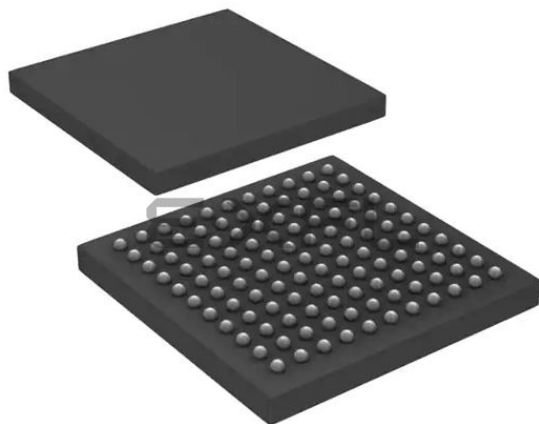




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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gm310-i-bg

dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 2: PIN NAMES: dsPIC33EP128/256/512GM310/710 DEVICES^(1,2,3) (CONTINUED)

Pin #	Full Pin Name	Pin #	Full Pin Name
E1	PWM6H/T8CK/RD4	J8	No Connect
E2	PWM6L/T9CK/RD3	J9	No Connect
E3	AN19/RP118/PMA5/RG6	J10	AN41/RP81/RE1
E4	PWM5H/RD2	J11	AN30/SDA1/RPI52/RC4
E5	No Connect	K1	PGED3/OA2IN-/AN2/C2IN1-/SS1/RPI32/CTED2/RB0
E6	RP113/RG1	K2	PGEC3/CVREF+/OA1OUT/AN3/C1IN4-/C4IN2-/RPI33/CTED1/RB1
E7	No Connect	K3	VREF+/AN34/PMA7/RF10
K4	OA3OUT/AN6/C3IN4-/C4IN4-/C4IN1+/RP48/OCFB/RC0	L3	AVss
K5	No Connect	L4	OA3IN-/AN7/C3IN1-/C4IN1-/RP49/RC1
K6	AN37/RF12	L5	OA3IN+/AN8/C3IN3-/C3IN1+/RPI50/U1RTS/BCLK1/FLT3/PMA13/RC2
K7	AN14/RPI94/FLT7/PMA1/RE14	L6	AN36/RF13
K8	VDD	L7	AN13/C3IN2-/U2CTS/FLT6/PMA10/RE13
K9	AN39/RD15	L8	AN15/RPI95/FLT8/PMA0/RE15
K10	OA5IN+/AN24/C5IN3-/C5IN1+/SDO1/RP20/T1CK/RA4	L9	AN38/RD14
K11	AN40/RPI80/RE0	L10	SDA2/RPI24/PMA9/RA8
L1	PGEC1/OA1IN+/AN4/C1IN3-/C1IN1+/C2IN3-/RPI34/RB2	L11	FLT32/SCL2/RP36/PMA8/RB4
L2	VREF-/AN33/PMA6/RF9		

- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- 3:** The availability of I²C™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5.4>). See **Section 30.0 “Special Features”** for more information.

NOTES:

dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
INDX1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Index1 pulse input.
HOME1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Home1 pulse input.
QEA1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase A input in QE11 mode. Auxiliary timer external clock input in Timer mode.
QEB1 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase A input in QE11 mode. Auxiliary timer external gate input in Timer mode.
CNTCMP1 ⁽¹⁾	O	—	Yes	Quadrature Encoder Compare Output 1.
INDX2 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Index2 Pulse input.
HOME2 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Home2 Pulse input.
QEA2 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase A input in QE12 mode. Auxiliary timer external clock input in Timer mode.
QEB2 ⁽¹⁾	I	ST	Yes	Quadrature Encoder Phase B input in QE12 mode. Auxiliary timer external gate input in Timer mode.
CNTCMP2 ⁽¹⁾	O	—	Yes	Quadrature Encoder Compare Output 2.
COFS	I/O	ST	Yes	Data Converter Interface frame synchronization pin.
CSCK	I/O	ST	Yes	Data Converter Interface serial clock input/output pin.
CSDI	I	ST	Yes	Data Converter Interface serial data input pin.
CSDO	O	—	Yes	Data Converter Interface serial data output pin.
C1RX	I	ST	Yes	CAN1 bus receive pin.
C1TX	O	—	Yes	CAN1 bus transmit pin
C2RX	I	ST	Yes	CAN2 bus receive pin.
C2TX	O	—	Yes	CAN2 bus transmit pin
RTCC	O	—	No	Real-Time Clock and Calendar alarm output.
CVREF	O	Analog	No	Comparator Voltage Reference output.
C1IN1+, C1IN2-, C1IN1-, C1IN3- C1OUT	I O	Analog —	No Yes	Comparator 1 inputs. Comparator 1 output.
C2IN1+, C2IN2-, C2IN1-, C2IN3- C2OUT	I O	Analog —	No Yes	Comparator 2 inputs. Comparator 2 output.
C3IN1+, C3IN2-, C2IN1-, C3IN3- C3OUT	I O	Analog —	No Yes	Comparator 3 inputs. Comparator 3 output.
C4IN1+, C4IN2-, C4IN1-, C4IN3- C4OUT	I O	Analog —	No Yes	Comparator 4 inputs. Comparator 4 output.
C5IN1-, C5IN2-, C5IN3-, C5IN4-, C5IN1+ C5OUT	I O	Analog —	No Yes	Comparator 5 inputs. Comparator 5 output.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

Note 1: This pin is not available on all devices. For more information, see the “Pin Diagrams” section for pin availability.

2: AVDD must be connected at all times.

dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP256GM3XX/6XX/7XX DEVICES⁽¹⁾

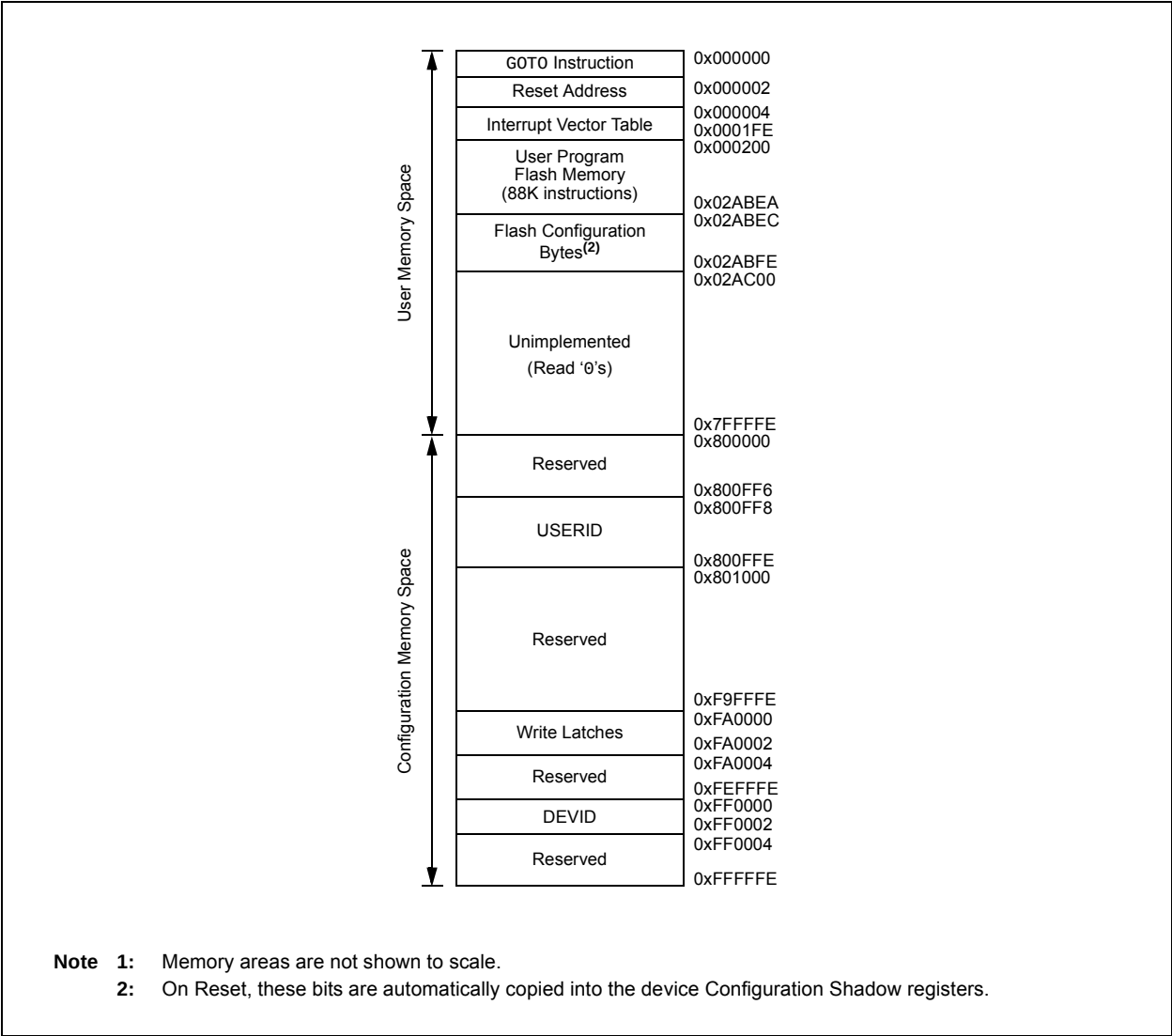


TABLE 4-21: DCI REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DCICON1	0280	DCIEN	r	DCISIDL	r	DLOOP	CCKD	CCKE	COFSD	UNFM	CSDOM	DJST	r	r	r	COFSM1	COFSM0	0000
DCICON2	0282	r	r	r	r	BLN1	BLN0	r	COFSG3	COFSG2	COFSG1	COFSG0	r	WS3	WS2	WS1	WS0	0000
DCICON3	0284	r	r	r	r	BCG<11:0>												0000
DCISTAT	0286	r	r	r	r	SLOT3	SLOT2	SLOT1	SLOT0	r	r	r	r	ROV	RFUL	TUNF	TMPTY	0000
TSCON	0288	TSE<15:0>																0000
RSCON	028C	RSE<15:0>																0000
RXBUF0	0290	Receive 0 Data Register																uuuu
RXBUF1	0292	Receive 1 Data Register																uuuu
RXBUF2	0294	Receive 2 Data Register																uuuu
RXBUF3	0296	Receive 3 Data Register																uuuu
TXBUF0	0298	Transmit 0 Data Register																0000
TXBUF1	029A	Transmit 1 Data Register																0000
TXBUF2	029C	Transmit 2 Data Register																0000
TXBUF3	029E	Transmit 3 Data Register																0000

Legend: u = unchanged; r = reserved; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: CAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES⁽¹⁾

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0500-051E	See definition when WIN = x																
C2BUFNT1	0520	F3BP3	F3BP2	F3BP1	F3BP0	F2BP3	F2BP2	F2BP1	F2BP0	F1BP3	F1BP2	F1BP1	F1BP0	F0BP3	F0BP2	F0BP1	F0BP0	0000
C2BUFNT2	0522	F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0	F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0	0000
C2BUFNT3	0524	F11BP3	F11BP2	F11BP1	F11BP0	F10BP3	F10BP2	F10BP1	F10BP0	F9BP3	F9BP2	F9BP1	F9BP0	F8BP3	F8BP2	F8BP1	F8BP0	0000
C2BUFNT4	0526	F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0	F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0	0000
C2RXM0SID	0530	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXM0EID	0532	EID<15:0>																xxxx
C2RXM1SID	0534	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXM1EID	0536	EID<15:0>																xxxx
C2RXM2SID	0538	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXM2EID	053A	EID<15:0>																xxxx
C2RXF0SID	0540	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF0EID	0542	EID<15:0>																xxxx
C2RXF1SID	0544	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF1EID	0546	EID<15:0>																xxxx
C2RXF2SID	0548	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF2EID	054A	EID<15:0>																xxxx
C2RXF3SID	054C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF3EID	054E	EID<15:0>																xxxx
C2RXF4SID	0550	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF4EID	0552	EID<15:0>																xxxx
C2RXF5SID	0554	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF5EID	0556	EID<15:0>																xxxx
C2RXF6SID	0558	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF6EID	055A	EID<15:0>																xxxx
C2RXF7SID	055C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF7EID	055E	EID<15:0>																xxxx
C2RXF8SID	0560	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF8EID	0562	EID<15:0>																xxxx
C2RXF9SID	0564	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF9EID	0566	EID<15:0>																xxxx
C2RXF10SID	0568	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF10EID	056A	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA<15> is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses an EDS or PSV page
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing. However, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSxPAG register is incremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA<15> bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-64 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA<15> bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

TABLE 4-64: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS AND PSV SPACE BOUNDARIES^(2,3,4)

O/U, R/W	Operation	Before			After		
		DSxPAG	DS EA<15>	Page Description	DSxPAG	DS EA<15>	Page Description
O, Read	[++Wn] or [Wn++]	DSRPAG = 0x1FF	1	EDS: Last Page	DSRPAG = 0x1FF	0	See Note 1
O, Read		DSRPAG = 0x2FF	1	PSV: Last lsw Page	DSRPAG = 0x300	1	PSV: First MSB Page
O, Read		DSRPAG = 0x3FF	1	PSV: Last MSB Page	DSRPAG = 0x3FF	0	See Note 1
O, Write		DSWPAG = 0x1FF	1	EDS: Last Page	DSWPAG = 0x1FF	0	See Note 1
U, Read	[- -Wn] or [Wn - -]	DSRPAG = 0x001	1	PSV Page	DSRPAG = 0x001	0	See Note 1
U, Read		DSRPAG = 0x200	1	PSV: First lsw Page	DSRPAG = 0x200	0	See Note 1
U, Read		DSRPAG = 0x300	1	PSV: First MSB Page	DSRPAG = 0x2FF	1	PSV: Last lsw Page

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the Base Data Space (0x0000-0x8000).

2: An EDS access with DSxPAG = 0x000 will generate an address error trap.

3: Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.

4: Pseudo Linear Addressing is not supported for large offsets.

11.7 Peripheral Pin Select Registers

REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	INT1R<6:0>						
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **INT1R<6:0>:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•
•
•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

dsPIC33EPXXXGM3XX/6XX/7XX

14.1 Input Capture Control Registers

REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/HC/HS-0	R/HC/HS-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7						bit 0	

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **ICSIDL:** Input Capture x Stop in Idle Mode Control bit
1 = Input Capture x halts in CPU Idle mode
0 = Input Capture x continues to operate in CPU Idle mode
- bit 12-10 **ICTSEL<2:0>:** Input Capture x Timer Select bits
111 = Peripheral clock (FP) is the clock source of ICx
110 = Reserved
101 = Reserved
100 = T1CLK is the clock source of ICx (only the synchronous clock is supported)
011 = T5CLK is the clock source of ICx
010 = T4CLK is the clock source of ICx
001 = T2CLK is the clock source of ICx
000 = T3CLK is the clock source of ICx
- bit 9-7 **Unimplemented:** Read as '0'
- bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits
(this field is not used if ICM<2:0> = 001 or 111)
11 = Interrupts on every fourth capture event
10 = Interrupts on every third capture event
01 = Interrupts on every second capture event
00 = Interrupts on every capture event
- bit 4 **ICOV:** Input Capture x Overflow Status Flag bit (read-only)
1 = Input Capture x buffer overflow occurred
0 = No Input Capture x buffer overflow occurred
- bit 3 **ICBNE:** Input Capture x Buffer Not Empty Status bit (read-only)
1 = Input Capture x buffer is not empty, at least one more capture value can be read
0 = Input Capture x buffer is empty
- bit 2-0 **ICM<2:0>:** Input Capture x Mode Select bits
111 = Input Capture x functions as an interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
110 = Unused (module disabled)
101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
011 = Capture mode, every rising edge (Simple Capture mode)
010 = Capture mode, every falling edge (Simple Capture mode)
001 = Capture mode, every edge, rising and falling (Edge Detect mode, ICI<1:0>), is not used in this mode)
000 = Input Capture x module is turned off

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 21-4: CxCTRL: CANx FIFO CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
DMABS2	DMABS1	DMABS0	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FSA4	FSA3	FSA2	FSA1	FSA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **DMABS<2:0>**: DMA Buffer Size bits

111 = Reserved

110 = 32 buffers in RAM

101 = 24 buffers in RAM

100 = 16 buffers in RAM

011 = 12 buffers in RAM

010 = 8 buffers in RAM

001 = 6 buffers in RAM

000 = 4 buffers in RAM

bit 12-5 **Unimplemented**: Read as '0'

bit 4-0 **FSA<4:0>**: FIFO Area Starts with Buffer bits

11111 = Receive Buffer RB31

11110 = Receive Buffer RB30

•

•

•

00001 = Transmit/Receive Buffer TRB1

00000 = Transmit/Receive Buffer TRB0

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 22-3: CTMUICON: CTMU CURRENT CONTROL REGISTER⁽³⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0
bit 15						bit 8	

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-10 **ITRIM<5:0>**: Current Source Trim bits

011111 = Maximum positive change from nominal current + 62%

011110 = Maximum positive change from nominal current + 60%

.

.

.

000010 = Minimum positive change from nominal current + 4%

000001 = Minimum positive change from nominal current + 2%

000000 = Nominal current output specified by IRNG<1:0>

111111 = Minimum negative change from nominal current – 2%

111110 = Minimum negative change from nominal current – 4%

.

.

.

100010 = Maximum negative change from nominal current – 60%

100001 = Maximum negative change from nominal current – 62%

bit 9-8 **IRNG<1:0>**: Current Source Range Select bits

11 = 100 × Base Current⁽²⁾

10 = 10 × Base Current⁽²⁾

01 = Base Current Level⁽²⁾

00 = 1000 × Base Current^(1,2)

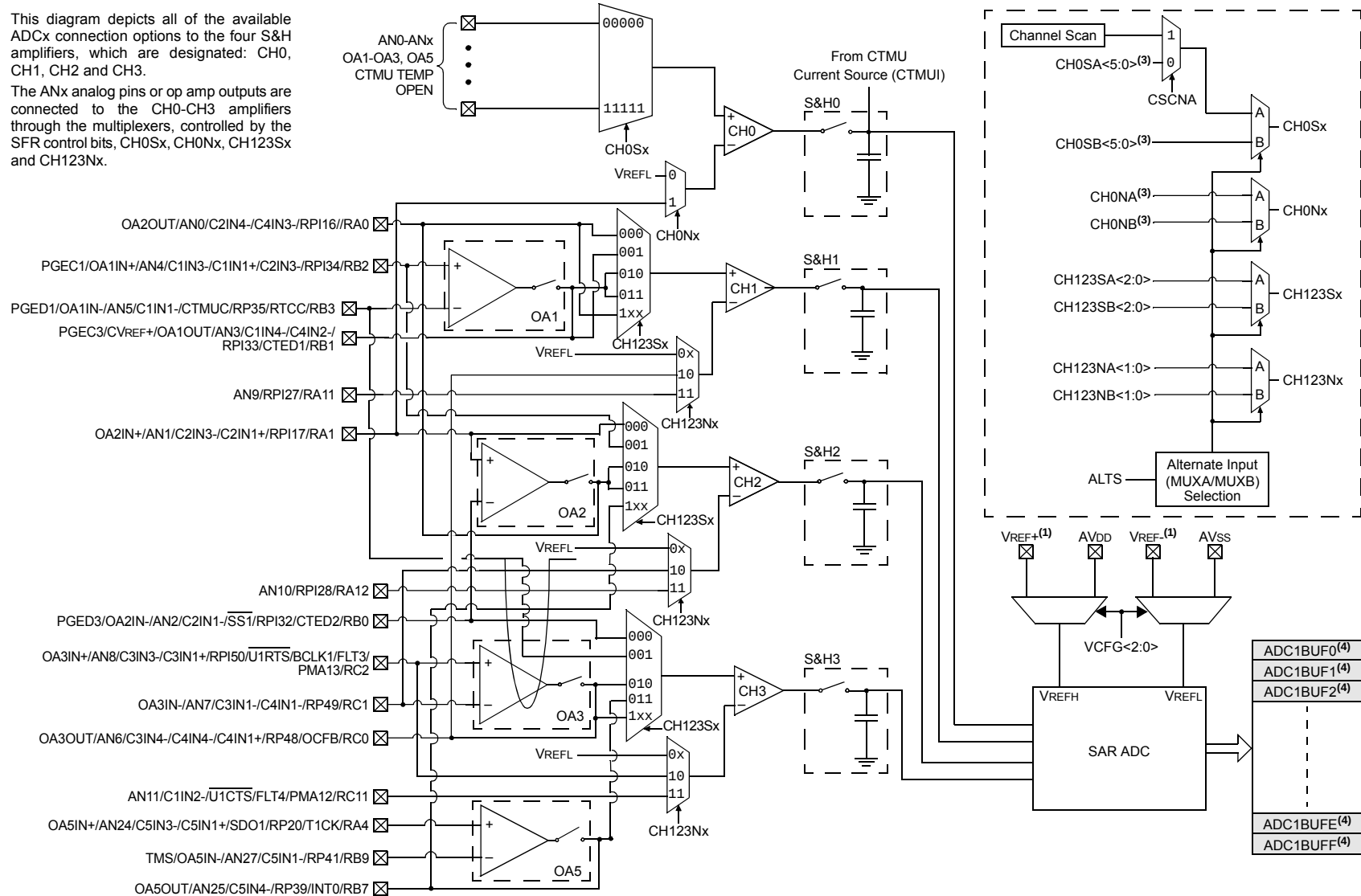
bit 7-0 **Unimplemented**: Read as '0'

- Note 1:** This current range is not available for use with the internal temperature measurement diode.
- 2:** Refer to the CTMU Current Source Specifications (Table 33-55) in **Section 33.0 “Electrical Characteristics”** for the current range selection values.
- 3:** Current sources are not generated when 12-Bit ADC mode is chosen. Current sources are active only when 10-Bit ADC mode is chosen.

FIGURE 23-1: ADCx MODULE BLOCK DIAGRAM WITH CONNECTION OPTIONS FOR ANx PINS AND OP AMPS

This diagram depicts all of the available ADCx connection options to the four S&H amplifiers, which are designated: CH0, CH1, CH2 and CH3.

The ANx analog pins or op amp outputs are connected to the CH0-CH3 amplifiers through the multiplexers, controlled by the SFR control bits, CH0Sx, CH0Nx, CH123Sx and CH123Nx.



- Note 1:** VREF+, VREF- inputs can be multiplexed with other analog inputs.
Note 2: Channels 1, 2 and 3 are not applicable for the 12-bit mode of operation.
Note 3: These bits can be updated with Step commands from the PTG module. For more information, refer to the "Peripheral Trigger Generator (PTG)" chapter in the specific device data sheet.
Note 4: When ADDMAEN (ADxCON4<8>) = 1, enabling DMA, only ADCxBUF0 is used.

27.3 RTCC Registers

REGISTER 27-1: RCFGCAL: RTCC CALIBRATION AND CONFIGURATION REGISTER⁽¹⁾

R/W-0	U-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
RTCEN ⁽²⁾	—	RTCWREN	RTCSYNC	HALFSEC ⁽³⁾	RTCOE	RTCPTR1	RTCPTR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **RTCEN:** RTCC Enable bit⁽²⁾
1 = RTCC module is enabled
0 = RTCC module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **RTCWREN:** RTCC Value Register Write Enable bit
1 = RTCVAL register can be written to by the user application
0 = RTCVAL register is locked out from being written to by the user application
- bit 12 **RTCSYNC:** RTCC Value Register Read Synchronization bit
1 = A rollover is about to occur in 32 clock edges (approximately 1 ms)
0 = A rollover will not occur
- bit 11 **HALFSEC:** Half-Second Status bit⁽³⁾
1 = Second half period of a second
0 = First half period of a second
- bit 10 **RTCOE:** RTCC Output Enable bit
1 = RTCC output is enabled
0 = RTCC output is disabled
- bit 9-8 **RTCPTR<1:0>:** RTCC Value Register Pointer bits
Points to the corresponding RTCC Value register when reading the RTCVAL register; the RTCPTR<1:0> value decrements on every access of the RTCVAL register until it reaches '00'.
- bit 7-0 **CAL<7:0>:** RTCC Drift Calibration bits
01111111 = Maximum positive adjustment; adds 508 RTCC clock pulses every one minute
.
.
.
00000001 = Minimum positive adjustment; adds 4 RTCC clock pulses every one minute
00000000 = No adjustment
11111111 = Minimum negative adjustment; subtracts 4 RTCC clock pulses every one minute
.
.
.
10000000 = Maximum negative adjustment; subtracts 512 RTCC clock pulses every one minute

- Note 1:** The RCFGCAL register is only affected by a POR.
2: A write to the RTCEN bit is only allowed when RTCWREN = 1.
3: This bit is read-only. It is cleared when the lower half of the MINSEC register is written.

28.0 PARALLEL MASTER PORT (PMP)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Parallel Master Port (PMP)” (DS70576), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Parallel Master Port (PMP) module is a parallel 8-bit I/O module, specifically designed to communicate with a wide variety of parallel devices, such as communication peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP is highly configurable.

Key features of the PMP module include:

- Eight Data Lines
- Up to 16 Programmable Address Lines
- Up to 2 Chip Select Lines
- Programmable Strobe Options:
 - Individual read and write strobes, or
 - Read/Write strobe with enable strobe
- Address Auto-Increment/Auto-Decrement
- Programmable Address/Data Multiplexing
- Programmable Polarity on Control Signals
- Legacy Parallel Slave Port (PSP) Support
- Enhanced Parallel Slave Support:
 - Address support
 - 4-byte deep auto-incrementing buffer
- Programmable Wait States

FIGURE 28-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES

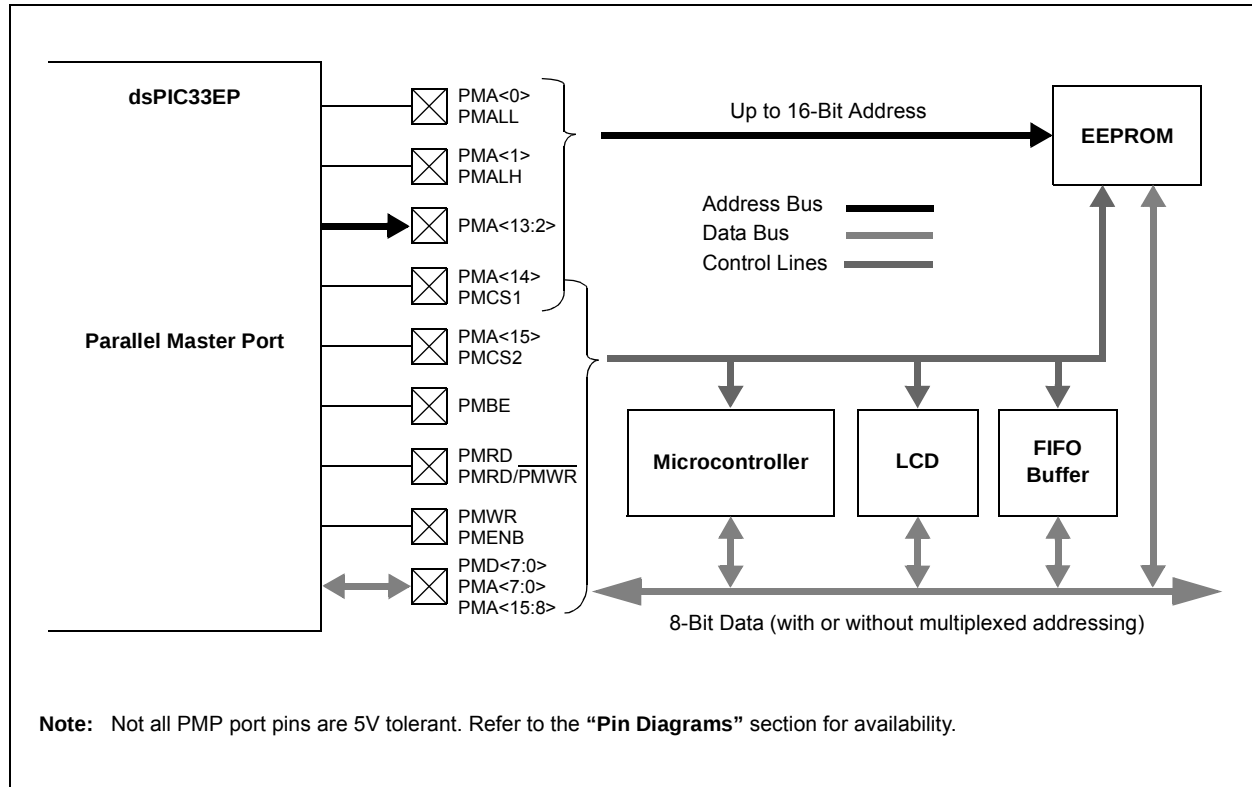


TABLE 30-2: CONFIGURATION BITS DESCRIPTION

Bit Field	Description
GCP	General Segment Code-Protect bit 1 = User program memory is not code-protected 0 = Code protection is enabled for the entire program memory space
GWRP	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
IESO	Two-Speed Oscillator Start-up Enable bit ⁽¹⁾ 1 = Starts up device with FRC, then automatically switches to the user-selected oscillator source when ready 0 = Starts up device with user-selected oscillator source
PWMLOCK	PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence
FNOSC<2:0>	Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Reserved 101 = Low-Power RC Oscillator (LPRC) 100 = Secondary Oscillator (SOSC) 011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit 1 = Allows only one reconfiguration 0 = Allows multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is the general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits 11 = Primary Oscillator mode is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
FWDTEN	Watchdog Timer Enable bit 1 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.) 0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register.)
WINDIS	Watchdog Timer Window Enable bit 1 = Watchdog Timer in Non-Window mode 0 = Watchdog Timer in Window mode
PLLKEN	PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled

Note 1: The Two-Speed Start-up is not enabled when EC mode is used since the EC clocks will be ready immediately.

dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 33-3: I/O TIMING CHARACTERISTICS

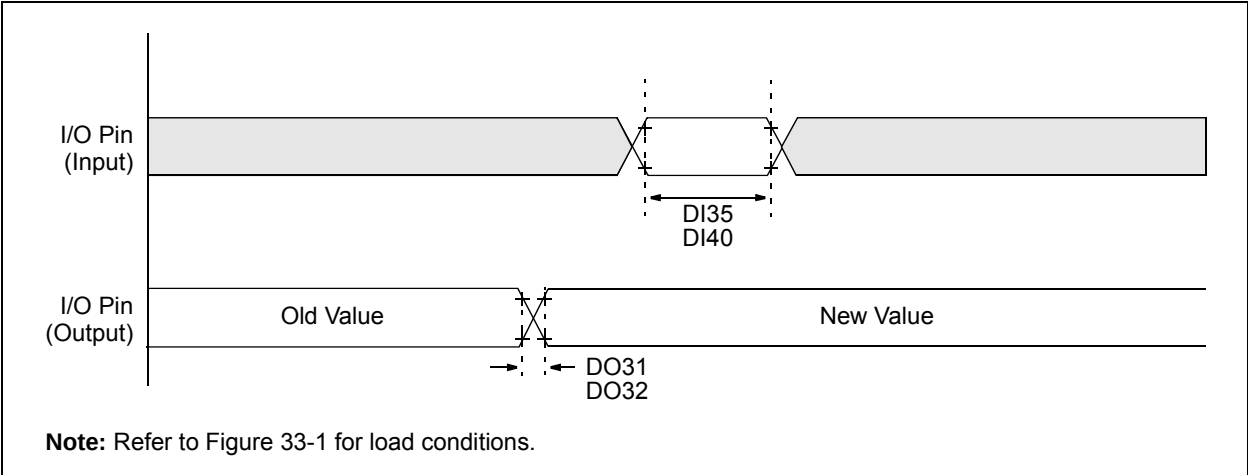
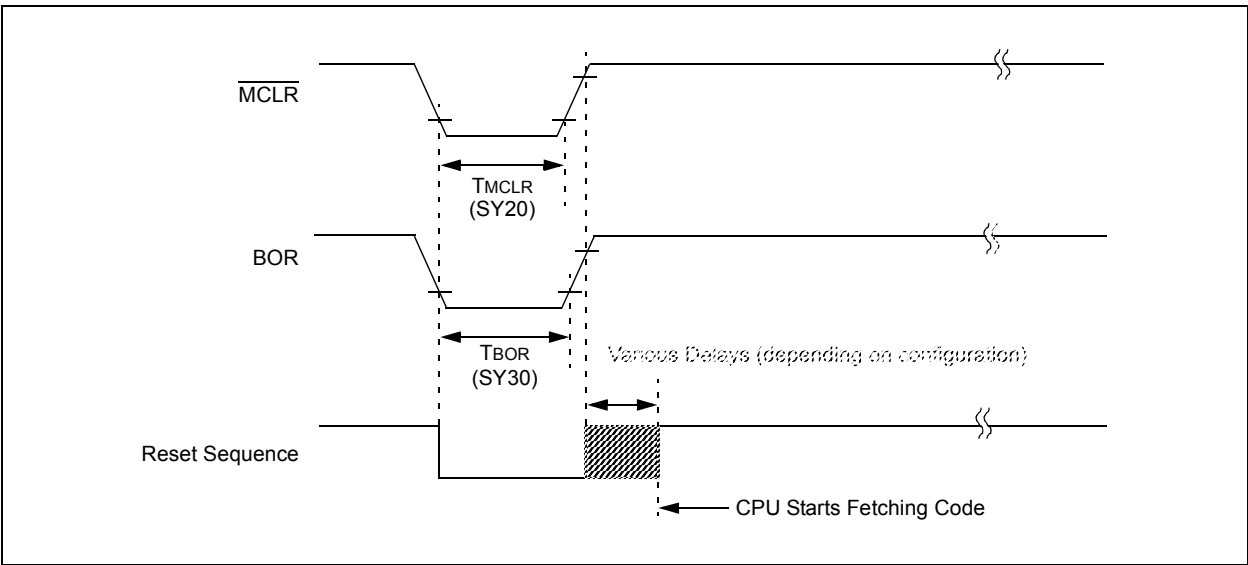


TABLE 33-20: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DO31	TioR	Port Output Rise Time	—	5	10	ns	
DO32	TioF	Port Output Fall Time	—	5	10	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	Tcy	

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

FIGURE 33-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS



dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 33-23: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Typ.	Max.	Units	Conditions
TB10	TtXH	TxCK High Time	Synchronous mode	Greater of: 20 or (TcY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescale value (1, 8, 64, 256)
TB11	TtXL	TxCK Low Time	Synchronous mode	Greater of: 20 or (TcY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescale value (1, 8, 64, 256)
TB15	TtXP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 TcY + 40)/N	—	—	ns	N = Prescale value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 TcY + 40	—	1.75 TcY + 40	ns	

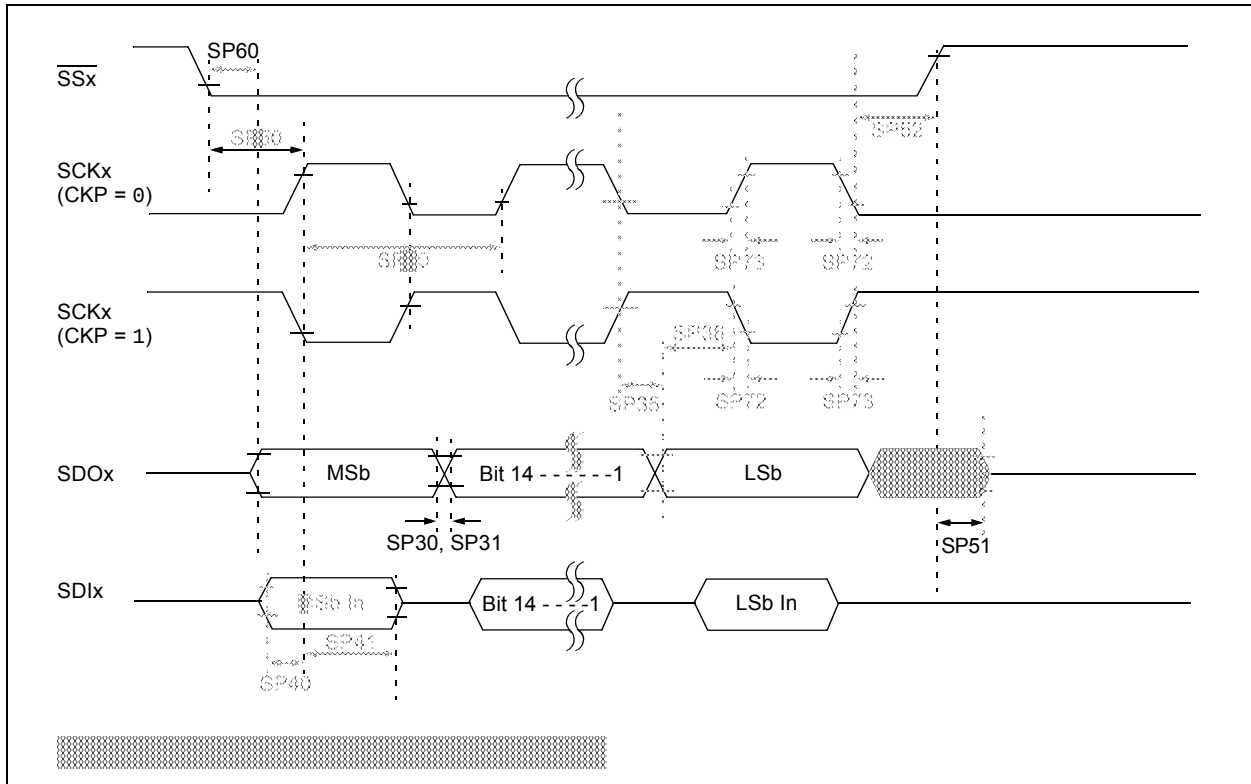
Note 1: These parameters are characterized, but are not tested in manufacturing.

TABLE 33-24: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾		Min.	Typ.	Max.	Units	Conditions
TC10	TtXH	TxCK High Time	Synchronous	TcY + 20	—	—	ns	Must also meet Parameter TC15
TC11	TtXL	TxCK Low Time	Synchronous	TcY + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtXP	TxCK Input Period	Synchronous, with Prescaler	2 TcY + 40	—	—	ns	N = Prescale value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 TcY + 40	—	1.75 TcY + 40	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

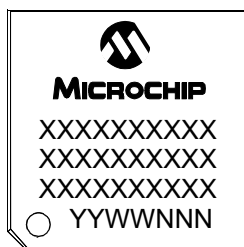
FIGURE 33-19: SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)
TIMING CHARACTERISTICS



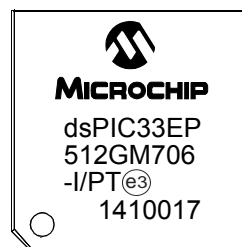
dsPIC33EPXXXGM3XX/6XX/7XX

35.1 Package Marking Information (Continued)

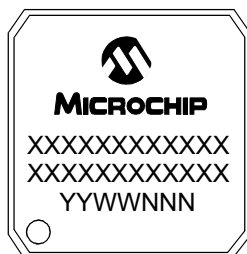
64-Lead TQFP (10x10x1 mm)



Example



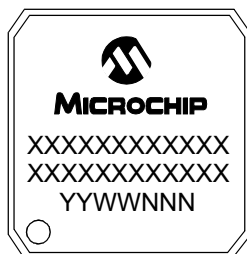
100-Lead TQFP (12x12x1 mm)



Example



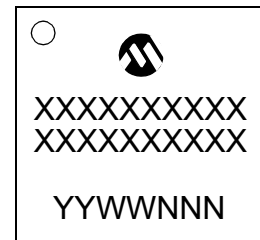
100-Lead TQFP (14x14x1 mm)



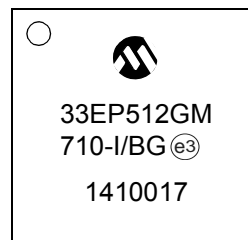
Example



121-Lead TFBGA (10x10x1.1 mm)



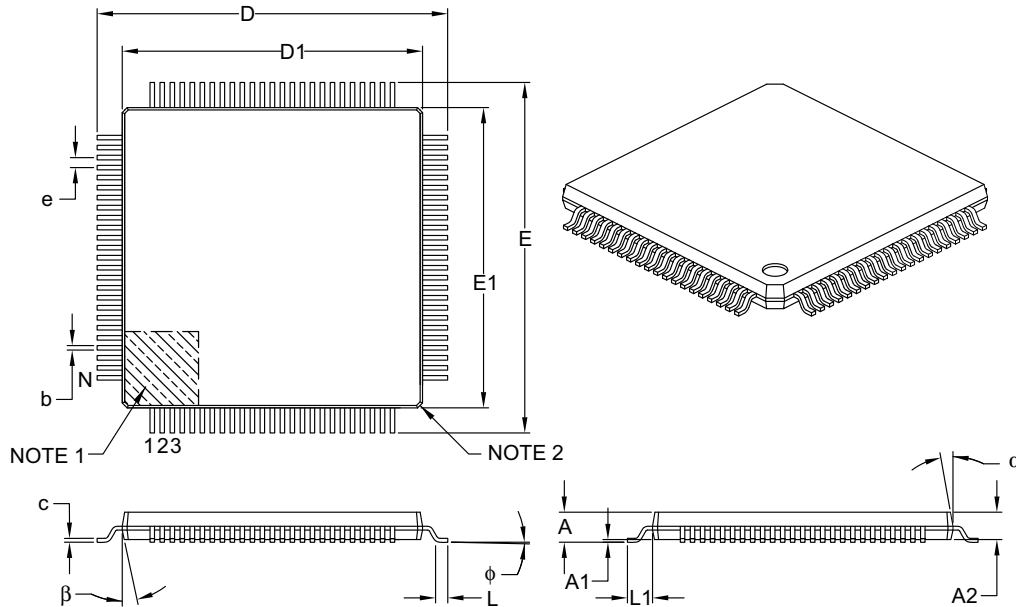
Example



dsPIC33EPXXXGM3XX/6XX/7XX

100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		100		
Lead Pitch	e		0.40 BSC		
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.95	1.00	1.05
Standoff	A1		0.05	–	0.15
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Foot Angle	φ		0°	3.5°	7°
Overall Width	E		14.00 BSC		
Overall Length	D		14.00 BSC		
Molded Package Width	E1		12.00 BSC		
Molded Package Length	D1		12.00 BSC		
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.13	0.18	0.23
Mold Draft Angle Top	α		11°	12°	13°
Mold Draft Angle Bottom	β		11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B