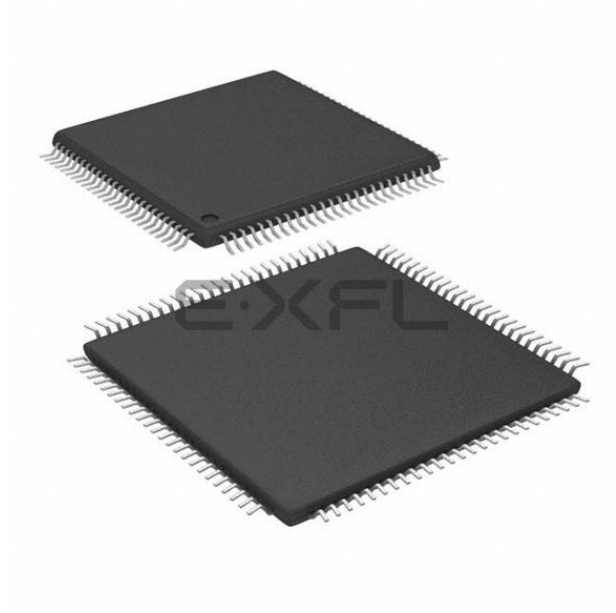
Microchip Technology - DSPIC33EP256GM310T-I/PT Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gm310t-i-pt

TABLE 4-2: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGM6XX/7XX DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	CMPIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	T6IF	—	PMPIF(1)	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	FLT1IF	RTCCIF(2)	—	DCIIF	DCIEIF	QEI1IF	PSEMIF	C2IF	C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000
IFS4	0808	—	—	CTMUIF	FLT4IF	QEI2IF	FLT3IF	PSESMIF	—	C2TXIF	C1TXIF	—	—	CRCIF	U2EIF	U1EIF	FLT2IF	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	SPI3IF	SPI3EIF	U4TXIF	U4RXIF	U4EIF	—	—	—	U3TXIF	U3RXIF	U3EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IF	PWM5IF	PWM4IF	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTEPIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	CMPIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	T6IE	—	PMPIE(1)	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	FLT1IE	RTCCIE(2)	—	DCIIE	DCIEIE	QEI1IE	PSEMIE	C2IE	C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000
IEC4	0828	—	—	CTMUIE	FLT4IE	QEI2IE	FLT3IE	PSESMIE	—	C2TXIE	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	FLT2IE	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	SPI3IE	SPI3EIE	U4TXIE	U4RXIE	U4EIE	—	—	—	U3TXIE	U3RXIE	U3EIE	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IE	PWM5IE	PWM4IE	PWM3IE	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTEPIE	—	0000
IPC0	0840	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP2	4444
IPC1	0842	—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	—	IC2IP2	IC2IP1	IC2IP0	—	DMA0IP2	DMA0IP1	DMA0IP2	4444
IPC2	0844	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0	4444
IPC3	0846	—	—	—	—	—	DMA1IP2	DMA1IP1	DMA1IP0	—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0	4444
IPC4	0848	—	CNIP2	CNIP1	CNIP0	—	CMPIP2	CMPIP1	CMPIP0	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4444
IPC5	084A	—	IC8IP2	IC8IP1	IC8IP0	—	IC7IP2	IC7IP1	IC7IP0	—	AD2IP2	AD2IP1	AD2IP0	—	INT1IP2	INT1IP1	INT1IP0	4444
IPC6	084C	—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0	—	OC3IP2	OC3IP1	OC3IP0	—	DMA2IP2	DMA2IP1	DMA2IP0	4444
IPC7	084E	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0	4444
IPC8	0850	—	C1IP2	C1IP1	C1IP0	—	C1RXIP2	C1RXIP1	C1RXIP0	—	SPI2IP2	SPI2IP1	SPI2IP0	—	SPI2EIP2	SPI2EIP1	SPI2EIP0	4444
IPC9	0852	—	IC5IP2	IC5IP1	IC5IP0	—	IC4IP2	IC4IP1	IC4IP0	—	IC3IP2	IC3IP1	IC3IP0	—	DMA3IP2	DMA3IP1	DMA3IP0	4444
IPC10	0854	—	OC7IP2	OC7IP1	OC7IP0	—	OC6IP2	OC6IP1	OC6IP0	—	OC5IP2	OC5IP1	OC5IP0	—	IC6IP2	IC6IP1	IC6IP0	4444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The PMPIF/PMPIE/PMPIPx flags are not available on 44-pin devices.

2: The RTCCIF/RTCCIE/RTCCIPx flags are not available on 44-pin devices.

TABLE 4-34: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGM3XX DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	—	INT1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	—	INT2R<6:0>							0000
RPINR3	06A6	—	—	—	—	—	—	—	—	—	T2CKR<6:0>							0000
RPINR7	06AE	—	IC2R<6:0>							—	IC1R<6:0>							0000
RPINR8	06B0	—	IC4R<6:0>							—	IC3R<6:0>							0000
RPINR9	06B2	—	IC6R<6:0>							—	IC5R<6:0>							0000
RPINR10	06B4	—	IC8R<6:0>							—	IC7R<6:0>							0000
RPINR11	06B6	—	—	—	—	—	—	—	—	—	OCFAR<6:0>							0000
RPINR12	06B8	—	FLT2R<6:0>							—	FLT1R<6:0>							0000
RPINR14	06BC	—	QEB1R<6:0>							—	QEA1R<6:0>							0000
RPINR15	06BE	—	HOME1R<6:0>							—	INDX1R<6:0>							0000
RPINR16	06C0	—	QEB2R<6:0>							—	QEA2R<6:0>							0000
RPINR17	06C2	—	HOME2R<6:0>							—	INDX2R<6:0>							0000
RPINR18	06C4	—	—	—	—	—	—	—	—	—	U1RXR<6:0>							0000
RPINR19	06C6	—	—	—	—	—	—	—	—	—	U2RXR<6:0>							0000
RPINR22	06CC	—	SCK2R<6:0>							—	SDI2R<6:0>							0000
RPINR23	06CE	—	—	—	—	—	—	—	—	—	SS2R<6:0>							0000
RPINR24	06D0	—	CSCKR<6:0>							—	CSDIR<6:0>							0000
RPINR25	06D2	—	—	—	—	—	—	—	—	—	COFSR<6:0>							0000
RPINR27	06D6	—	U3CTSR<6:0>							—	U3RXR<6:0>							0000
RPINR28	06D8	—	U4CTSR<6:0>							—	U4RXR<6:0>							0000
RPINR29	06DA	—	SCK3R<6:0>							—	SDI3R<6:0>							0000
RPINR30	06DC	—	—	—	—	—	—	—	—	—	SS3R<6:0>							0000
RPINR37	06EA	—	SYNCI1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR38	06EC	—	DTCMP1R<6:0>							—	—	—	—	—	—	—	—	0000
RPINR39	06EE	—	DTCMP3R<6:0>							—	DTCMP2R<6:0>							0000
RPINR40	06F0	—	DTCMP5R<6:0>							—	DTCMP4R<6:0>							0000
RPINR41	06F2	—	—	—	—	—	—	—	—	—	DTCMP6R<6:0>							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33/PIC24 Family Reference Manual*", **"Interrupts"** (DS70000600), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXXGM3XX/6XX/7XX CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The dsPIC33EPXXXGM3XX/6XX/7XX Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory, starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 151 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXXGM3XX/6XX/7XX devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

REGISTER 7-5: INTCON3: INTERRUPT CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	—	DAE	DOOVR	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5 **DAE:** DMA Address Error Soft Trap Status bit
1 = DMA address error soft trap has occurred
0 = DMA address error soft trap has not occurred

bit 4 **DOOVR:** DO Stack Overflow Soft Trap Status bit
1 = DO stack overflow soft trap has occurred
0 = DO stack overflow soft trap has not occurred

bit 3-0 **Unimplemented:** Read as '0'

REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SGHT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **SGHT:** Software Generated Hard Trap Status bit
1 = Software generated hard trap has occurred
0 = Software generated hard trap has not occurred

8.0 DIRECT MEMORY ACCESS (DMA)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Direct Memory Access (DMA)"** (DS70348), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The DMA Controller transfers data between Peripheral Data registers and Data Space SRAM

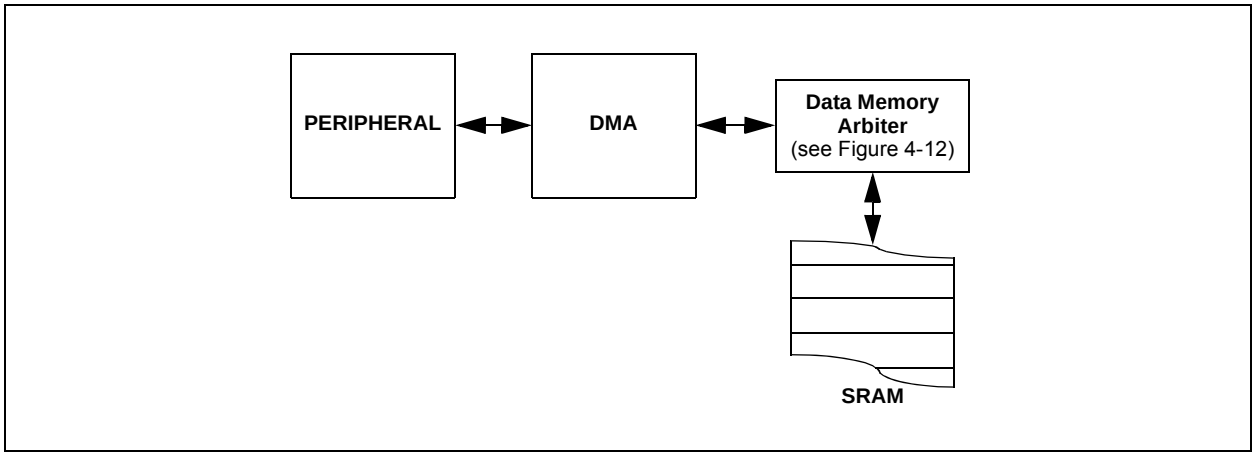
In addition, DMA can access the entire data memory space. The data memory bus arbiter is utilized when either the CPU or DMA attempts to access SRAM, resulting in potential DMA or CPU stalls.

The DMA Controller supports 4 independent channels. Each channel can be configured for transfers to or from selected peripherals. The peripherals supported by the DMA Controller include:

- CAN
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare
- DCI
- PMP
- Timers

Refer to Table 8-1 for a complete list of supported peripherals.

FIGURE 8-1: PERIPHERAL TO DMA CONTROLLER



REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Input Source Select for Synchronization and Trigger Operation bits(4)

11111 = Capture timer is unsynchronized
11110 = Capture timer is unsynchronized
11101 = Capture timer is unsynchronized
11100 = CTMU trigger is the source for the capture timer synchronization
11011 = ADC1 interrupt is the source for the capture timer synchronization(5)
11010 = Analog Comparator 3 is the source for the capture timer synchronization(5)
11001 = Analog Comparator 2 is the source for the capture timer synchronization(5)
11000 = Analog Comparator 1 is the source for the capture timer synchronization(5)
10111 = Input Capture 8 interrupt is the source for the capture timer synchronization
10110 = Input Capture 7 interrupt is the source for the capture timer synchronization
10101 = Input Capture 6 interrupt is the source for the capture timer synchronization
10100 = Input Capture 5 interrupt is the source for the capture timer synchronization
10011 = Input Capture 4 interrupt is the source for the capture timer synchronization
10010 = Input Capture 3 interrupt is the source for the capture timer synchronization
10001 = Input Capture 2 interrupt is the source for the capture timer synchronization
10000 = Input Capture 1 interrupt is the source for the capture timer synchronization
01111 = GP Timer5 is the source for the capture timer synchronization
01110 = GP Timer4 is the source for the capture timer synchronization
01101 = GP Timer3 is the source for the capture timer synchronization
01100 = GP Timer2 is the source for the capture timer synchronization
01011 = GP Timer1 is the source for the capture timer synchronization
01010 = PTGx trigger is the source for the capture timer synchronization(6)
01001 = Capture timer is unsynchronized
01000 = Output Compare 8 is the source for the capture timer synchronization
00111 = Output Compare 7 is the source for the capture timer synchronization
00110 = Output Compare 6 is the source for the capture timer synchronization
00101 = Output Compare 5 is the source for the capture timer synchronization
00100 = Output Compare 4 is the source for the capture timer synchronization
00011 = Output Compare 3 is the source for the capture timer synchronization
00010 = Output Compare 2 is the source for the capture timer synchronization
00001 = Output Compare 1 is the source for the capture timer synchronization
00000 = Capture timer is unsynchronized

Note 1: The IC32 bit in both the Odd and Even ICx must be set to enable Cascade mode.

2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.

3: This bit is set by the selected input source (selected by SYNCSEL<4:0> bits); it can be read, set and cleared in software.

4: Do not use the ICx module as its own Sync or Trigger source.

5: This option should only be selected as a trigger source and not as a synchronization source.

6: Each Input Capture x module (ICx) has one PTG input source. See **Section 25.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
PTGO8 = IC1, IC5
PTGO9 = IC2, IC6
PTGO10 = IC3, IC7
PTGO11 = IC4, IC8

REGISTER 16-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **PCLKDIV<2:0>:** PWMx Input Clock Prescaler (Divider) Select bits(1)

111 = Reserved
110 = Divide-by-64
101 = Divide-by-32
100 = Divide-by-16
011 = Divide-by-8
010 = Divide-by-4
001 = Divide-by-2
000 = Divide-by-1, maximum PWMx timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 16-9: CHOP: PWMx CHOP CLOCK GENERATOR REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
CHPCLKEN	—	—	—	—	—	CHOPCLK9	CHOPCLK8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHOPCLK7	CHOPCLK6	CHOPCLK5	CHOPCLK4	CHOPCLK3	CHOPCLK2	CHOPCLK1	CHOPCLK0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CHPCLKEN:** Enable Chop Clock Generator bit
1 = Chop clock generator is enabled
0 = Chop clock generator is disabled

bit 14-10 **Unimplemented:** Read as ‘0’

bit 9-0 **CHOPCLK<9:0>:** Chop Clock Divider bits
The frequency of the chop clock signal is given by the following expression:
Chop Frequency = (FP/PCLKDIV<2:0>)/(CHOP<9:0> + 1)

REGISTER 16-10: MDC: PWMx MASTER DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **MDC<15:0>:** PWMx Master Duty Cycle Value bits

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = Transmit has not yet started, SPIxTXB is full
0 = Transmit has started, SPIxTXB is empty

Standard Buffer Mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer Mode:
Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full
0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX family of devices contains four UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXXGM3XX/6XX/7XX device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

Note: Hardware flow control using $\overline{\text{UxRTS}}$ and $\overline{\text{UxCTS}}$ is not available on all pin count devices. See the **"Pin Diagrams"** section for availability.

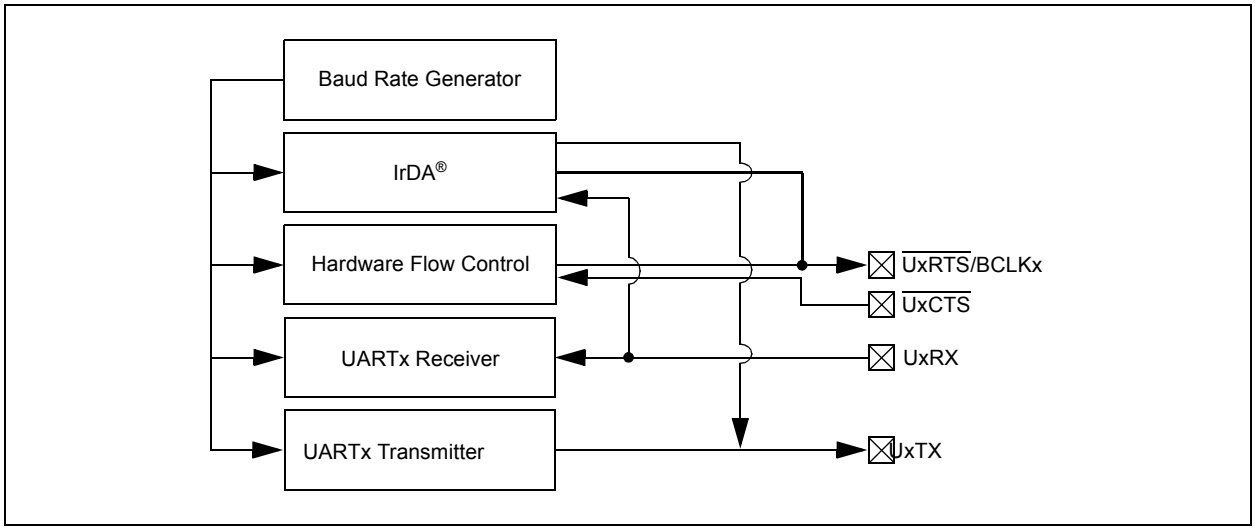
The primary features of the UART module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop Bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for All UART Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA® Support

A simplified block diagram of the UART module is shown in Figure 20-1. The UART module consists of these key hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

FIGURE 20-1: UARTx SIMPLIFIED BLOCK DIAGRAM



REGISTER 22-2: CTMUCON2: CTMU CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge Sampling Mode Selection bit
1 = Edge 1 is edge-sensitive
0 = Edge 1 is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 is programmed for a positive edge response
0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = FOSC
1110 = OSCI pin
1101 = FRC oscillator
1100 = Reserved
1011 = Internal LPRC oscillator
1010 = Reserved
100x = Reserved
01xx = Reserved
0011 = CTED1 pin
0010 = CTED2 pin
0001 = OC1 module
0000 = Timer1 module

bit 9 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control the edge source.
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control the edge source.
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge Sampling Mode Selection bit
1 = Edge 2 is edge-sensitive
0 = Edge 2 is level-sensitive

bit 6 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 is programmed for a positive edge response
0 = Edge 2 is programmed for a negative edge response

Note 1: If the TGEN bit is set to ‘1’, then the CMP1 module should be selected as the Edge 2 source in the EDG2SELx bits field; otherwise, the module will not function.

REGISTER 25-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)

bit 1-0 **PTGITM<1:0>:** PTG Input Trigger Command Operating Mode bits(1)

11 = Single level detect with step delay is not executed on exit of command (regardless of PTGCTRL command)
10 = Single level detect with step delay is executed on exit of command
01 = Continuous edge detect with step delay is not executed on exit of command (regardless of PTGCTRL command)
00 = Continuous edge detect with step delay is executed on exit of command

Note 1: These bits apply to the PTGWHI and PTGWLO commands only.

2: This bit is only used with the PTGCTRL Step command software trigger option.

REGISTER 25-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER(1,2) (CONTINUED)

bit 4 **OC1CS:** Clock Source for OC1 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 3 **OC4TSS:** Trigger/Synchronization Source for OC4 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 2 **OC3TSS:** Trigger/Synchronization Source for OC3 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 1 **OC2TSS:** Trigger/Synchronization Source for OC2 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 0 **OC1TSS:** Trigger/Synchronization Source for OC1 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: This register is only used with the PTGCTRL OPTION = 1111 Step command.

FIGURE 26-3: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM

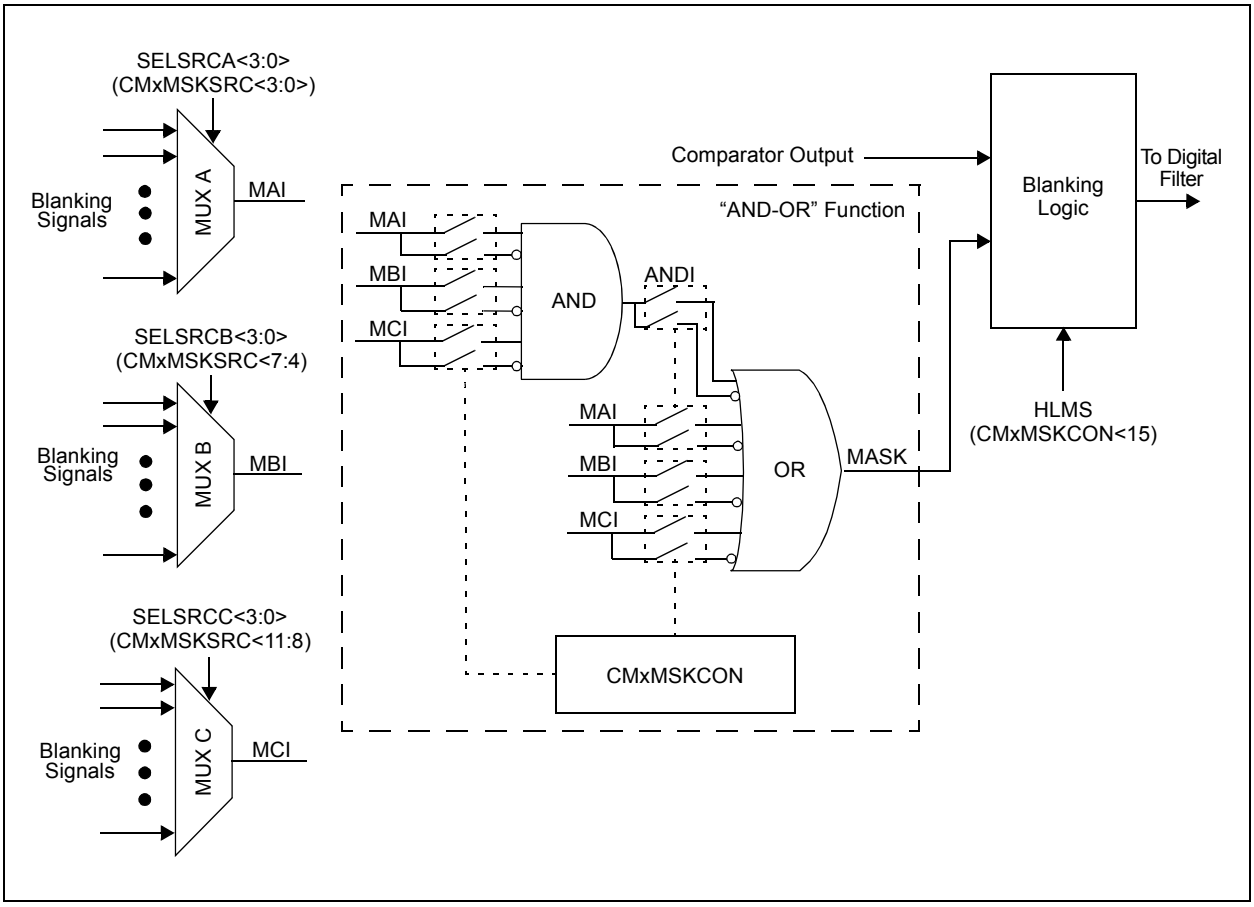
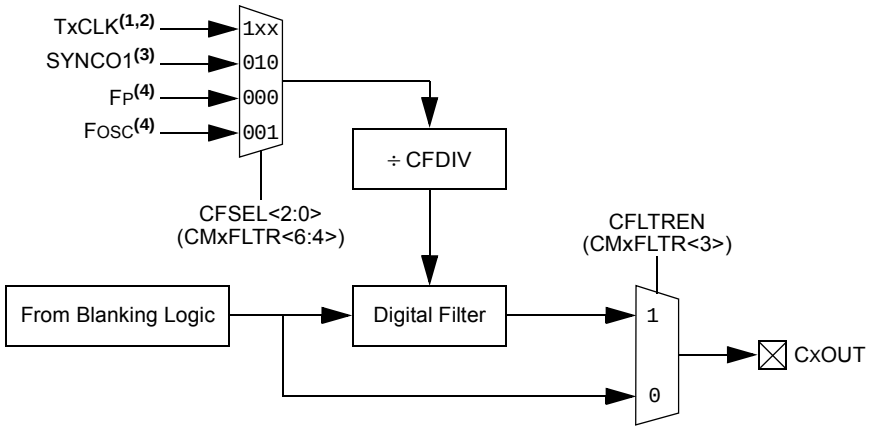


FIGURE 26-4: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM



Note 1: See the Type C Timer Block Diagram (Figure 13-2).
2: See the Type B Timer Block Diagram (Figure 13-1).
3: See the PWMx Module Register Interconnect Diagram (Figure 16-2).
4: See the Oscillator System Diagram (Figure 9-1).

REGISTER 26-2: CMxCON: OP AMP/COMPARATOR x CONTROL REGISTER (x = 1, 2, 3 OR 5)

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
CON	COE	CPOL	—	—	OPMODE(2)	CEVT(3)	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1(3)	EVPOL0(3)	—	CREF(1)	—	—	CCH1(1)	CCH0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CON:** Op Amp/Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **OPMODE:** Op Amp Select bit(2)
1 = Op amp is enabled
0 = Op amp is disabled

bit 9 **CEVT:** Comparator Event bit(3)
1 = Comparator event, according to the EVPOL<1:0> settings, occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1 (inverted polarity):
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

Note 1: Inputs that are selected and not available will be tied to V_{SS}. See the **"Pin Diagrams"** section for available inputs for each package.

2: The op amp and the comparator can be used simultaneously in these devices. The OPMODE bit only enables the op amp while the comparator is still functional.

3: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the Comparator Event bit, CEVT (CMxCON<9>), and the Comparator Combined Interrupt Flag, CMPIF (IFS1<2>), **must be cleared** before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

28.1 PMP Control Registers

REGISTER 28-1: PMCON: PARALLEL MASTER PORT CONTROL REGISTER(3)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0	R/W-0	R/W-0
CSF1	CSF0	ALP	CS2P	CS1P	BEP	WRSP	RDSP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PMPEN:** Parallel Master Port Enable bit
1 = PMP module is enabled
0 = PMP module is disabled, no off-chip access is performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **PSIDL:** PMP Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = Reserved
10 = All 16 bits of address are multiplexed on PMD<7:0> pins
01 = Lower eight bits of address are multiplexed on PMD<7:0> pins, upper eight bits are on PMA<15:8>
00 = Address and data appear on separate pins

bit 10 **PTBEEN:** Byte Enable Port Enable bit (16-Bit Master mode)
1 = PMBE port is enabled
0 = PMBE port is disabled

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
1 = PMWR/PMENB port is enabled
0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/$\overline{\text{PMWR}}$ port is enabled
0 = PMRD/$\overline{\text{PMWR}}$ port is disabled

bit 7-6 **CSF<1:0>:** Chip Select Function bits
11 = Reserved
10 = PMCS1 and PMCS2 function as Chip Select
01 = PMCS2 functions as Chip Select, PMCS1 functions as Address Bit 14
00 = PMCS1 and PMCS2 function as Address Bits 15 and 14

bit 5 **ALP:** Address Latch Polarity bit(1)
1 = Active-high ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)
0 = Active-low (PMALL and PMALH)

bit 4 **CS2P:** Chip Select 1 Polarity bit(1)
1 = Active-high ($\overline{\text{PMCS2}}$)
0 = Active-low (PMCS2)

Note 1: These bits have no effect when their corresponding pins are used as address lines.
2: PMCS1 applies to Master mode and PMCS applies to Slave mode.
3: This register is not available on 44-pin devices.

32.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

32.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

32.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

32.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

TABLE 33-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.	**Typ.(2)**	**Max.**	**Units**	**Conditions**		
Operating Current (IDD)(1)						
DC20d	6.0	18.0	mA	-40°C	3.3V	10 MIPS
DC20a	6.0	18.0	mA	+25°C		
DC20b	6.0	18.0	mA	+85°C		
DC20c	6.0	18.0	mA	+125°C		
DC21d	11.0	20.0	mA	-40°C	3.3V	20 MIPS
DC21a	11.0	20.0	mA	+25°C		
DC21b	11.0	20.0	mA	+85°C		
DC21c	11.0	20.0	mA	+125°C		
DC22d	17.0	30.0	mA	-40°C	3.3V	40 MIPS
DC22a	17.0	30.0	mA	+25°C		
DC22b	17.0	30.0	mA	+85°C		
DC22c	17.0	30.0	mA	+125°C		
DC23d	25.0	50.0	mA	-40°C	3.3V	60 MIPS
DC23a	25.0	50.0	mA	+25°C		
DC23b	25.0	50.0	mA	+85°C		
DC23c	25.0	50.0	mA	+125°C		
DC24d	30.0	60.0	mA	-40°C	3.3V	70 MIPS
DC24a	30.0	60.0	mA	+25°C		
DC24b	30.0	60.0	mA	+85°C		

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing

```
while(1)
{
NOP();
}
```

- JTAG is disabled

2: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

FIGURE 33-22: SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

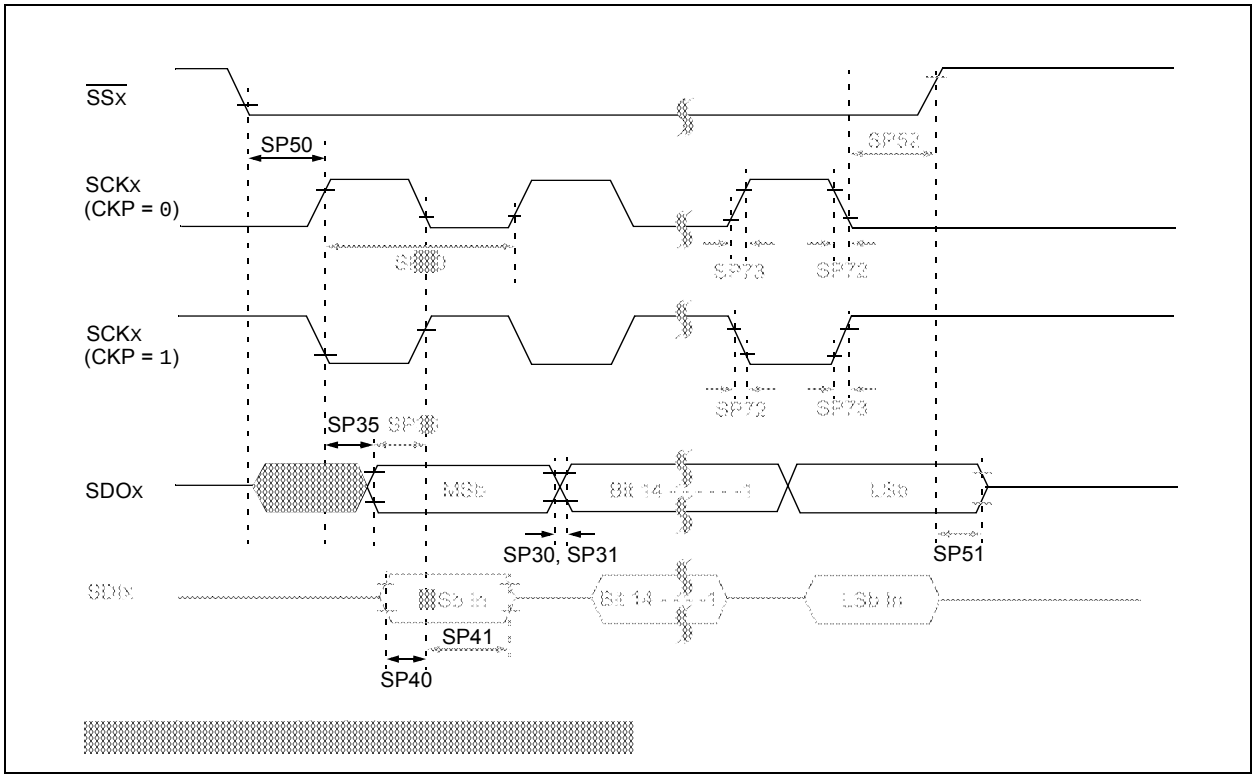


TABLE 33-59: ADCx CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(4)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADCx Clock Period	117.6	—	—	ns	
AD51	tRC	ADCx Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	14 TAD		ns	
AD56	FCNV	Throughput Rate	—	—	500	ksps	
AD57a	TSAMP	Sample Time When Sampling Any ANx Input	3 TAD	—	—	—	
AD57b	TSAMP	Sample Time When Sampling the Op Amp Outputs	3 TAD	—	—	—	
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger(1)	2 TAD	—	3 TAD	—	Auto-convert trigger is not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit(1)	2 TAD	—	3 TAD	—	
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1)(1)	—	0.5 TAD	—	—	
AD63	tDPU	Time to Stabilize Analog Stage from ADCx Off to ADCx On(1)	—	—	20	μs	**(Note 3)**

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

3: The parameter, tDPU, is the time required for the ADCx module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1<15>) = 1). During this time, the ADCx result is indeterminate.

4: These parameters are characterized, but not tested in manufacturing.